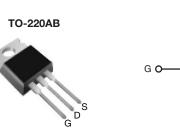


Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	400				
R _{DS(on)} (Ω)	V _{GS} = 10 V 1.0				
Q _g (Max.) (nC)	38				
Q _{gs} (nC)	5.7				
Q _{gd} (nC)	22				
Configuration	Single				



S N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- · Fast Switching
- · Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION			
Package	TO-220AB		
Lead (Pb)-free	IRF730PbF		
	SiHF730-E3		
SnPb	IRF730		
	SiHF730		

ABSOLUTE MAXIMUM RATINGS ($T_{\rm C}$	– 25 O, um					
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	400	v	
Gate-Source Voltage			V _{GS}	± 20	v	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	l_	5.5		
	VGS at TO V	T _C = 100 °C	I _D	3.5	А	
Pulsed Drain Current ^a			I _{DM}	22		
Linear Derating Factor				0.59	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	290	mJ	
Repetitive Avalanche Current ^a			I _{AR}	5.5	A	
Repetitive Avalanche Energy ^a			E _{AR}	7.4	mJ	
Maximum Power Dissipation $T_{C} = 25 \text{ °C}$			P _D	74	W	
Peak Diode Recovery dV/dt ^c			dV/dt	4.0	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for ⁻	10 s		300 ^d		
Mounting Torque	6-32 or M3 screw			10	lbf ∙ in	
Mounting Torque				1.1	N · m	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

k. V_{DD} = 50 V, starting T_J = 25 °C, L = 16 mH, R_g = 25 Ω , I_{AS} = 5.5 A (see fig. 12). c. I_{SD} \leq 5.5 A, dI/dt \leq 90 A/µs, V_{DD} \leq V_{DS}, T_J \leq 150 °C. d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

Document Number: 91047 S11-0508-Rev. C, 21-Mar-11 www.vishay.com

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THERMAL RESISTANCE RATI	NGS							
PARAMETER	SYMBOL	TYP.		MAX.		UNIT		
Maximum Junction-to-Ambient	R _{thJA}	- 62 0.50 - - 1.7						
Case-to-Sink, Flat, Greased Surface	R _{thCS}					°C/W		
Maximum Junction-to-Case (Drain)	R _{thJC}							
SPECIFICATIONS ($T_J = 25 \ ^{\circ}C$, u	Inless otherw	ise noted)						
PARAMETER	SYMBOL	TEST	CONDITI	ONS	MIN.	TYP.	MAX.	UNIT
Static							•	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0	0 V, I _D = 2	50 µA	400	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C,	l _D = 1 mA	-	0.54	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V$	/ _{GS} , I _D = 2	50 µA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	Vo	GS = ± 20 \	/	-	-	± 100	nA
7		V _{DS} = 400 V, V _{GS} = 0 V		-	-	25		
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 320 V,	V _{DS} = 320 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D	= 3.3 A ^b	-	-	1.0	Ω
Forward Transconductance	9 _{fs}	V _{DS} = 5	50 V, I _D = 3	3.3 A ^b	2.9	-	-	S
Dynamic		•						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	700	-		
Output Capacitance	C _{oss}			-	170	-	pF	
Reverse Transfer Capacitance	C _{rss}			-	64	-		
Total Gate Charge	Qg				-	-	38	<u> </u>
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V} \qquad \begin{array}{c} I_D = 3.5 \text{ A}, V_{DS} = 320 \text{ V},\\ \text{see fig. 6 and } 13^{\text{b}} \end{array}$		-	-	5.7	nC
Gate-Drain Charge	Q _{gd}				-	-	22	
Turn-On Delay Time	t _{d(on)}		1		-	10	-	1
Rise Time	t _r	V_{DD} = 200 V, I _D = 3.5 A R _g = 12 Ω , R _D = 57 Ω , see fig. 10 ^b		-	15	-	ns	
Turn-Off Delay Time	t _{d(off)}			-	38	-		
Fall Time	t _f			-	14	-		
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-		
Internal Source Inductance	L _S			-	7.5	-	nH	
Drain-Source Body Diode Characteristic	cs							
Continuous Source-Drain Diode Current	١ _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.5	А	
Pulsed Diode Forward Current ^a	I _{SM}			-	-	22		
Body Diode Voltage	V_{SD}	T _J = 25 °C, I	_S = 5.5 A,	$V_{GS} = 0 V^{b}$	-	-	1.6	V
Body Diode Reverse Recovery Time	t _{rr}	$T_{\rm J} = 25 \ ^{\circ}\text{C}, I_{\rm F} = 3.5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}^{ m b}$		-	270	530	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.8	2.2	μC	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn			-on is dor	ninated b	$v L_s and$	L _D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width \leq 300 µs; duty cycle \leq 2 %.

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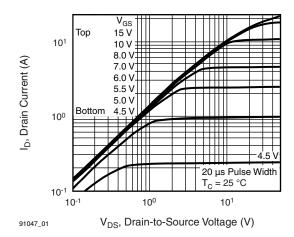


Fig. 1 - Typical Output Characteristics, $T_C = 25 \ ^{\circ}C$

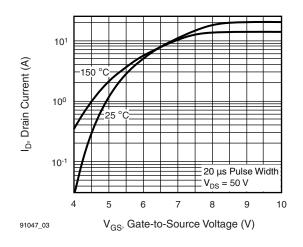


Fig. 3 - Typical Transfer Characteristics

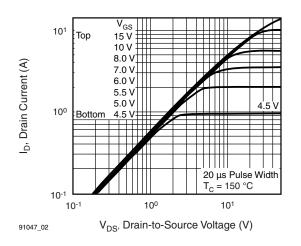


Fig. 2 - Typical Output Characteristics, $T_C = 150 \ ^{\circ}C$

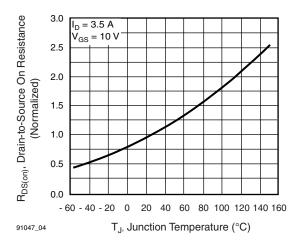


Fig. 4 - Normalized On-Resistance vs. Temperature

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3

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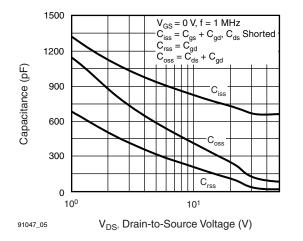
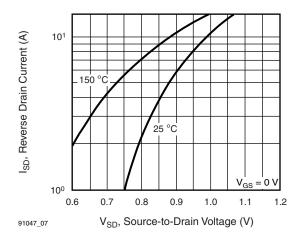
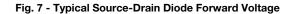


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage





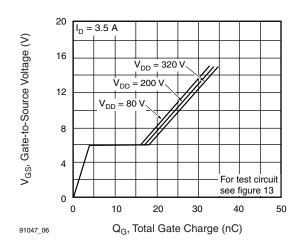


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

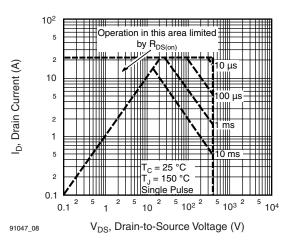


Fig. 8 - Maximum Safe Operating Area

Document Number: 91047 S11-0508-Rev. C, 21-Mar-11



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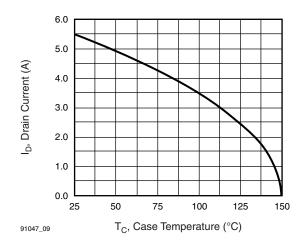


Fig. 9 - Maximum Drain Current vs. Case Temperature

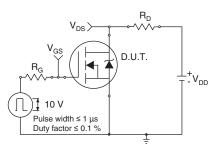


Fig. 10a - Switching Time Test Circuit

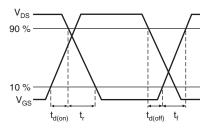


Fig. 10b - Switching Time Waveforms

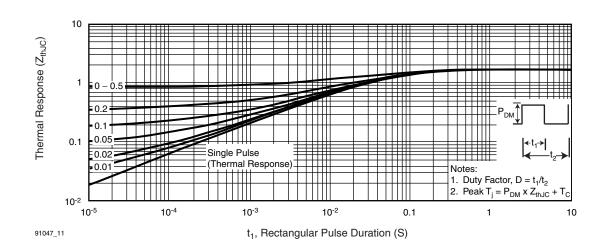


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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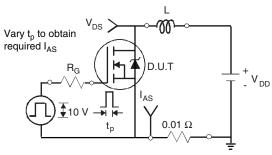


Fig. 12a - Unclamped Inductive Test Circuit

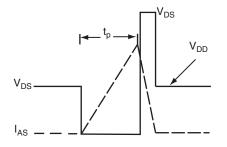
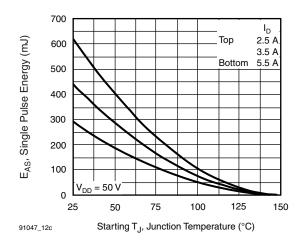
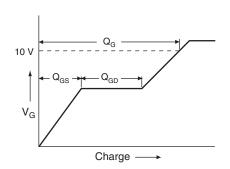


Fig. 12b - Unclamped Inductive Waveforms









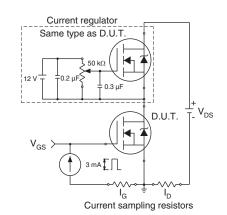
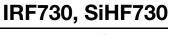


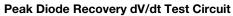
Fig. 13b - Gate Charge Test Circuit

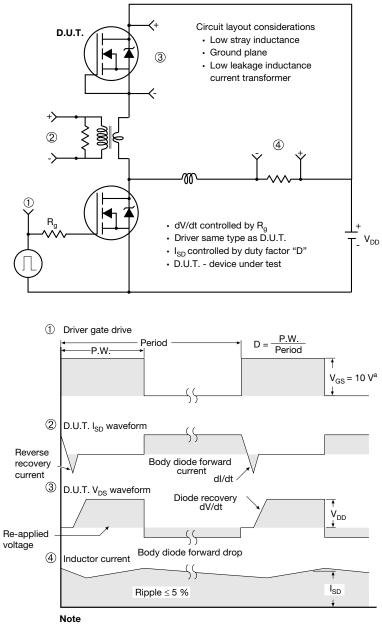
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a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIN	IETERS	INCHES		
DIN.	MIN.	MAX.	MIN.	MAX.	
А	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
E	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØР	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031					

Note

- M^{\star} = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture						
ASE		Xi'an				
		IRF 9510 744K AB				

Revison: 14-Dec-15

1 For technical questions, contact: <u>hvm@vishay.com</u> Document Number: 66542

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