

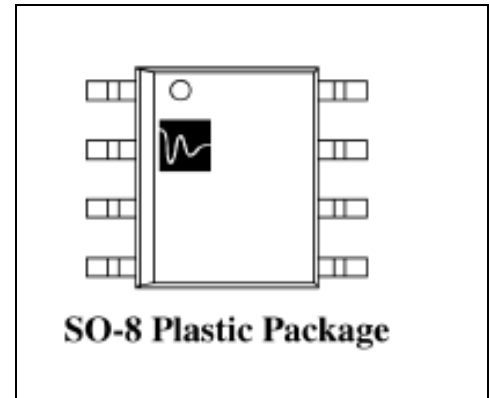
Single Supply RFIC Power Amplifier 800 - 1675 MHz Operation

Features

- >30 dBm Output Power @ 5V
- Single 3V to 5V Supply - Class A Operation
- Linear Class AB Operation (requires -VGG2)
- 50% Efficiency
- Unconditionally Stable

Applications

- Wireless Data Collection
- Cellular & Cordless Telephones
- Mobile Satellite Communications



Description

The PM2111G is a two stage high-efficiency GaAs FET RFIC power amplifier designed for wireless applications with 850 MHz to 1650 MHz center frequencies, where greater than 50 MHz bandwidths are achieved using external matching components.

In a single supply mode both stages of the PM2111G are inherently biased for (saturated) Class A operation and the current will remain constant, or increase slightly under input power back-off. By applying a negative voltage to VGG2 a more linear, Class AB operation is possible, reducing current consumption when in an idle or backed-off input power mode. Using the PM2111G in this Class AB mode has an advantage over traditional deep depletion mode devices since it does not require two negative supply voltages or sequencing circuits for safe and proper operation.

Electrical Characteristics

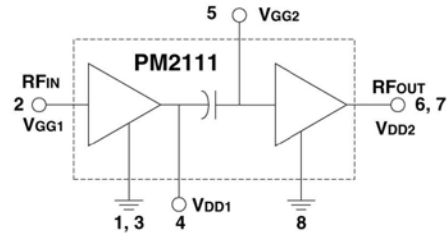
Typical values specified for $f = 1675$ MHz, $V_{DD} = 5.0V$, $T_A = +25^\circ C$, unless otherwise noted. Minimum and Maximum Specifications are Guaranteed over Frequency and Temperature. Tested in a 50Ω system using the external circuits shown on page 3.

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Frequency Range	f		800		1675	MHz
Small Signal Gain	G	$P_{IN} = -10$ dBm		29.0		dB
Input Return Loss	RL			-15.0		dB
Power Output (P1dB)	P1dB			29.5		dBm
Power Output (saturated)	P_{SAT}	$P_{IN} = +5$ dBm, $f = 915$ MHz		31.0		dBm
Power Output (saturated)	P_{SAT}	$P_{IN} = +5$ dBm, $f = 1675$ MHz	29	30.5		dBm
Power Added Efficiency	η	$P_{IN} = +5$ dBm, $f = 1675$ MHz	40	50		%
Drain Current	IDD	$P_{IN} = +5$ dBm		500	600	mA
Load VSWR for Output Stability	VSWR	Source VSWR < 1.2: 1		10:1		
Thermal Resistance	θ_{JC}	Junction to GND		35		$^\circ C/W$

Absolute Maximum Ratings

Characteristics	Symbol	Value	Units
Drain Voltage	V_{DD}	+9.0	V
Power Dissipation	P_{DISS}	1.9	W
Load VSWR	VSWR	10:1	
RF Input Power	P_{IN}	+10.0	dBm
Operating Temperature	T_{OP}	-40 to +85	°C
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Caution: Operating beyond the specified rating for any of these parameters may cause permanent damage to device.



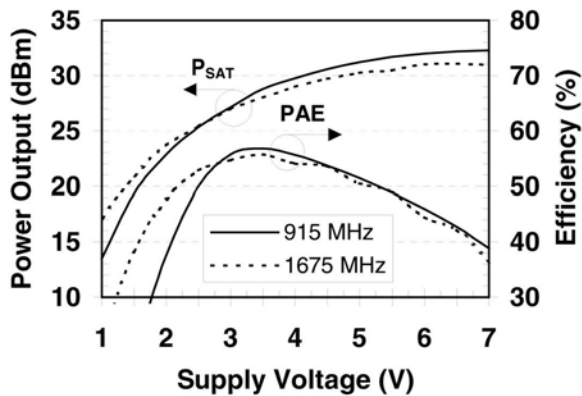
Note: Pins 1, 3 and 8 are common to the metal bottom side of package.

Typical Performance Characteristics

Obtained using external circuits shown on page 3.

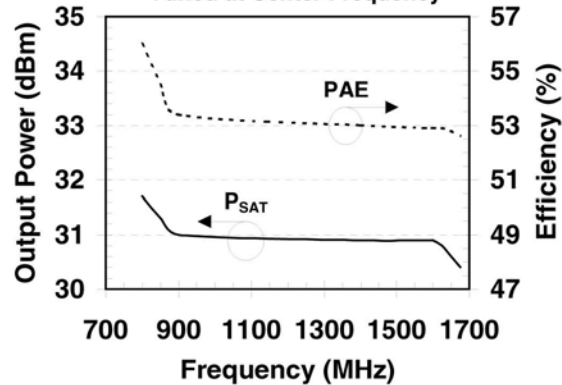
RF Power and PAE vs. Supply Voltage

$P_{in} = 6$ dBm

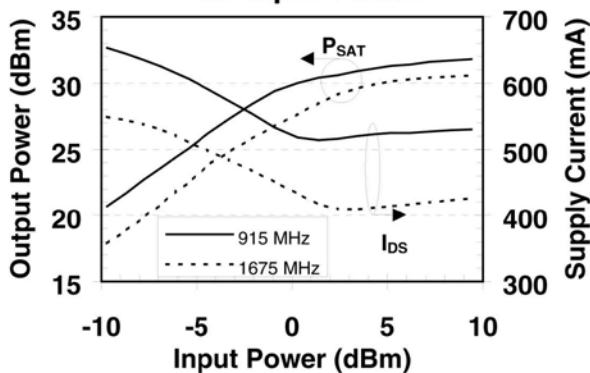


Power and Efficiency vs. Frequency

Performance Data for 30 MHz BW
Tuned at Center Frequency

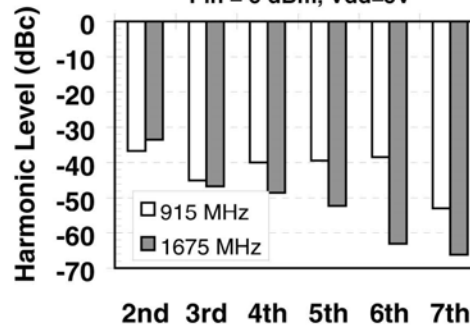


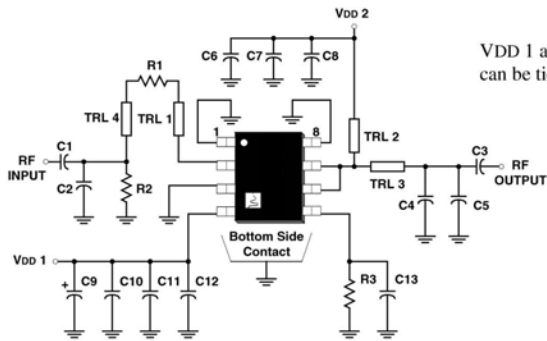
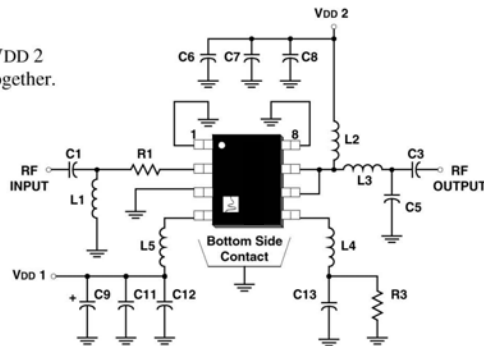
Output Power and Supply Current vs. Input Power



Harmonic Levels at P_{SAT}

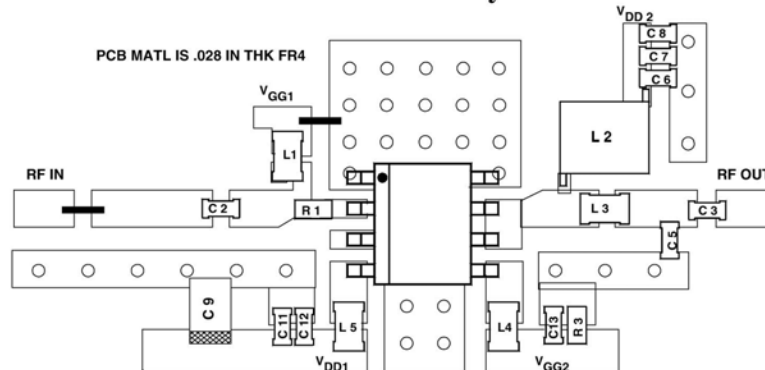
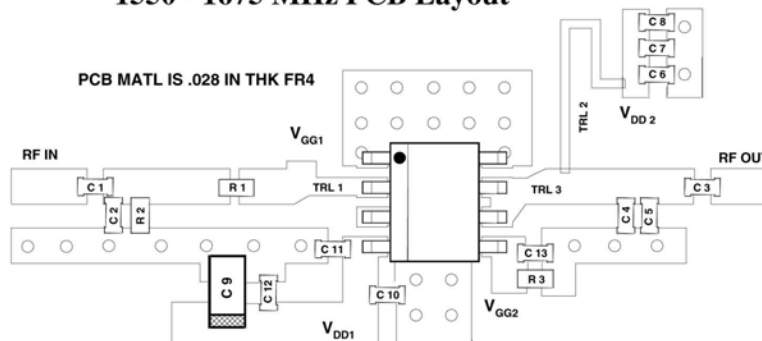
$P_{in} = 5$ dBm, $V_{dd} = 5$ V



Recommended Matching Networks for the PM2111G
1550 - 1675 MHz Schematic

800 - 950 MHz Schematic


VDD 1 and VDD 2
can be tied together.

Note: For Class AB Operation R3 is connected to V_{GG2} rather than to ground.

800 - 950 MHz PCB Layout

1550 - 1675 MHz PCB Layout


Application Information

The metalized bottom side contact area of the amplifier and the associated matching networks must have a continuous ground plane or the amplifier performance may be degraded. Terminate pins 1, 3, 8 and package base to a common ground pad. This ground pad must provide a connection to the back side of the ground plane with plated via holes. It is important to provide a good thermal path for the PM2111G since the device can dissipate up to 1.9 Watts of continuous average power.

The PM2111G requires external input, output, and interstage matching for proper operation. The input match is accomplished using C2, L1, R1 and TRL1. R1 also serves to reduce low frequency gain and improve stability. R2 is a DC return for the gate of the first stage FET at 1675 MHz. R3 and C13 limits the gate current and is only required if PIN exceeds 5 dBm. The interstage matching consists of L4 and L5. Output power match is achieved using L3/TRL3, C4, and C5. L2 must be able to support DC current in excess of 700 mA to insure reliable operation. Extensive bypassing is recommended for linear digitally modulated applications requiring good IMD performance. In addition, a negative bias voltage may be applied to V_{GG2} (pin 5) for class-AB operation. In this mode, no power sequencing is required to eliminate excess current draw prior to the application of sufficient gate voltage. The typical pinch-off voltage is -0.6V. V_{GG2} of -0.4 V provides idle currents below 200 mA.

List of Components

800-900 MHz		1550-1675 MHz	
Part	Value	Value	Size
C1	33 pF	33 pf	0603
C2		3.0 pf	0603
C3	33 pF	3.0 pf	0603
C4		1.2 pF	0603
C5	5.6 pF	1.2 pF	0603
C6	33 pF	33 DF	0603
C7	1000 pF	1000 pF	0603
C8	0.1μF	0.1μF	0603
C9	6.8μF	6.8μF	0603
C10		33 pF	0603
C11	33 pF	33 pF	0603
C12	1000 pF	0.1 pF	0603
CD13	56 pF	56 pF	0603
L1	12nH		0805
TRL1		$\theta = 15$ $f = 1675 \text{ MHz}$ $Z_o = 50 \Omega$	
L2/TRL2	18.5 nH	$\theta = 39$ $f = 1675 \text{ MHz}$ $Z_o = 95 \Omega$	0805
L3/TRL3	1.8 nH	$\theta = 29$ $f = 1675 \text{ MHz}$ $Z_o = 50 \Omega$	0805
TRL4		$\theta = 16$ $f = 1675 \text{ MHz}$ $Z_o = 50 \Omega$	
L4	6.8 nH		0805
L5	4.7 nH		0805
R1	47 Ω	5.1 Ω	0603
R2		680 Ω	0603
R3	20 Ω	20 Ω	0603

Part Number

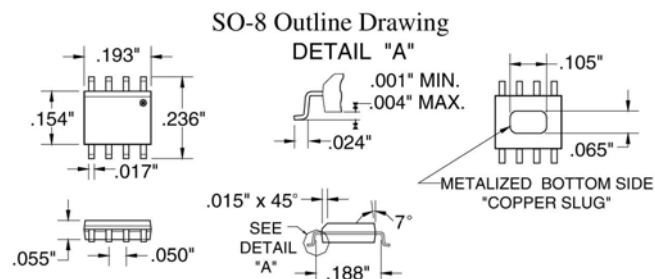
Marking System:

The PM2111G shall be marked as follows:
 Model Number:
 PM2111G
 Or
 VR2111G
 Lot Date Code:
 YYWW

Pin Connections

Pin#	Function
1	GND
2	RFIN/VGG1
3	GND
4	VOOI
5	VGG2
6	RFOIrr/VOD2
7	RFOIT/VDD2
8	GND
Base	GND

Package Specifications



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Ordering Information

Part Number	PM2111G
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