Data Sheet

5 kV RMS Dual Channel Digital Isolators

ADuM2280/ADuM2281/ADuM2285/ADuM2286

FEATURES

High isolation voltage: 5000 V rms
Up to 100 Mbps data rate
Low propagation delay: 24 ns maximum
Low dynamic power consumption
Bidirectional communication
3 V to 5 V level translation
High temperature operation: 125°C
High common-mode transient immunity: >25 kV/μs
Default high output: ADuM2280/ADuM2281
Default low output: ADuM2285/ADuM2286
16-lead SOIC wide body enhanced creepage package
Safety and regulatory approvals (pending)
- **UL recognition: 5000 V rms for 1 minute per UL 1577**
- **CSA Component Acceptance Notice #5A**
  - **IEC 60601-1: 250 V rms (reinforced)**
  - **IEC 60950-1: 400 V rms (reinforced)**
- **VDE Certificate of Conformity**
  - **DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12**
  - **V_{IORM} = 846 V peak**

Pin-compatible with ADuM220x and ADuM221x families

APPLICATIONS

General-purpose, high voltage, multichannel isolation
Medical equipment
Power supplies
RS-232/RS-422/RS-485 transceiver isolation

GENERAL DESCRIPTION

The ADuM2280/ADuM2281/ADuM2285/ADuM2286[1] (also referred to as ADuM228x in this data sheet) are 5 kV rms dual-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices and other integrated couplers.

With propagation delay at 24 ns maximum, pulse width distortion is less than 2 ns for C grade. Channel-to-channel matching is tight at 5 ns for C grade. The ADuM228x are available in two channel configurations with three different data rates up to 100 Mbps (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. Unlike other optocoupler alternatives, the ADuM228x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions. When power is first applied or is not yet applied to the input side, the ADuM2280 and ADuM2281 have a default high output and the ADuM2285 and ADuM2286 have a default low output.

FUNCTIONAL BLOCK DIAGRAMS

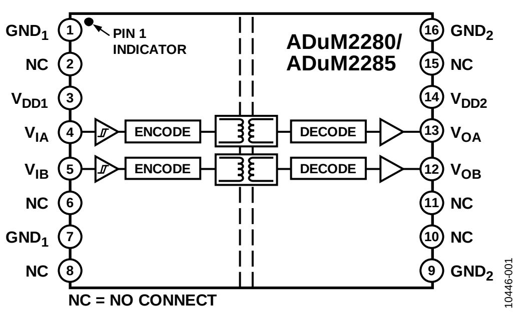


Figure 1. ADuM2280/ADuM2285 Pin-Compatible with ADuM2200/ADuM2210

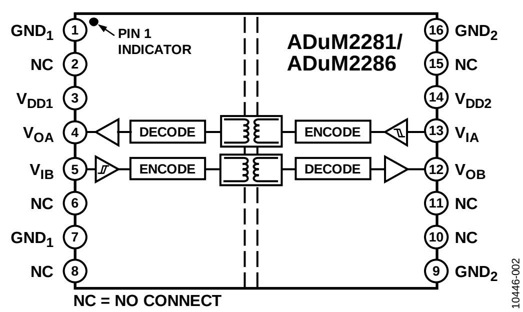


Figure 2. ADuM2281/ADuM2286 Pin-Compatible with ADuM2201/ADuM2211

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagrams ... 1
Revision History ... 2
Specifications ... 3
Electrical Characteristics—5 V Operation ... 3
Electrical Characteristics—3 V Operation ... 4
Electrical Characteristics—Mixed 5 V/3 V Operation ... 5
Electrical Characteristics—Mixed 3 V/5 V Operation ... 6
Package Characteristics ... 7
Regulatory Information ... 7
Insulation and Safety-Related Specifications ... 7
DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics ... 8
Recommended Operating Conditions ... 8
Absolute Maximum Ratings ... 9
ESD Caution ... 9
Pin Configurations and Function Descriptions ... 10
Typical Performance Characteristics ... 13
Applications Information ... 14
PC Board Layout ... 14
Propagation Delay-Related Parameters ... 14
DC Correctness and Magnetic Field Immunity ... 14
Power Consumption ... 15
Insulation Lifetime ... 16
Outline Dimensions ... 17
Ordering Guide ... 17

REVISION HISTORY

11/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, −40°C ≤ T_A ≤ 125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	C Grade Min	C Grade Typ	C Grade Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS												
Pulse Width	PW	1000			40			10			ns	Within PWD limit
Data Rate				1			25			100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			39	13	20	24	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3			2	ns	$\|t_{PLH} − t_{PHL}\|$
Change vs. Temperature			7			3			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			38			12			9	ns	Between any two units at same operating conditions
Channel Matching												
Codirectional	t_{PSKCD}			5			3			2	ns	
Opposing Direction	t_{PSKOD}			10			6			5	ns	
Jitter			2			2			1		ns	

Table 2.

Parameter	Symbol	1 Mbps—A, B, C Grades Min	Typ	Max	25 Mbps—B, C Grades Min	Typ	Max	100 Mbps—C Grade Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT												No load
ADuM2280/ADuM2285	I_{DD1}		1.3	1.6		6.2	7.0		20	25	mA	
	I_{DD2}		2.7	4.5		4.8	7.0		9.5	15	mA	
ADuM2281/ADuM2286	I_{DD1}		2.3	2.6		5.8	6.5		16	19	mA	
	I_{DD2}		2.3	2.9		5.8	6.5		16.5	19	mA	

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.54	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.6	2.0	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.09		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.04		mA/Mbps	
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		2.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		2.4		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.2		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Period	t_r		1.6		µs	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V. Minimum/maximum specifications apply over the entire recommended operation range: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V, −40°C ≤ T_A ≤ 125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	A Grade			B Grade			C Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Pulse Width	PW	1000			40			10			ns	Within PWD limit
Data Rate				1			25			100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			39	20	28	35	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3			2.5	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			7			3			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			38			16			12	ns	Between any two units at same operating conditions
Channel Matching												
Codirectional	t_{PSKCD}			5			3			2.5	ns	
Opposing-Direction	t_{PSKOD}			10			6			5	ns	
Jitter			2			2			1		ns	

Table 5.

Parameter	Symbol	1 Mbps—A, B, C Grades			25 Mbps—B, C Grades			100 Mbps—C Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												No load
ADuM2280/ADuM2285	I_{DD1}		0.75	1.4		5.1	9.0		17	23	mA	
	I_{DD2}		2.0	3.5		2.7	4.6		4.8	9	mA	
ADuM2281/ADuM2286	I_{DD1}		1.6	2.1		3.8	5.0		11	15	mA	
	I_{DD2}		1.7	2.3		3.9	6.2		11	15	mA	

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.6	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.2	1.7	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.08		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.015		mA/Mbps	
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		2.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		2.4		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.2		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		3		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Period	t_r		1.6		µs	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.0 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; and −40°C ≤ T_A ≤ 125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 7.

Parameter	Symbol	A Grade			B Grade			C Grade			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Pulse Width	PW	1000			40			10			ns	Within PWD limit
Data Rate				1			25			100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			39	13	20	26	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3			2	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			7			3			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			38			16			12	ns	Between any two units at same operating conditions
Channel Matching												
Codirectional	t_{PSKCD}			5			3			2	ns	
Opposing-Direction	t_{PSKOD}			10			6			5	ns	
Jitter			2			2			1		ns	

Table 8.

Parameter	Symbol	1 Mbps—A, B, C Grades			25 Mbps—B, C Grades			100 Mbps—C Grades			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												No load
ADuM2280/ADuM2285	I_{DD1}		1.3	1.6		6.2	7.0		20	25	mA	
	I_{DD2}		2.0	3.5		2.7	4.6		4.8	9.0	mA	
ADuM2281/ADuM2286	I_{DD1}		2.3	2.6		5.8	6.5		16	19	mA	
	I_{DD2}		1.7	2.3		3.9	6.2		11	15	mA	

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.54	0.75	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.2	2.0	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.09		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.02		mA/Mbps	
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		2.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		2.4		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.2		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Period	t_r		1.6		µs	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3 V/5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.0 V, V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; and −40°C ≤ T_A ≤ 125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	C Grade Min	C Grade Typ	C Grade Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS												
Pulse Width	PW	1000			40			10			ns	Within PWD limit
Data Rate				1			25			100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			39	16	24	30	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3			2.5	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			7			3			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			38			16			12	ns	Between any two units at same operating conditions
Channel Matching												
Codirectional	t_{PSKCD}			5			3			2.5	ns	
Opposing-Direction	t_{PSKOD}			10			6			5	ns	
Jitter			2			2			1		ns	

Table 11.

Parameter	Symbol	1 Mbps—A, B, C Grades Min	Typ	Max	25 Mbps—B, C Grades Min	Typ	Max	100 Mbps—C Grade Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT												No load
ADuM2280/ADuM2285	I_{DD1}		0.75	1.4		5.1	9.0		17	23	mA	
	I_{DD2}		2.7	4.5		4.8	7.0		9.5	15	mA	
ADuM2281/ADuM2286	I_{DD1}		1.6	2.1		3.8	5.0		11	15	mA	
	I_{DD2}		1.7	2.3		5.8	6.5		16.5	19	mA	

Table 12. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.75	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.6	2.0	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.08		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		2.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		2.4		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.2		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Period	t_r		1.6		µs	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
RESISTANCE AND CAPACITANCE						
Resistance (Input-to-Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at the center of the package underside; test conducted on a 4-layer board with thin traces

[1] This device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM228x will be approved by the organizations listed in Table 14. See Table 19 and the Absolute Maximum Ratings section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 14.

UL (Pending)	CSA (Pending)	VDE (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single Protection 5000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage Reinforced insulation per IEC 60601-1 250 V rms (353 V peak) maximum working voltage	Reinforced insulation, 846 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM228x is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM228x is proof tested by applying an insulation test voltage ≥1590 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 15.

Parameter	Symbol	Value	Unit	Test Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap	L(I01)	8.0 min	mm	Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PC board layout
Minimum External Tracking (Creepage)	L(I02)	8.3 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits. Note that the asterisk (*) branded on packages denotes DIN V VDE V 0884-10 approval for 846 V_{PEAK} working voltage.

Table 16.

Description	Test Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to II	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	846	V_{PEAK}
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m$ = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1590	V_{PEAK}
Input-to-Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini}=60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1269	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1818	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	6000	V_{PEAK}
Withstand Isolation Voltage	1 minute withstand rating	V_{ISO}	5000	V_{RMS}
Surge Isolation Voltage	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Side 1 I_{DD1} Current		I_{S1}	555	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

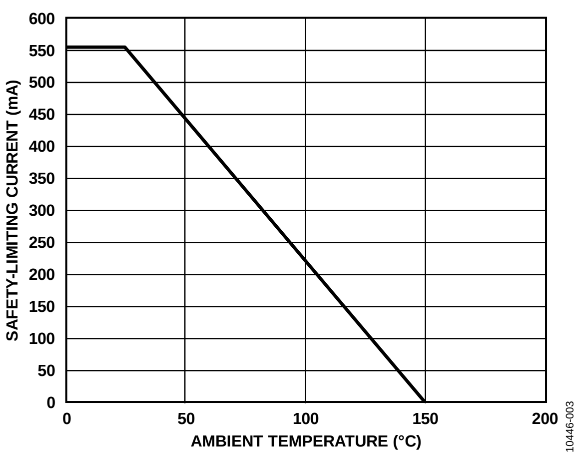


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 17.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+125	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] See the DC Correctness and Magnetic Field Immunity section. All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 18.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB})	−0.5 V to V_{DD2} + 0.5 V
Average Output Current per Pin[1]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[2]	−100 kV/μs to +100 kV/μs

[1] See Figure 3 for maximum rated current values for various temperatures.
[2] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

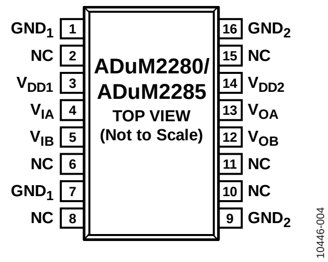
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 19. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform	1131	V peak	50-year minimum lifetime
DC Voltage	1131	V peak	50-year minimum lifetime

[1] Refers to the continuous voltage magnitude imposed across theisolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



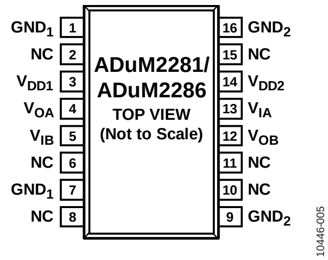
NOTES
1. NC = NO CONNECT.
2. PIN 1 AND PIN 7 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_1 IS RECOMMENDED.
3. PIN 9 AND PIN 16 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_2 IS RECOMMENDED.

Figure 4. ADuM2280/ADuM2285 Pin Configuration

Table 20. ADuM2280/ADuM2285 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND_1	Ground 1. Ground reference for Isolator Side 1.
2	NC	No internal connection.
3	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
4	V_{IA}	Logic Input A.
5	V_{IB}	Logic Input B.
6	NC	No internal connection.
7	GND_1	Ground 1. Ground reference for Isolator Side 1.
8	NC	No internal connection.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	NC	No internal connection.
11	NC	No internal connection.
12	V_{OB}	Logic Output B.
13	V_{OA}	Logic Output A.
14	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.
15	NC	No internal connection.
16	GND_2	Ground 2. Ground reference for Isolator Side 2.

For specific layout guidelines, refer to the AN-1109 Application Note, *Recommendations for Control of Radiated Emissions with i*Coupler *Devices*.



NOTES:
1. NC = NO CONNECT.
2. PIN 1 AND PIN 7 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_1 IS RECOMMENDED.
3. PIN 9 AND PIN 16 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_2 IS RECOMMENDED.

Figure 5. ADuM2281/ADuM2286 Pin Configuration

Table 21. ADuM2281/ADuM2286 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND_1	Ground 1. Ground reference for Isolator Side 1.
2	NC	No internal connection.
3	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
4	V_{OA}	Logic Output A.
5	V_{IB}	Logic Input B.
6	NC	No internal connection.
7	GND_1	Ground 1. Ground reference for Isolator Side 1.
8	NC	No internal connection.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	NC	No internal connection.
11	NC	No internal connection.
12	V_{OB}	Logic Output B.
13	V_{IA}	Logic Input A.
14	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.
15	NC	No internal connection.
16	GND_2	Ground 2. Ground reference for Isolator Side 2.

For specific layout guidelines, refer to the AN-1109 Application Note, *Recommendations for Control of Radiated Emissions with* iCoupler *Devices*.

Table 22. ADuM2280 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	Outputs return to the input state within 1.6 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1.6 µs of V_{DDO} power restoration.

Table 23. ADuM2281 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	H	Outputs return to the input state within 1.6 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	H	Indeterminate	Outputs return to the input state within 1.6 µs of V_{DDO} power restoration.

Table 24. ADuM2285 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1.6 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1.6 µs of V_{DDO} power restoration.

Table 25. ADuM2286 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	L	Outputs return to the input state within 1.6 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	L	Indeterminate	Outputs return to the input state within 1.6 µs of V_{DDO} power restoration.

TYPICAL PERFORMANCE CHARACTERISTICS

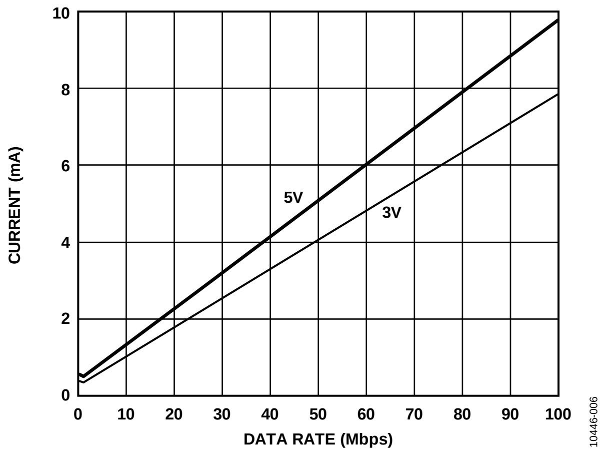


Figure 6. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3 V Operation

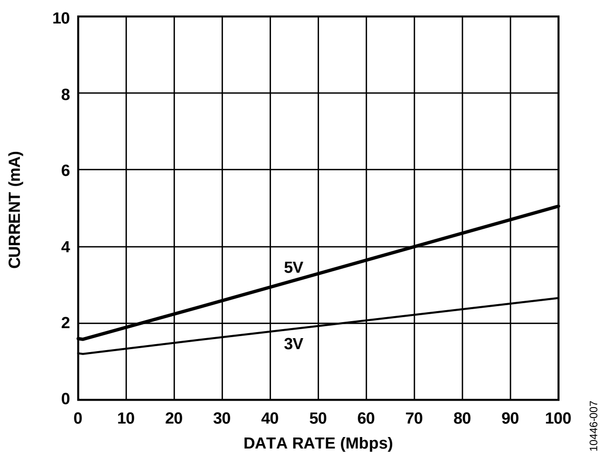


Figure 7. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

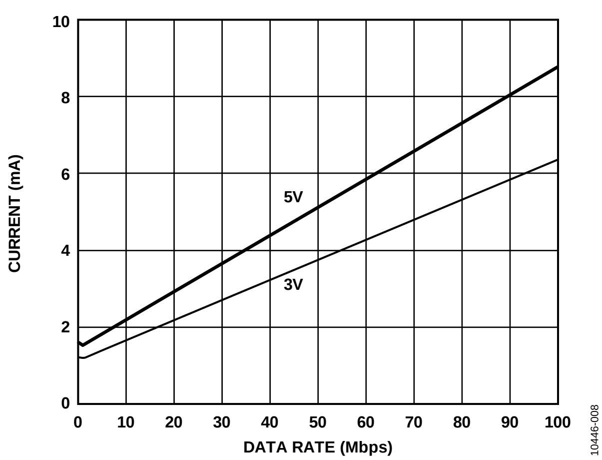


Figure 8. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

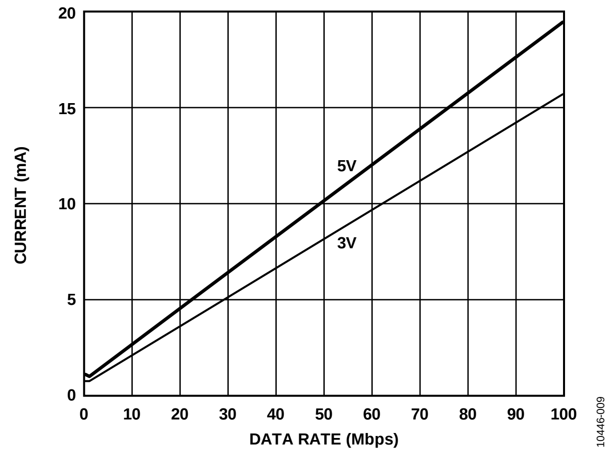


Figure 9. Typical ADuM2280 or ADuM2285 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

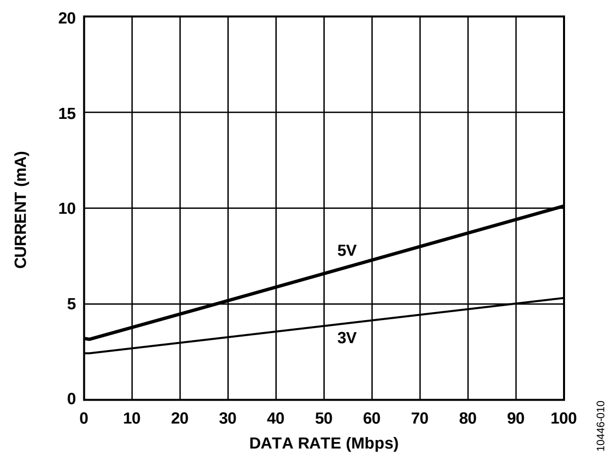


Figure 10. Typical ADuM2280 or ADuM2285 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

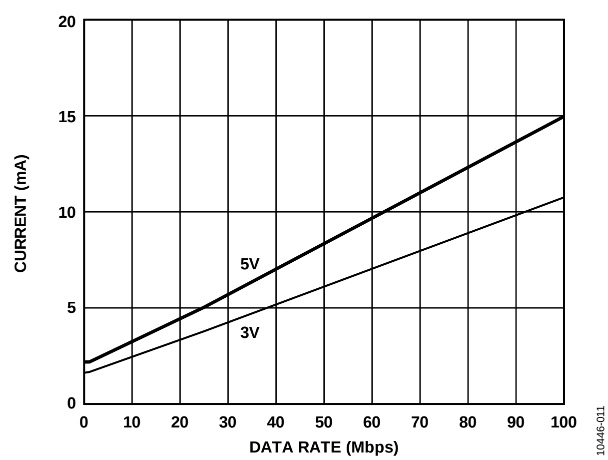


Figure 11. Typical ADuM2281 or ADuM2286 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM228x digital isolators requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 12). Bypass capacitors are most conveniently connected between Pin 1 and Pin 3 for V_{DD1} and between Pin 14 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 3 and Pin 7 and between Pin 9 and Pin 14 should be considered unless the ground pair on each package side are connected close to the package.

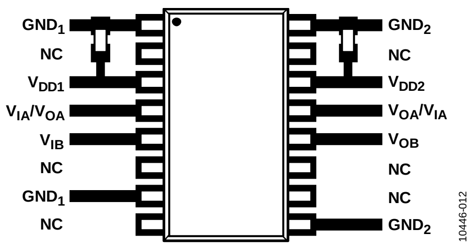


Figure 12. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's absolute maximum ratings, thereby leading to latch-up or permanent damage.

The ADuM228x can readily meet CISPR 22 Class A (and FCC Class A) emissions standards, as well as the more stringent CISPR 22 Class B (and FCC Class B) standards in an unshielded environment, with proper PCB design choices. Refer to the AN-1109 Application Note for PCB-related EMI mitigation techniques, including board layout and stack-up issues.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time of a low-to-high transition.

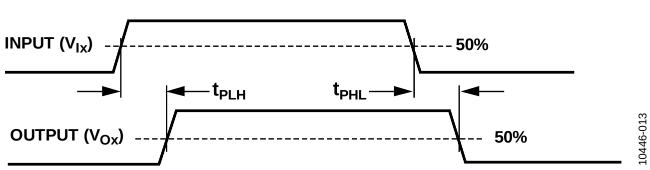


Figure 13. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM228x component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM228x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is, therefore, either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output.

If the decoder receives no pulses for more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default low state by the watchdog timer circuit.

The limitation on the device's magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines such conditions. The ADuM2280 is examined in a 3 V operating condition because it represents the most susceptible mode of operation of this product.

The pulses at the transformer output have an amplitude greater than 1.5 V. The decoder has a sensing threshold of about 1.0 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density.
r_n is the radius of the n^{th} turn in the receiving coil.
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM2280 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 14.

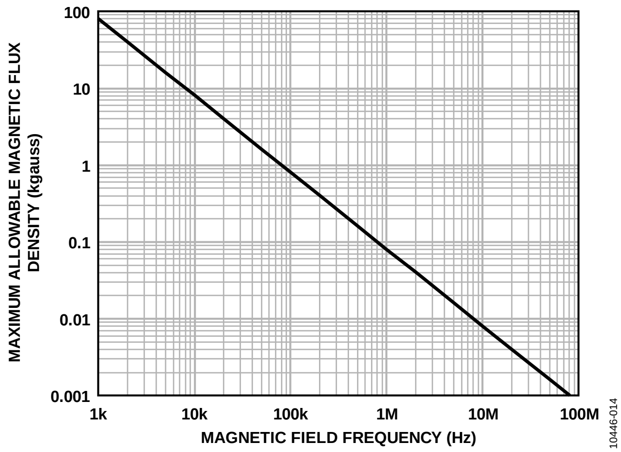


Figure 14. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.08 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs, with the worst-case polarity, during a transmitted pulse, it would reduce the received pulse from >1.0 V to 0.75 V. This is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM2280 transformers. Figure 15 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM2280 is very insensitive to external fields. Only extremely large, high frequency currents, very close to the component could potentially be a concern. For the 1 MHz example noted, one would have to place a 0.2 kA current 5 mm away from the ADuM2280 to affect component operation.

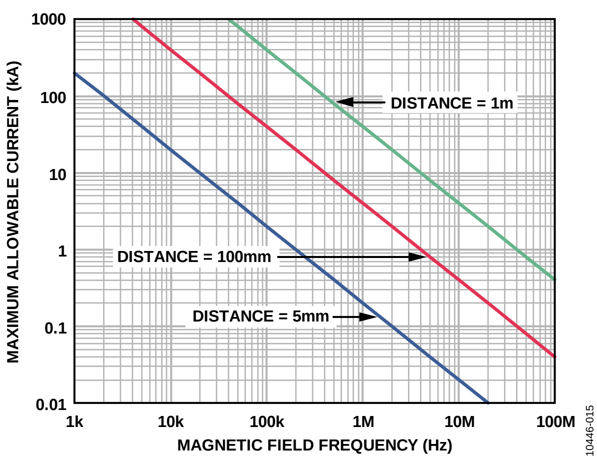


Figure 15. Maximum Allowable Current for Various Current to ADuM2280 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Take care to avoid PCB structures that form loops.

POWER CONSUMPTION

The supply current at a given channel of the ADuM228x isolators is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \qquad f \leq 0.5\, f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5\, f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \qquad f \leq 0.5\, f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \qquad f > 0.5\, f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.
f_r is the input stage refresh rate (Mbps) = $1/T_r$ (µs).
$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 6 and Figure 7 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 shows the per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 11 show the total V_{DD1} and V_{DD2} supply current as a function of data rate for the ADuM2280/ADuM2285 and ADuM2281/ADuM2286 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM228x.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 19 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM228x depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 16, Figure 17, and Figure 18 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 19 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage case. Any cross-insulation voltage waveform that does not conform to Figure 17 or Figure 18 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 19.

Note that the voltage presented in Figure 17 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

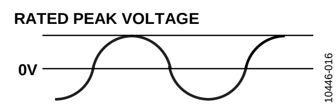


Figure 16. Bipolar AC Waveform

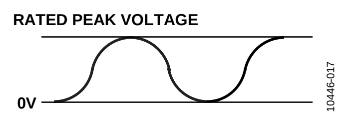


Figure 17. Unipolar AC Waveform

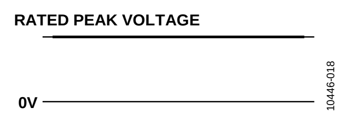


Figure 18. DC Waveform

OUTLINE DIMENSIONS

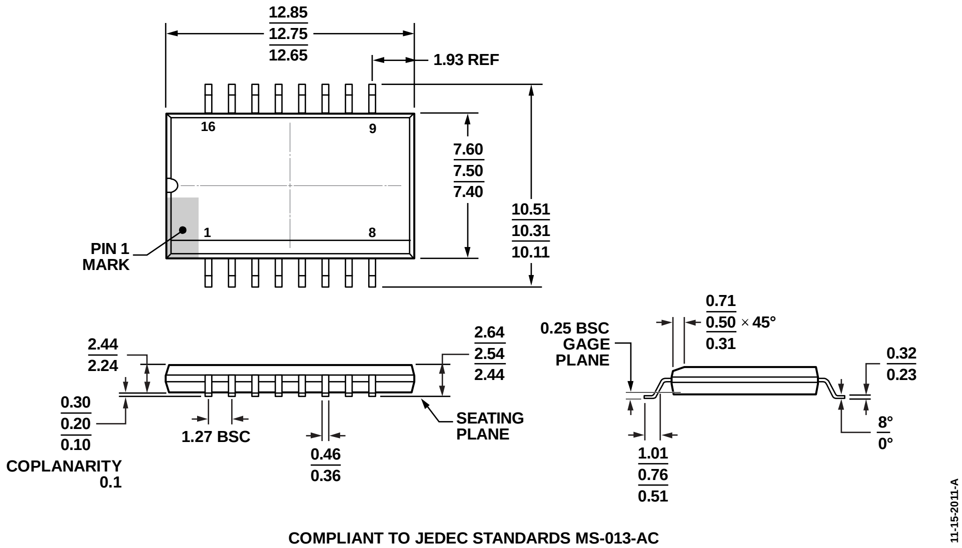


Figure 19. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-16-2)
Dimension shown in millimeters

ORDERING GUIDE

Model[1, 2]	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Max Data Rate	Max Prop Delay, 5 V	Output Default State	Temperature Range	Package Description	Package Option
ADuM2280ARIZ	2	0	1 Mbps	50	High	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2280BRIZ	2	0	25 Mbps	35	High	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2280CRIZ	2	0	100 Mbps	24	High	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2281ARIZ	1	1	1 Mbps	50	High	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2281BRIZ	1	1	25 Mbps	35	High	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2281CRIZ	1	1	100 Mbps	24	High	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2285ARIZ	2	0	1 Mbps	50	Low	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2285BRIZ	2	0	25 Mbps	35	Low	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2285CRIZ	2	0	100 Mbps	24	Low	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2286ARIZ	1	1	1 Mbps	50	Low	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2286BRIZ	1	1	25 Mbps	35	Low	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2
ADuM2286CRIZ	1	1	100 Mbps	24	Low	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2

[1] Tape and reel is available. The addition of an -RL suffix designates a 13” (1,000 units) tape and reel option.
[2] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES