PIC16(L)F1784/6/7 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F1784/6/7 family devices that you have received conform functionally to the current Device Data Sheet (DS41637**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1784/6/7 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**C1**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1784/6/7 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>[(1),(2)]		
	DEV<8:0>	REV<4:0> Silicon Revision	
		C0	C1
PIC16F1784	10 1010 010	0 1001	0 1010
PIC16LF1784	10 1010 111	0 1001	0 1010
PIC16F1786	10 1010 011	0 1001	0 1010
PIC16LF1786	10 1011 000	0 1001	0 1010
PIC16F1787	10 1010 100	0 1001	0 1010
PIC16LF1787	10 1011 001	0 1001	0 1010

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16(L)F178X Memory Programming Specification"* (DS41457) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: **SILICON ISSUE SUMMARY**

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]	
				C0	**C1**
Comparator	Low-Power mode	1.1	Improper Low-Power mode operation.	X	X
PSMC	Rising Edge Input	2.1	Period and falling edge race condition.	X	X
PSMC	64 MHz Clock	2.2	Failure to operate when PLLEN Configuration bit is set.	X	X
Resets	Low-Power Sleep	3.1	$\overline{\text{MCLR}}$ Reset during low-power Sleep will be reported as a POR Reset (PIC16F1784/6/7 devices only).	X	X
CPU	BRA/BRW	4.1	An interrupt during execution of BRA or BRW instruction can return an incorrect PC value.	X	
CCP3	Capture	5.1	TTL Input suppresses capture event.	X	
MSSP	Capture	6.1	Bit 1 always '0' when CKE = 0	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**C1**).

1. Module: Comparator

1.1 No Low-Power, No Low-Speed Mode

The comparator operation in Low-Power, Low-Speed mode (CxSP = 0) may not perform properly.

Work around

Use the comparator in High-Power mode.

Affected Silicon Revisions

C0	C1						
X	X						

2. Module: PSMC

2.1 Rising Edge Inhibit

When the period and falling edge sources are from the same asynchronous input, then a race condition may occur where the period is detected before the falling edge. When this occurs, the falling edge properly terminates the cycle but subsequent rising edge inputs are ignored.

Work around

To configure the PSMC for fixed off-time and variable frequency, set the following:

- Period = Asynchronous feedback
- Rising Event = Synchronous @ PSMCxPH = 0
- Falling Event = Synchronous @ PSMCxDC = Off Time
- Output inverted so drive time is from falling event to period event.

Affected Silicon Revisions

C0	C1						
X	X						

2.2 64 MHz Clock

When the Configuration bits select both PLL enabled and INTOSC as the default system clock, then the 64 MHz PSMC clock will not operate after a device Reset until the IRCF<3:0> bits of the OSCCON register are set to '111x'. The IRCF bits can then be set to any desired value and the 64 MHz clock will continue to operate.

Work around

Ensure that the PLLEN bit of the CONFIG2 register is cleared when the FOSC<2:0> bits of the CONFIG1 register select the INTOSC (FOSC<2:0> = '100').

Affected Silicon Revisions

C0	C1						
X	X						

3. Module: Resets

3.1 Low-Power Sleep (PIC16F1784/6/7 devices only)

When the device is in low-power Sleep (VREGPM = 1 and SLEEP instruction is executed), a $\overline{MCLR}$ Reset will be reported as a POR Reset:

- $\overline{PD}$ = 1
- $\overline{POR}$ = 0
- $\overline{RDMCLR}$ = 1

Work around

Use Normal-Power Sleep mode (VREGPM = 0).

Affected Silicon Revisions

C0	C1						
X	X						

4. Module: CPU

4.1 BRA/BRW

If a BRA or BRW instruction is executed concurrently with an interrupt event, the ISR routine can restore the PC to an incorrect value.

Work around

Use the GOTO instruction rather than the BRA or BRW instruction.

Affected Silicon Revisions

C0	C1						
X							

5. Module: CCP3

5.1 CCP3 Capture (PIC16(L)F1784/7 only)

When the input threshold control for RE0 is configured for TTL, the CCP3 capture input is ignored.

Work around

Use ST Threshold.

Affected Silicon Revisions

C0	C1						
X							

6. Module: MSSP

6.1 MSSP SPI Mode

In Master and Slave mode, when the CKE bit is cleared to '0', then received data bytes may have bit 1 (where bit 0 is the Least Significant bit) improperly received as a '0'.

Work around

Set both master and slave CKE bits to '1'.

Affected Silicon Revisions

C0	C1						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41637**C**):

> **Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (03/2013)

Initial release of this document.

Rev B Document (07/2013)

Added Module 5; Added Silicon Revision C1; Other minor corrections.

Rev C Document (10/2014)

Added Module 6.

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