MiniPOD™
AFBR-811vx3Z, AFBR-821vx3Z

10 Gbps/Channel, 300m link
Twelve Channel, Parallel Fiber Optics Modules

Avago TECHNOLOGIES

Data Sheet
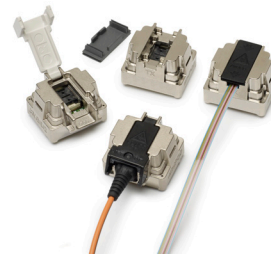
Description

The AFBR-811vx3Z Twelve Channel, Pluggable, Parallel Fiber Optics Transmitter and AFBR-821vx3Z Twelve Channel, Pluggable, Parallel Fiber Optics Receiver are high performance fiber optics modules for short-range parallel multi-lane data communication and interconnect applications. The high density optical modules are designed to operate over multimode fiber systems using a nominal wavelength of 850 nm. These MiniPODs can support 300m10GBASE-SR with Avago SFP+ transceivers over OM3 fiber.

Avago's MiniPOD solution offers system designers two module package options to optimize their cable management and board layout. AFBR-811Rx3Z (Tx)/AFBR-821Rx3Z (Rx) are used with round multi-lane cable assemblies for applications requiring multiple turns of the jumper cable inside the chassis. AFBR-811Fx3Z (Tx)/AFBR-821Fx3Z (Rx) are used with flat ribbon cable assemblies, allowing dense tiling of the modules as the jumper cables can be thread under the dust-cap of the next module. This top mounted optical connection maximizes board layout density by eliminating board space lost to the optical connector and strain relief.

The electrical interface uses a 9×9 MEG-Array connector with 1.27 mm pitch (http://portal.fciconnect.com/Comergent//fci/drawing/55714.pdf)

The optical interface requires the user to provide a custom designed optical turn 1×12 ribbon cable PRIZM® LightTurn® connector.

The thermal interface provided can require either a user provided heat sink or use of the Avago general purpose clip on heat sink, to maintain the module case temperature to be between 0 °C to 70 °C during continuous operation.

Applications

- 100GbE, 10GbE, and IB-QDR / IB-DDR / IB-SDR interconnects
- Data Aggregation, Backplane and Proprietary Protocol and Density Applications
- High Performance and High Productivity computer interconnects
- Switch Fabric interconnects

Patent - www.avagotech.com/patents

Features

- Compliant to IEEE 802.3ba 100GbE (100GBASE-SR10 and nPPI) per lane, and compatible with 10GBASE-SR
- Compliant to 12×QDR Infiniband
- Operates at 10.3125 Gbps per channel with 64b/66b encoded data for 100GbE application and with 8b/10b for 10GbE applications. Supports 10 Gbps with 8b/10b for IB-QDR applications.
- High Aggregate bandwidth: 120 Gbps per module
- High density footprint: 21.95 mm × 18.62 mm size
- Two package options to optimize internal cable management and system layout
- Separate transmitter and receiver modules
- 850 nm VCSEL array in transmitter; PIN array in receiver
- 10.3125 Gbps links up to 300 m & 400 m with OM3 & OM4 50 μm MMF, respectively
- Optical Interface: PRIZM™ LightTurn® optical turn 1×12 ribbon fiber connector
- Pluggable electrical interface: 9×9 MEG-Array for ease of design and manufacturability
- Low Power consumption: 3.0 W Max per Transmitter/Receiver pair (0 °C to 70 °C operating range)
- Dedicated signals for module address, module reset and host interrupt
- Two Wire Serial (TWS) interface with maskable interrupt for expanded functionality including:
  - Individual channel functions: disable, squelch disable, lane polarity inversion, TX eye margin enable
  - A/D read back: module temperature and supply voltages, per channel laser current and laser power, or received power
  - Status: per channel Tx fault, electrical (transmitter) or optical (receiver) LOS, and alarm flags
  - Programmable equalization integrated with DC blocking caps at transmitter data input
  - Programmable receiver output swing and de-emphasis level
  - Field Upgradable Firmware capability
- 0 °C to 70 °C case temperature continuous operating range. 85 °C supported for short durations

Part Number Ordering Options

Modules for use with Flat Ribbon Jumper Cable	Transmitter Base Part Number	AFBR-811Fx3Z
	Receiver Base Part Number	AFBR-821Fx3Z
Modules for use with Round Jumper Cable	Transmitter Base Part Number	AFBR-811Rx3Z
	Receiver Base Part Number	AFBR-821Rx3Z
MiniPOD Evaluation Board		AFBR-800EVB
MiniPOD Evaluation Kit		AFBR-800EVK
MiniPOD Round Module Dust Cover Opening Tool		AFBR-800RTL
MiniPOD Extraction Tool		AFBR-800ETL
MiniPOD PRIZM® LightTurn® Removal Tool		AFBR-800FTL

Where:

81 = Transmitter; 82 = Receiver

1: 10.3 Gbps

F/R: R = module package for use with round cable;
F = module package for use with Flat ribbon cable

x: N = No Heat Sink,
H = Pin Clip-on Heat Sink attached (see Figure 24)

Warning

INVISIBLE LASER RADIATION
AVOID DIRECT EYE EXPOSURE
CLASS 3R LASER PRODUCT
Wavelength: 850nm
Max Power: 31mW CW

INVISIBLE LASER RADIATION
AVOID DIRECT EYE EXPOSURE
CLASS 3R LASER PRODUCT

EN 60825-1:2007
COMPLIES WITH 21 CPR 1040.10 AND 1040.11
EXCEPT FOR DEVIATIONS PERSUANT TO LASER
NOTICE NO. 50, DATED JUNE 24, 2007

CLASS 1 LASER PRODUCT

CAUTION! Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure

CAUTION! Laser Class 3R for laser module assembly without fiber optic cable attachment.

INVISIBLE LASER RADIATION, AVOID DIRECT EYE EXPO-SURE! CLASS 3R LASER PRODUCT WITHOUT OPTIC CABLE ASSEMBLY

CAUTION! Laser Class 1 Classification for laser module assembly including fiber optic cable attachment. Safe to view laser output with the naked eye or with the aid of typical magnifying optics (e.g. telescope or microscope)

INVISIBLE LASER RADIATION, DO NOT VIEW DIRECTLY WITH OPTICAL IN-STRUMENTS. CLASS 1 LASER PRODUCT WITH OPTIC CABLE ASSEMBLY.

Note: Standard used for classification: EN 60825-1:2007

Avago Technologies Confidential. Restricted under NDA

Transmitter Module

The optical transmitter module (see Figure 1) incorporates a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 12-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. The transmitter is designed for EN-60825 and CDRH eye safety compliance; Class 3R out of the module. When fully assembled with the PRIZM LightTurn optical connector class 1M is achieved. The Tx Input Buffer provides CML compatible differential inputs (presenting a nominal differential input impedance of 100 Ω and a nominal common mode impedance to signal ground of 25 Ω) for the high speed electrical interface that can operate over a wide common mode range without requiring external DC blocking capacitors. For module control and interrogation, the control interface incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for VCSEL bias, light output power (LOP), temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential inputs,

de-activate channels, place channels into margin mode (system level diagnostic mode where TX OMA is reduced by ~1dB), disable the squelch function and program input equalization levels to reduce the effect of long PCB traces. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register. The optical output will squelch for loss of input signal unless squelch is disabled. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm and fault information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm, LOS and/or Tx fault.
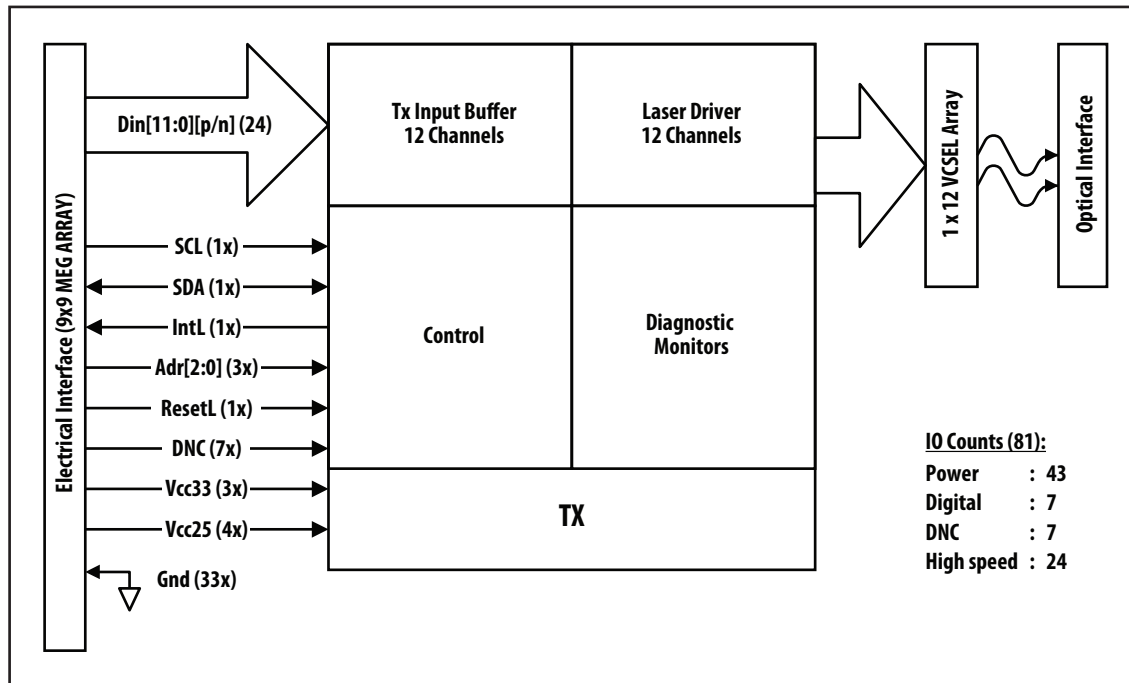

Figure 1. Transmitter Block Diagram

Avago Technologies Confidential. Restricted under NDA

Receiver Module

The optical receiver module (see Figure 2) incorporates a 12-channel PIN photodiode array, a 12-channel pre-amplifier and output buffer, diagnostic monitors, control and bias blocks. The Rx Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ω to AC ground and 100 Ω differentially that should be differentially terminated with 100 Ω. External DC blocking capacitors are required. For module control and interrogation, the control interface incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for optical input power, temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential outputs, de-activate channels, disable the squelch function, program output signal amplitude and de-emphasis and change receiver bandwidth. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. Status and alarm information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm and/or LOS.
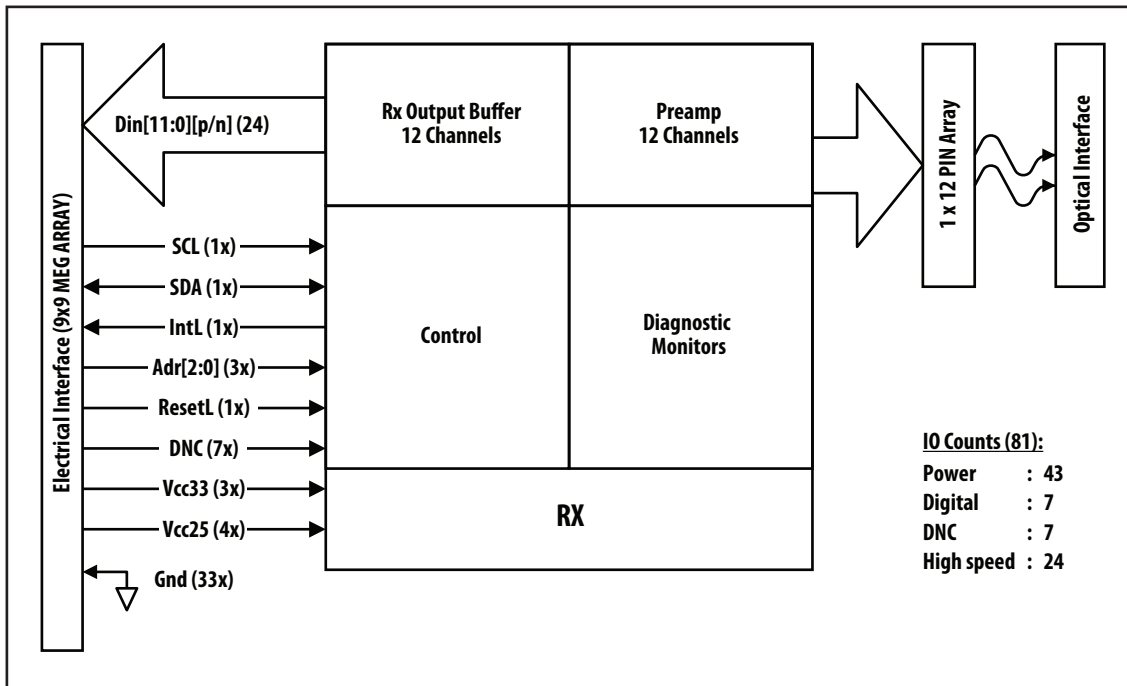

Figure 2. Receiver Block Diagram

High Speed Signal Interface

Figure 3 shows the interface between an ASIC/SerDes and the fiber optics modules. For simplicity, only one channel is shown. As shown in Figure 3, the compliance points are on the host board side of the electrical connectors. Sets of s-parameters are defined for the transmitter and receiver interfaces. The transmitter and receiver are designed, when operating within Recommended Operating Conditions, to provide a robust eye-opening at the receiver outputs. See the Recommended Operating Conditions and the Receiver Electrical Characteristics for details.

Unused inputs and outputs should be terminated with 100 Ω differential loads.

The transmitter inputs support a wide common mode range and DC blocking capacitors are not needed (internal capacitors are not shown in Figure 3). Depending on the common mode range tolerance of the ASIC/SerDes inputs, DC blocking capacitors may be required in series with the receiver; in this case 100 nF capacitors are recommended. Differential impedances are nominally 100 Ω. The common mode output impedance for the receiver is nominally 25 Ω while the nominal common mode input impedance of the transmitter is 25 Ω.

Transmitter Input Equalization

Transmitter inputs can be programmed for one of several levels of equalization. See Figure 4. The default case provides a flat gain-frequency response in the inputs. Different levels of compensation can be selected to equalize skin-effect losses across the host circuit board. See Tx Memory Map 01h Upper Page section addresses 228 – 233 for programming details.

Receiver Output Amplitude and De-emphasis

Receiver outputs can be programmed to provide several levels of amplitude and de-emphasis. See Figure 5 for de-emphasis definition. The user can program for peak-to-peak amplitude and then a de-emphasis level. If zero de-emphasis is selected, then the signal steady state equals the peak-to-peak level. For other levels of de-emphasis the selected de-emphasis reduces the steady-state from the peak-to-peak level. The change from peak-to-peak level to steady-state occurs within a bit time. See Rx Memory Map 01h Upper Page section addresses 228 – 233 for amplitude programming details and addresses 234 – 239 for de-emphasis programming details.
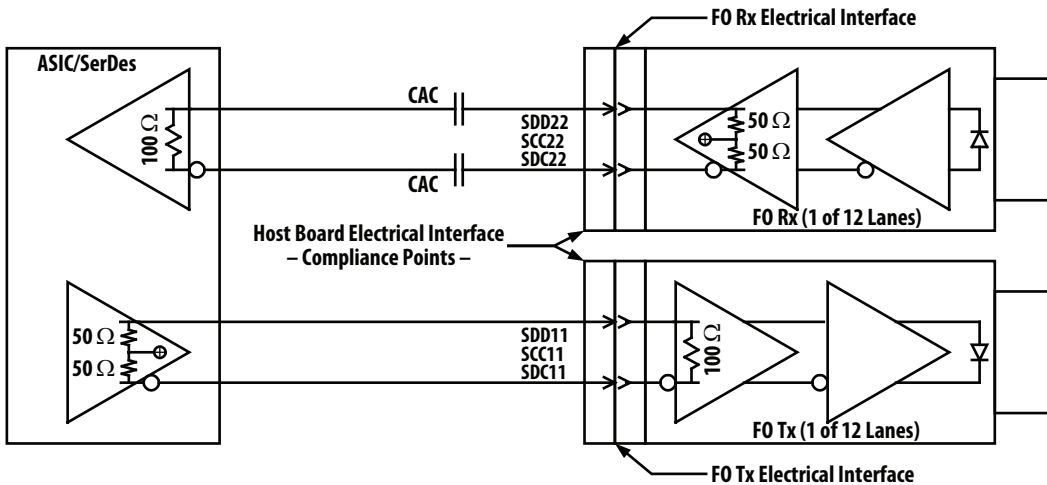
Figure 3. Application Reference Diagram
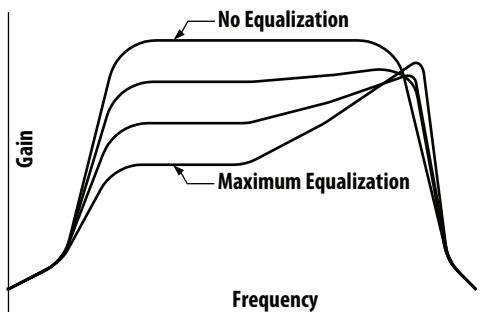
Figure 4. Transmitter Input Equalization

Avago Technologies Confidential. Restricted under NDA
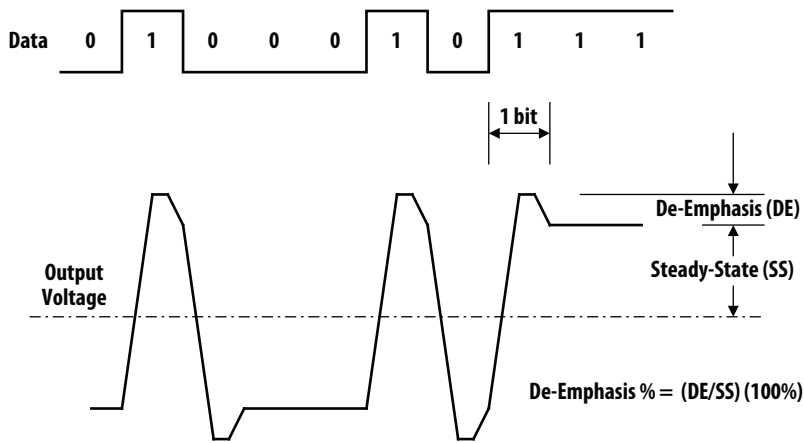
Figure 5. Definition of De-emphasis and Steady State

Control Signal Interface

The control interface includes dedicated signals for address inputs, interrupt output and reset input and bi-directional clock and data lines for a two-wire serial access (TWS interface) to control and status and information registers. The TWS interface is compatible with industry standard two-wire serial protocol. The MiniPOD module is implemented as a slave device. Signal and timing characteristics are further defined in the Control Characteristics and Control Interface and Memory Map sections.

The registers of the serial interface memory are defined in the Control Interface and Memory Map section.

Link Model and Reference Channel
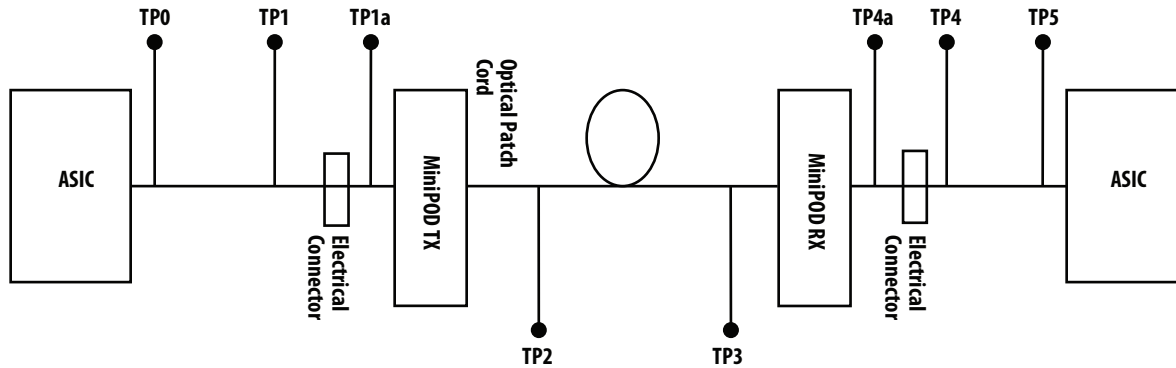
Figure 6. Link Model test point definitions

Performance specifications for the MiniPOD modules based on IEEE 802.3ba 100GBASE-SR10.

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operation Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_s	-40	85	°C	
Absolute Maximum Operating Temperature			85	°C	1
2.5 V Power Supply Voltage	V_{cc25}	-0.5	3.0	V	
3.3 V Power Supply Voltage	V_{cc33}	-0.5	4.0	V	
Data Input Voltage – Single Ended		-0.5	Vcc33+0.5, Vcc25+0.5, 4.0	V	
Data Input Voltage – Differential	$\|V_{Dip} - V_{Din}\|$		1.0	V	2
Control Input Voltage	V_i	-0.5	Vcc33+0.5, 4.0	V	3
Control Output Current	I_o	-20	20	mA	
Relative Humidity	RH	5	95	%	4
Receiver Damage Threshold	Rx_P_{MAX}		+4	dBm	

Notes:
1. Electro-optical specifications are not guaranteed outside the recommended operating temperature range. Operation above the Absolute Maximum Case Temperature for extended periods may adversely affect reliability.
2. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry.
3. The maximum limit is the lesser of V_{cc} + 0.5 V or 4.0 V.
4. Exposure to a condensing environment is not allowed.

Avago Technologies Confidential. Restricted under NDA

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Case Temperature	T_c	0		70	°C	Note 1
Case Temperature (short term)	T_{c_ext}	70		85	°C	Note 2
2.5 V Power Supply Voltage	V_{cc25}	2.375	2.5	2.625	V	Note 3
3.3 V Power Supply Voltage	V_{cc33}	3.135	3.3	3.465	V	
Signal Rate per Channel (rates < 3.125 Gb/s must be 8b/10b encoded)		1.25		10.3125	GBd	Note 4
Host Electrical Compliance			Per IEEE 802.3ba-2010 TP1a and TP4 nPPI specifications for host			
Control Input Voltage High	V_{ih}	2.3		3.6	V	
Control Input Voltage Low	V_{il}	-0.3		0.4	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Two Wire Serial Interface Write Cycle Time (up to 2 sequential bytes)	t_{WC}	100			ms	
Reset Pulse Width	$t_{RSTL\ PW}$	10			μs	
Power Supply Noise				100	mVpp	Note 5, 500 Hz to 5.4 GHz
Receiver Differential Data Output Load			100		Ω	Figure 3
AC Coupling Capacitors – Receiver Data Outputs	C_{ac}		0.1		μF	Note 6, Figure 3
Fiber Length: 4700 MHz•km 50 μm MMF (OM4) 2000 MHz•km 50 μm MMF (OM3)		0.5 0.5		400 300	m m	Note 7
Module Retention Screw Torque				0.06	N.m	Note 8
Module Top Surface Load Limit				100	N	Note 9
MEG-Array Mating Force (required)				70	N	
MEG-Array de-Mating Force (required)				35	N	
MEG-Array Side Load				50	N	See Figure 28
Fiber Pull Force (long duration**)				0.98	N	See Figure 29
Fiber Pull Force (short duration*)				2.2	N	See Figure 29
PRIZM Insertion Force (short duration*)				40	N	Note 10, See Figure 30
Number of Ribbons (Flat Cable Housing)				3		Note 11

Notes:

1. To prevent a degradation in reliability, avoid continuous operation above 70 °C. The case temperature is referenced to the Thermocouple measurement point, as shown in Figure 20; it is the same location for Tx and Rx, flat and round cable housing.
2. Short term is defined per section 4.1.2 of Telcordia GR-63-CORE Issue 3, March 2006 and corresponds to a period of not more than 96 consecutive hours and a total of not more than 15 days in 1 year (This refers to a total of 360 hours in any given year, but no more than 15 occurrences during that 1-year period).
3. There are no restrictions to the 2.5 V and 3.3 V power supply sequencing.
4. Higher data rates are possible. For further details, contact your Avago sales representative.
5. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 8 for recommended power supply filters.
6. For data pattern with restricted run lengths and disparity, e.g. 8b10b, smaller value capacitors may provide acceptable results.
7. Channel insertion loss includes 3.5 dB/km attenuation, 1.5 dB connector loss and 0.3 dB modal noise penalty allocations.
8. The PCB material should be evaluated to ensure that damage does not occur.
9. Load applied perpendicular to the module heat sink interface surface. See Figure 27.
10. Refer to the "PRIZM® LightTurn® Connector – to – Mini-POD™ Parallel Optic Module Assembly Recommendations" procedure available from Avago sales. 40 N max applies only when the PRIZM connector is being inserted/attached, per the PRIZM Connector Assembly Instructions. For all other objects being inserted inside the MiniPOD module, (i.e., not the PRIZM optical connector), the max force is 10 N. The 40 N can only be applied by a human finger tip. No tools or thumbs are to be used in the PRIZM connector attach process.
11. This is the number of ribbon fibers that can be accommodated beneath the dust-cap of a flat cable housing MiniPOD. Hence the maximum number of MiniPODs that can be tiled in a row is 3.
* Short duration is < 15 seconds.
** Long duration (> 5 minutes), exceeding this force long term could cause the optical light output power to drop or Rx sensitivity to diminish, which is not recoverable.

Avago Technologies Confidential. Restricted under NDA

Transmitter Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V.

Parameter	Symbols	Min	Typ	Max	Units	Reference
Power Consumption (Max EQ)			1.2	1.6	W	Note 1
Power Supply Current – V_{cc25}			280	365	mA	Note 2
Power Supply Current – V_{cc33}			105	185	mA	Note 3
Differential Input Impedance		85	100	115	Ω	Informative
LOS Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\,PP\,LOS}$	50			mVpp	Informative
LOS De-Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\,PP\,LOS}$			210	mVpp	Note 4, Informative
LOS Hysteresis		0.5		4	dB	
Power On Initialization Time	$t_{PWR\,INIT}$		350	2000	ms	Note 5

Parameter	Test Point	Min	Typ	Max	Units	Reference
Single ended input voltage tolerance	TP1a	-0.3		4.0	V	Note 6
AC common mode input voltage tolerance	TP1a	15			mV	RMS
Differential input return loss	TP1				dB	Note 7, 10 MHz to 11.1 GHz
Differential to common-mode						
input return loss	TP1	10			dB	10 MHz to 11.1 GHz
J2 Jitter tolerance	TP1a	0.17			UI	Defined in 802.3ba
J9 Jitter tolerance	TP1a	0.29			UI	Defined in 802.3ba
Data Dependent Pulse Width Shrinkage (DDPWS) tolerance	TP1a	0.07			UI	Defined in 802.3ba
Eye Mask Coordinates: X1, X2, Y1, Y2	TP1a	SPECIFICATION VALUES 0.11, 0.31, 95, 350			UI mV	Note 8, Hit Ratio = 5x10⁻⁵

* For control signal timing including Adr[2:0], IntL, ResetL, SCL and SDA see Control Characteristics: Transmitter/Receiver.

Notes:
1. Max power is 1.7 W above 70 °C, to 85 °C case temperature.
2. Supply current includes that of all V_{cc25} contacts.
3. Supply current includes that of all V_{cc33} contacts. Max current is 210 mA above 70 °C, to 85 °C case temperature.
4. Tx data input must conform to IEEE 802.3ba-2010 TP1a electrical host compliance specification.
5. Power On Initialization Time is the time from when the supply voltages reach and remain above the minimum Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.
6. Referred to TP1 signal common; The single-ended input voltage tolerance is the allowable range of the instantaneous input signals.
7. From 10 MHz to 11.1 GHz, the magnitude in decibels of the module differential input return loss at TP1 and the host differential output return loss at TP1a shall not exceed the limit given in Equation

Return_loss (f) $\geq 12 - 2\sqrt{(f)}$ $0.01 \leq f < 4.1$ dB
$\geq 6.3 - 13\log10(f/5.5)$ $4.11 \leq f < 11.1$ dB

Return_loss (f) is the return loss at frequency f
f is the frequency in GHz

8.
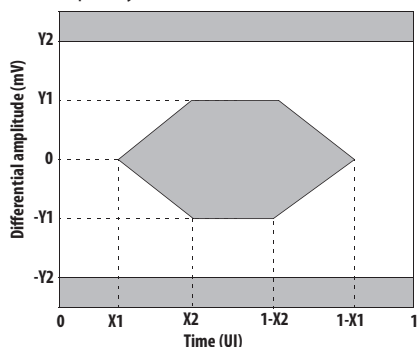
Tx Electrical Eye Mask Coordinates (TP1a) at Hit ratio 5 x 10⁻⁵ hits per sample

Avago Technologies Confidential. Restricted under NDA

Receiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V.

Parameter	Test Point	Min	Typ	Max	Units	Reference
Power Consumption			1.1	1.4	W	Note 1
Power Supply Current (V_{cc25}) – @ Default De-emphasis / Default output swing			350	425	mA	Note 2
Power Supply Current (V_{cc33}) – @ Default De-emphasis / Default output swing			48	90	mA	Note 3
Power Supply Current (V_{cc25}) – @ Max De-emphasis/Max output swing			430	525	mA	Note 2
Power Supply Current (V_{cc33}) – @ Max De-emphasis/Max output swing			48	90	mA	Note 3
Data Output Differential Peak-to-Peak Voltage Swing (Default De-emphasis)	TP4	400	500	600	mVpp	Note 4, 100 Ω Load (default setting)
Data Output Common Mode Voltage	TP4	2.0		2.540	V	Over Amplitude Range
AC common-mode output voltage (RMS)	TP4			7.5	mV	
Termination mismatch at 1 MHz	TP4			5	%	
Differential Output Impedance	TP4	85		115	Ω	Informative
Differential Output Return Loss, 10M – 11.1 GHz	TP4				dB	Note 5
CM to Differential Mode Conversion, 0.1G –11.1 GHz	TP4				dB	Note 6
Power On Initialization Time			288	2000	ms	
Output transition time (20% to 80%)	TP4	28			ps	
J2 Jitter Output	TP4			0.42	UI	Defined in 802.3ba
J9 Jitter Output	TP4			0.65	UI	Defined in 802.3ba
Data Dependent Pulse Width Shrinkage	TP4			0.34	UI	Defined in 802.3ba
Inter-channel Skew	TP4			11	ns	
Inter-channel Skew Variation	TP4		100		ps	Note 7
Eye Mask Coordinates: X1, X2, Y1, Y2	TP4		SPECIFICATION VALUES 0.29, 0.5, 150, 425		UI mV	Note 8, Hit Ratio = 5x10^{-5}

Notes:
1. Max conditions include default output amplitude and de-emphasis programming.
2. Supply current includes that of all Vcc25 contacts.
3. Supply current includes that of all Vcc33 contacts.
4. See section on page 61 "Receiver Output Amplitude Control Code Description" for range of voltages defined in the receiver upper page 01h, address range 228 to 233. Data outputs are CML compatible. Data Output Differential Peak to Peak Voltage Swing is defined as follows: $\Delta V_{DO\,pp}$ = ΔV_{DOH} − ΔV_{DOL} where ΔV_{DOH} = High State Differential Data Output Voltage and ΔV_{DOL} = Low State Differential Data Output Voltage. Output voltage swing is adjustable via TWS interface.
5. From 10 MHz to 11.1 GHz. The magnitude in decibels of the module differential output return loss at TP4 and the host differential input return loss at TP4a shall not exceed the limit given in Equation
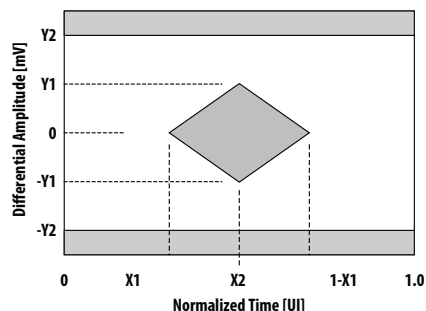   Return_loss (f) $\geq 12 - 2\sqrt{(f)}$ $0.01 \leq f < 4.1$ dB
                         $\geq 6.3 - 13\log10(f/5.5)$ $4.11 \leq f < 11.1$ dB
6. From 10 MHz to 11.1 GHz. The magnitude in decibels of the host common mode output return loss at TP4 shall not exceed the limit given in Equation:
   Return_loss (f) $\geq 7 - 1.6f$ $0.01 \leq f < 2.5$ dB
                         ≥ 3 $2.5 \leq f < 11.1$ dB
   f is the frequency in GHz.
7. Inter-Channel Skew is defined for the condition of equal amplitude, zero ps skew input signals at TP1a.
8.

Rx Electrical Eye Mask Coordinates (TP4) at Hit ratio 5 x 10^{-5} hits per sample

Avago Technologies Confidential. Restricted under NDA

Transmitter Optical Characteristics [1]

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_C = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V. Test point = TP2. Note: The TX output performance is only guaranteed with a differential input that meets the recommended operating conditions. A link driven with a single-ended signal will degrade the jitter performance.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Center Wavelength	λ_C	840	850	860	nm	
RMS spectral width			0.35	0.65	nm	2
Average launch Power, each lane	$P_{O\ AVE}$	-7.6		2.4	dBm	
Output Optical Power: Disabled	$P_{O\ OFF}$			-30	dBm	
Extinction Ratio	ER	3			dB	
Optical Modulation Amplitude, each lane	OMA	-4.3		2.4	dBm	3
Output Power (Squelched OMA)			-2.4		dBm	AC Squelch
Tx Mask Margin	Tx_MM	10%				
Difference in launch power between any two lanes (OMA)				4	dB	
Peak power, each lane				4	dBm	
Launch Power in OMA minus TDP, each lane	Po - TDP	-6.5			dBm	
Transmitter and Dispersion Penalty, each lane	TDP			3.5	dB	
Optical return loss tolerance				12	dB	
Encircled flux			≥ 86% at 19 μm, ≤ 30% at 4.5 μm			
Specification Values						
Eye mask coordinates: X1, X2, X3 Y1, Y2, Y3			0.23, 0.34, 0.43 0.27, 0.35, 0.4		UI	4, Hit ratio = 5×10^{-5} per sample
Power On Initialization Time Tx Outputs	$t_{PWR\ INIT}$		350	2000	ms	
Reset De-assert Re-initialization Time Tx Outputs	$t_{RSTL\ OFF}$		350	2000	ms	
Output Disable Assert Time for Fault	$t_{DIS\ ON}$		9	100	ms	
Output Squelch Assert Time for LOS	$t_{SQ\ ON}$		52	80	μs	
Output Squelch De-assert Time for LOS	$t_{SQ\ OFF}$		49	80	μs	

Notes:
1. These optical specifications are dependent upon the performance of the PRIZM LightTurn to cable assembly, which assumes a maximum of 2 dB insertion loss. More details are provided on the PRIZM LightTurn cable assembly specification. Please contact your Avago sales representative to receive this specification.
2. RMS spectral width is the standard deviation of the spectrum.
3. Output of user provided fiber connector. Even if the TDP < 0.9 dB, the OMA minimum must exceed this minimum value. Power exceeds IEEE802.3ae but Avago SFP+ transceivers are compatible with this higher receiver input power. Note the possibility of high optical power DMI alarms on SFP+ Receivers
4. Compliance assured up to 10.3125 Gbps.

Transmitter eye mask definitions (TP2) at Hit ratio 5 x 10^-5 hits per sample

Avago Technologies Confidential. Restricted under NDA
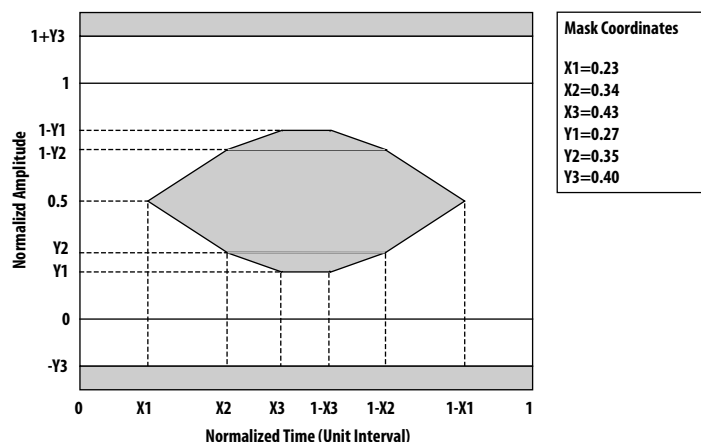
Receiver Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions from 0 °C to 70 °C, unless otherwise noted. Typical values are for T_c = 40 °C, V_{cc33} = 3.3 V and V_{cc25} = 2.5 V.

Parameter	Test Point	Min	Typ	Max	Units	Reference
Optical Modulation Amplitude (OMA), each lane	TP3			+3	dBm	1
Stressed Sensitivity (OMA), each lane	TP3			-5.4	dBm	2
Receiver Sensitivity (OMA)	TP3	-12			dBm	Informative
Operating Center Wavelength	TP3	840		860	nm	
Receiver Reflectance	TP3			-12	dB	
Peak Power, each lane	TP3			+4	dBm	
Output Rise/Fall time (20-80%)	TP3	25	40	50	ps	3
LOS to Data Output Squelch Assert Time	TP3		50	300	µs	4
Data Output Squelch De-assert Time	TP3		120	300	µs	5
LOS ASSERT Threshold (OMA)	TP3	-30	-14		dBm	
LOS De-ASSERT Threshold (OMA)	TP3		-12.4	-8	dBm	
LOS Hysteresis	TP3	0.5	1.6		dB	

Notes:
1. These optical specifications are dependent upon the performance of the PRIZM LIghtTurn cable assembly, which assumes a maximum of 2 dB insertion loss. More details are provided on the PRIZM LightTurn cable assembly specification. Please contact your Avago sales representative to receive this specification.
2. Measured with conformance test signal at TP3 for BER = 10e-12.
3. These are unfiltered rise and fall times without de-emphasis measured between the 20% and 80% levels using a 500 MHz square wave test pattern. Impairments in measurements due to the test system are removed. Specifications are for information only.
4. This is the module response time from fall of Rx input to less than Rx input LOS threshold to squelch of Rx outputs.
5. This is the module response time from rise of Rx input to greater than Rx input LOS threshold to resumption of Rx outputs.

Avago Technologies Confidential. Restricted under NDA

100GBASE-SR10 Illustrative Link Power Budgets

Parameter	OM3	OM4	Units	Reference
Effective Modal Bandwidth at 850 nm	2000	4700	MHz•km	
Launch Power in OMA minus TDP, each lane	-6.5		dBm	
Transmitter and Dispersion Penalty, each lane	3.5		dB	
Receiver Sensitivity (OMA)	-11.3		dBm	
Power Budget (for maximum TDP)	8.3		dB	
Operating Distance	0.5 to 100	0.5 to 150	m	
Channel Insertion Loss	1.9	1.5	dB	
Allocation for Penalties (for max. TDP)	6.4	6.5	dB	
Unallocated Margin	0	0.3	dB	
Additional Insertion Loss Allowed		0	dB	

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	Transmitter and Receiver modules withstand minimum 1000 V on all pins.
	JEDEC Machine Model (MM) (JESD22-A115-A)	Transmitter and Receiver modules withstand minimum 50 V on all pins.
Immunity	Variation of EN 61000-4-3	Typically minimum effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing	EN 60825-1:2007 CFR21 section 1040	P_{out}: IEC AEL and US FDA CDRH Class 3R* without optical connector, Class 1 with optical connector. CDRH Accession Number: 1020008-001 TUV Certificate Number: R72131700
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File Number: E173874
RoHS Compliance (RoHS Directive 2002/95/EC issued January 27, 2003)	BS EN 1122:2001 Mtd B by ICP for Cadmium, EPA Method 3051A by ICP for Lead and Mercury, EPA Method 3060A and 7196A by UV/Vis Spectrophotometry for Hexavalent Chromium. EPA Method 3540C/3550B by GC/MS for PPB and PBDE BS EN method by ICP and EPA methods by ICP, UV/Vis Spectrophotometry and GC/MS.	Less than 100 ppm of cadmium, Less than 1000 ppm lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl esters.

Transmitter / Receiver Module Contact Assignment and Signal Description

Optical Fiber Exit Side

	1	2	3	4	5	6	7	8	9
A	GND	D2+	GND	D4+	GND	D6+	GND	D8+	GND
B	GND	D2−	GND	D4−	GND	D6−	GND	D8−	GND
C	GND	GND	ADR<2>	Vcc33	Vcc33	Vcc33	DNC	GND	GND
D	D0+	D0−	GND	SDA	DNC	INTL	GND	D10−	D10+
E	GND	GND	ADR<1>	RESET	DNC	SCL	DNC	GND	GND
F	D1+	D1−	GND	Vcc25	DNC	DNC	GND	D11−	D11+
G	GND	GND	ADR<0>	Vcc25	Vcc25	Vcc25	DNC	GND	GND
H	GND	D3−	GND	D5−	GND	D7−	GND	D9−	GND
J	GND	D3+	GND	D5+	GND	D7+	GND	D9+	GND

TX/RX Host Board Pattern – TOP VIEW

Figure 7. TX / RX Host Board Pattern

Signal Name	Signal Description	I/O	Type
Adr[2:0]	TWS Module Bus Address bits: Address has the form 0101hjkx where Adr2, Adr1 and Adr0 correspond to h, j and k respectively and x corresponds to the R/W command.	I	3.3 V LVTTL
D[11:0]p	Module Data Non-inverting Input / Output for channels 11 through 0	I	CML
D[11:0]n	Module Data Inverting Input/ Output for channels 11 through 0	I	CML
DNC	Reserved – Do Not Connect to any electrical potential on Host PCB		
GND	Signal Common: All module voltages are referenced to this potential unless otherwise stated. Connect these pins directly to the host board signal ground plane.		
IntL	Interrupt signal to Host, Asserted Low: An interrupt is generated in response to any Fault condition, loss of input signal or assertion of any monitor Flag. It may be programmed through the TWS interface to generate either a pulse or static level with static mode as default. This output presents a High-Z condition when IntL is de-asserted and requires a pull-up on the Host board. Pull-up to the Host 3.3 V supply is required.	O	3.3 V LVTTL, high-Z or driven to 0 level
ResetL	Reset signal to module, Asserted Low: When asserted the optical outputs are disabled, TWS interface commands are inhibited, and the module returns to default and non-volatile settings. An internal pull-up biases the input High if the input is open.	I	3.3 V LVTTL
SDA	TWS interface data signal: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is required.	I/O	3.3 V LVTTL, high-Z or driven to 0 level
SCL	TWS interface clock signal l: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is required.	I	3.3 V LVTTL
V_{cc25}	2.5 V Power supply, External common connection of pins required – not common internally		
V_{cc33}	3.3 V Power supply, External common connection of pins required – not common internally		
Case Common	Not accessible in connector. Case common incorporates exposed conductive surfaces including threaded bosses and is electrically isolated from signal common, i.e. GND. Connect as appropriate for EMI shield integrity		

Recommended Power Supply Filtering

It is recommended to use separate power supply filters for V_{cc33} and V_{cc25} as in Figure 8. This filter is similar to other module specifications, such as SFF-8431 Rev 3.0 section D17 Figure 56.

Separate power supply filters shall be used for TX and RX modules.

The host power supply noise level compliance point is at point X.

The host power supply voltage level compliance point is at point Y, and host must take into account of the possible power supply drop due to the MEG-Array interface.
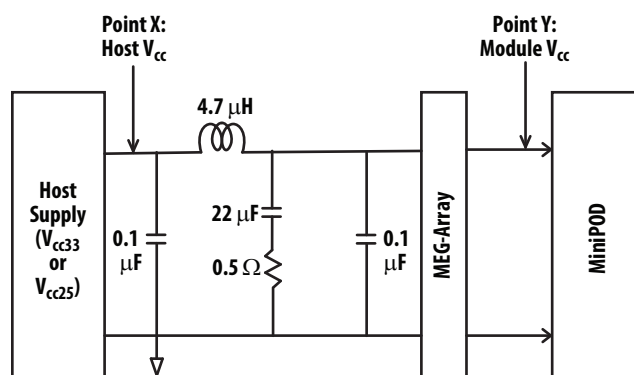

Figure 8. Recommended TX and RX Power Supply Filter

Power Supply Sequence

TX and RX Modules Power Supplies

There is no special requirement in the order of V_{cc33} and V_{cc25} power supply up/down sequence for TX or RX modules. However, it is recommended that

- Upon power down, the V_{cc33} and V_{cc25} shall be within 0 mV to +50 mV. If the residual voltage is larger than 50 mV, it can cause the TX or RX module to fail to start up.

Host ASIC Power Supplies

It is required that

- The maximum delay of power up/down between host ASIC and TX or RX module shall be shorter than 1 s to avoid any potential reliability damage to the modules.

It is recommended that: [1]

- The host ASIC power supply shall be turned on no later than TX or RX module power supplies (3.3 V and 2.5 V).
- The host ASIC power supply shall be turned off no earlier than module power supplies (3.3 V and 2.5 V).

If this condition cannot be met in the system design, the following shall be taken into account in the ASIC design. In the case when the RX module is powered on, host ASIC is power off, the host ASIC electrical input ESD diodes can be forward-biased through a 50 Ω resistor to the V_{cc25} supply (see Figure 10). The host ASIC ESD diodes shall be designed to tolerate such forward biasing.

High Speed and Low Speed IOs

The power supply sequence and the ramp rate shall be designed by the user to meet the absolute maximum specifications as in "Data Input Voltage – Single Ended" and "Control Input Voltage".

It is required that:

- Data signal shall NOT be presented at TX high speed inputs before both V_{cc33} and V_{cc25} are turned on for the TX module; and data signal shall be turned off at TX high speed inputs before both V_{cc33} and V_{cc25} are turned off for the TX module.

It is recommended that:

- The low speed inputs are pulled down when the TX and RX V_{cc33} or V_{cc25} are off.

Note:
1. In the case when host ASIC is turned on and the module power supply is off, the TX high speed input (if DC coupled to ASIC) and TX/RX low speed IO ESD diodes can be forward-biased by the ASIC. The following design shall take care of the potential latch up or reliability issues:
    - The TX high speed ESD diodes are designed to tolerate a minimum of 10 mA forward biasing current assuming ASIC is CML driver
    - The host system or ASIC low speed IO pull-ups shall be sufficient to limit the forward biasing current in the low speed IO ESD diodes.

Avago Technologies Confidential. Restricted under NDA

Figure 9. Transmitter Data Input Equivalent Circuit
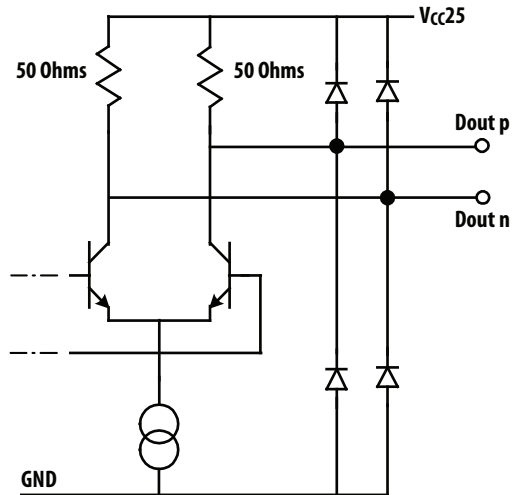
Figure 10. Receiver Data Output Equivalent Circuit
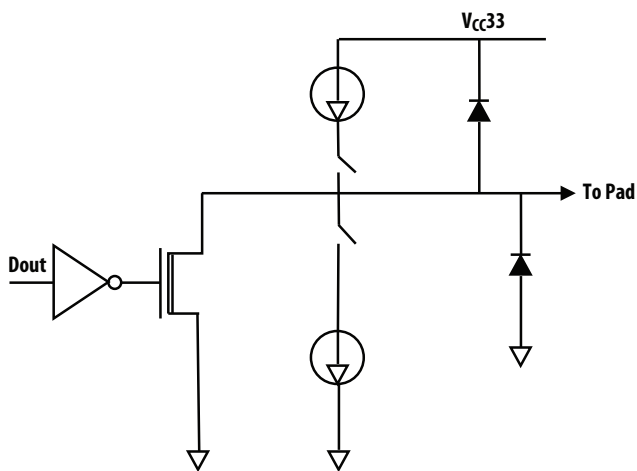
Figure 11. Low Speed IO Equivalent Circuit, INTL
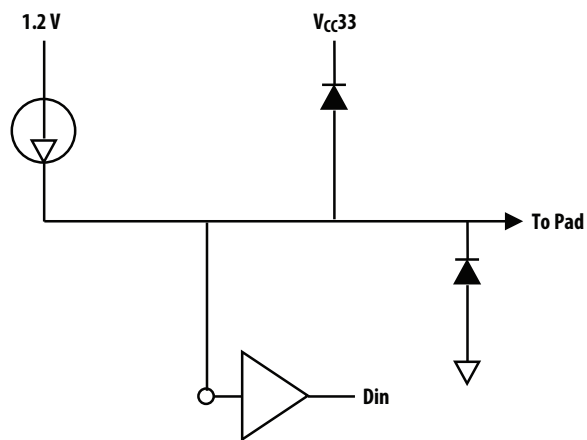
Figure 12. Low Speed IO Equivalent Circuit, RESETL
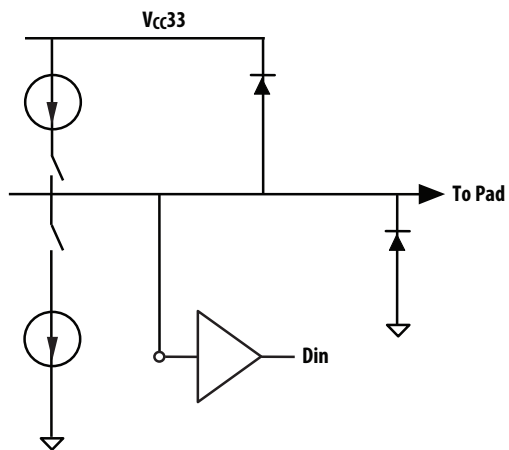
Figure 13. Low Speed IO Equivalent Circuit, ADR<2:0>
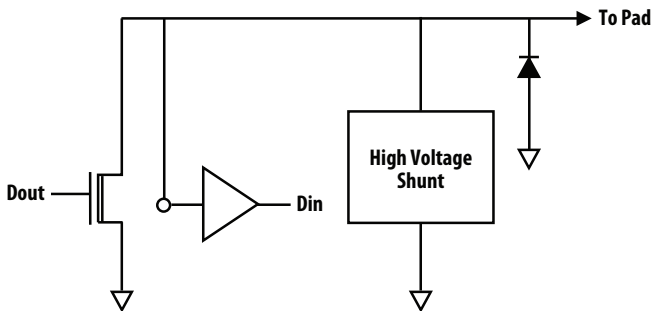
Figure 14. Low Speed IO Equivalent Circuit, SDA, SCL

Control Timing Diagrams
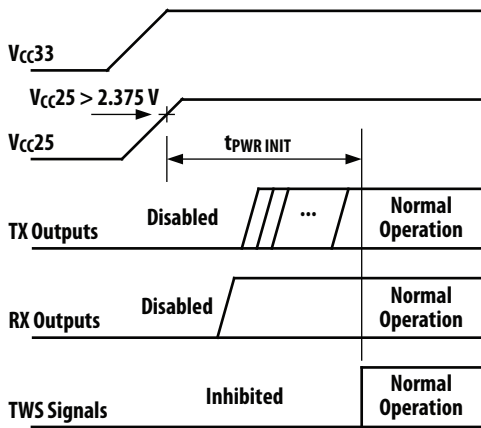
Figure 15. Power-Up Sequence
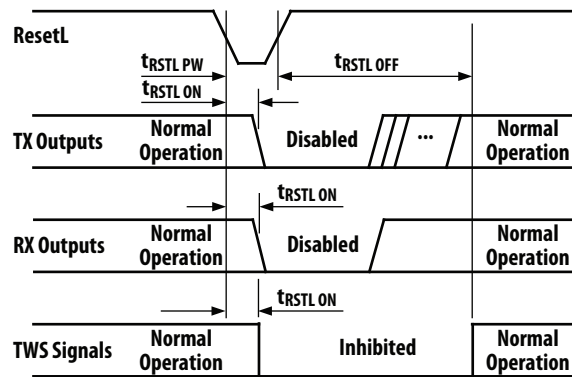
Figure 16. ResetL Sequence
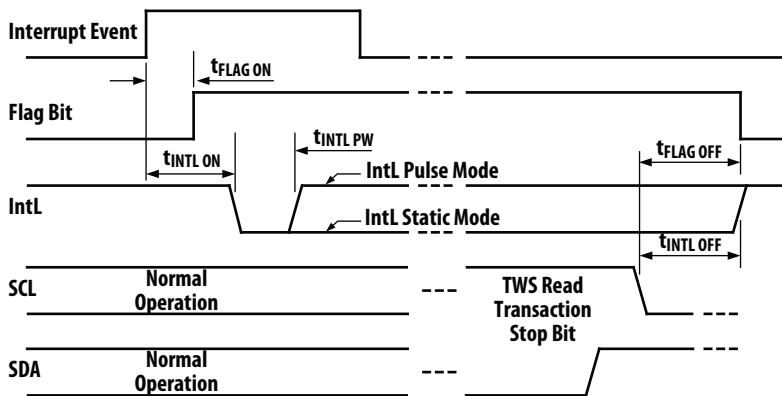
Figure 17. Interrupt Sequence
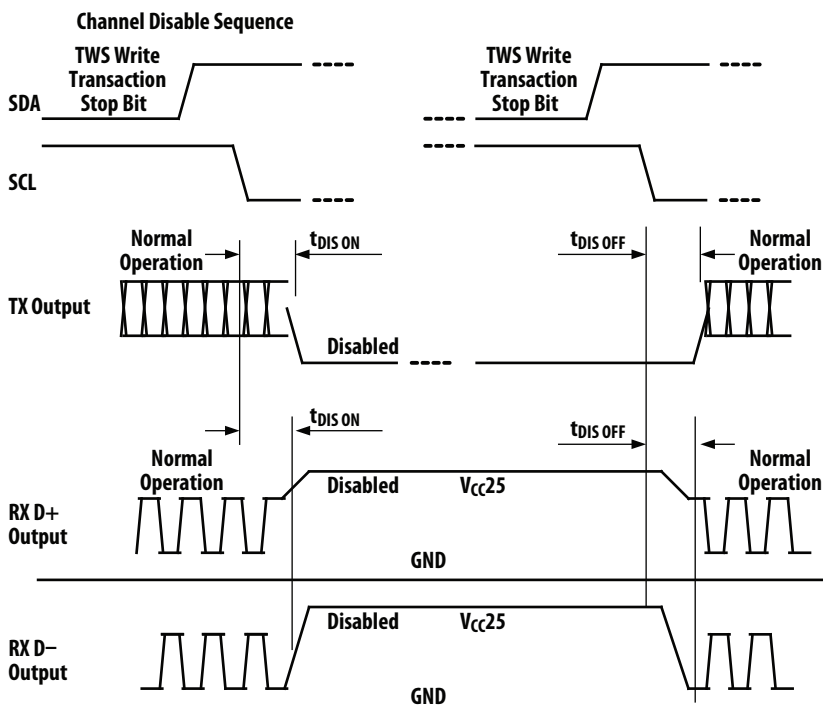
Figure 18. Channel Disable Sequence

Avago Technologies Confidential. Restricted under NDA

LOS Squelch Sequence
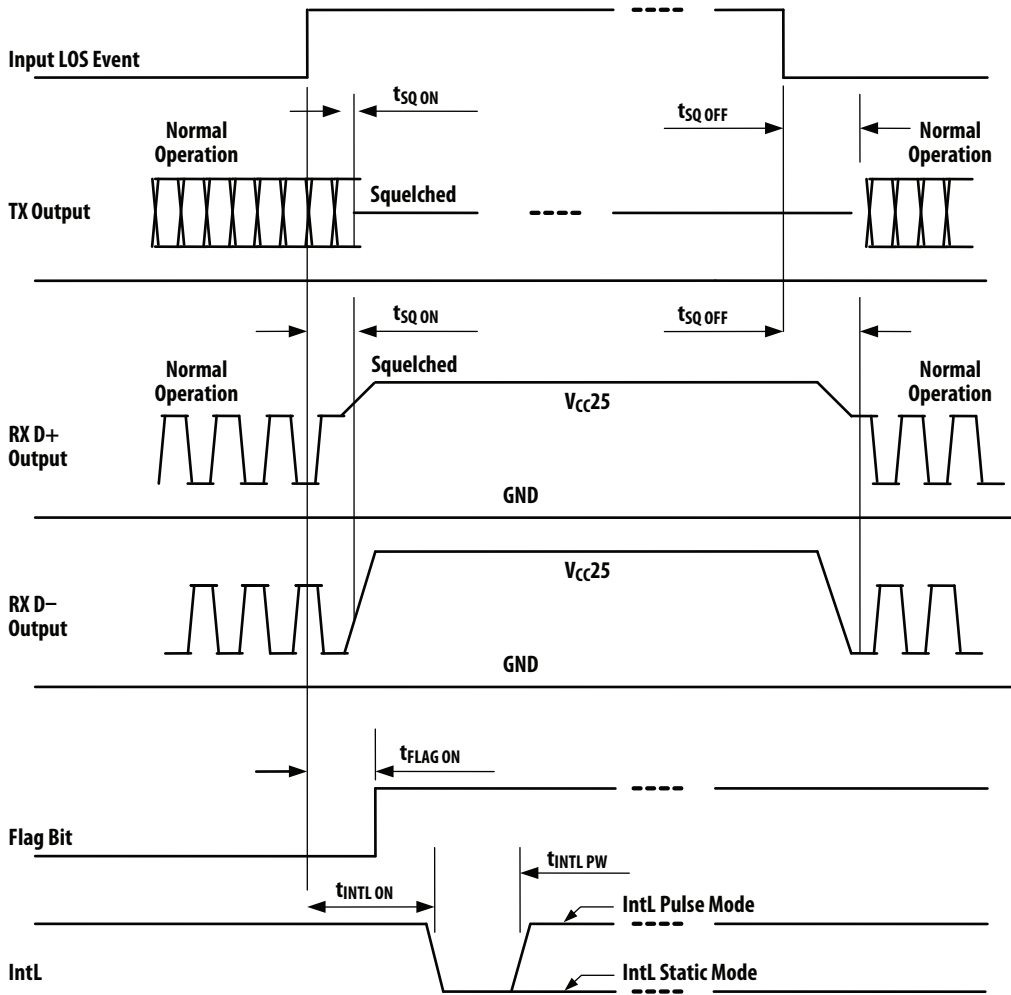
Figure 19. LOS Squelch Sequence

Avago Technologies Confidential. Restricted under NDA

Package Mechanical Outline – Flat Ribbon Cable Housing

HEAT SINK SURFACES
KEEP CLEAN
AVOID SCRATCHES
AVOID DENTS

(14.50)

FIBER EXIT SIDE
INDICATOR ON
BOTH SIDES

(18.82 WITH LABELS)

(18.62)

(21.95)

(4X R1.50)

THERMAL
COUPLE
POINT

4.00

9.35

Channel 0

FIBER
EXIT
SIDE
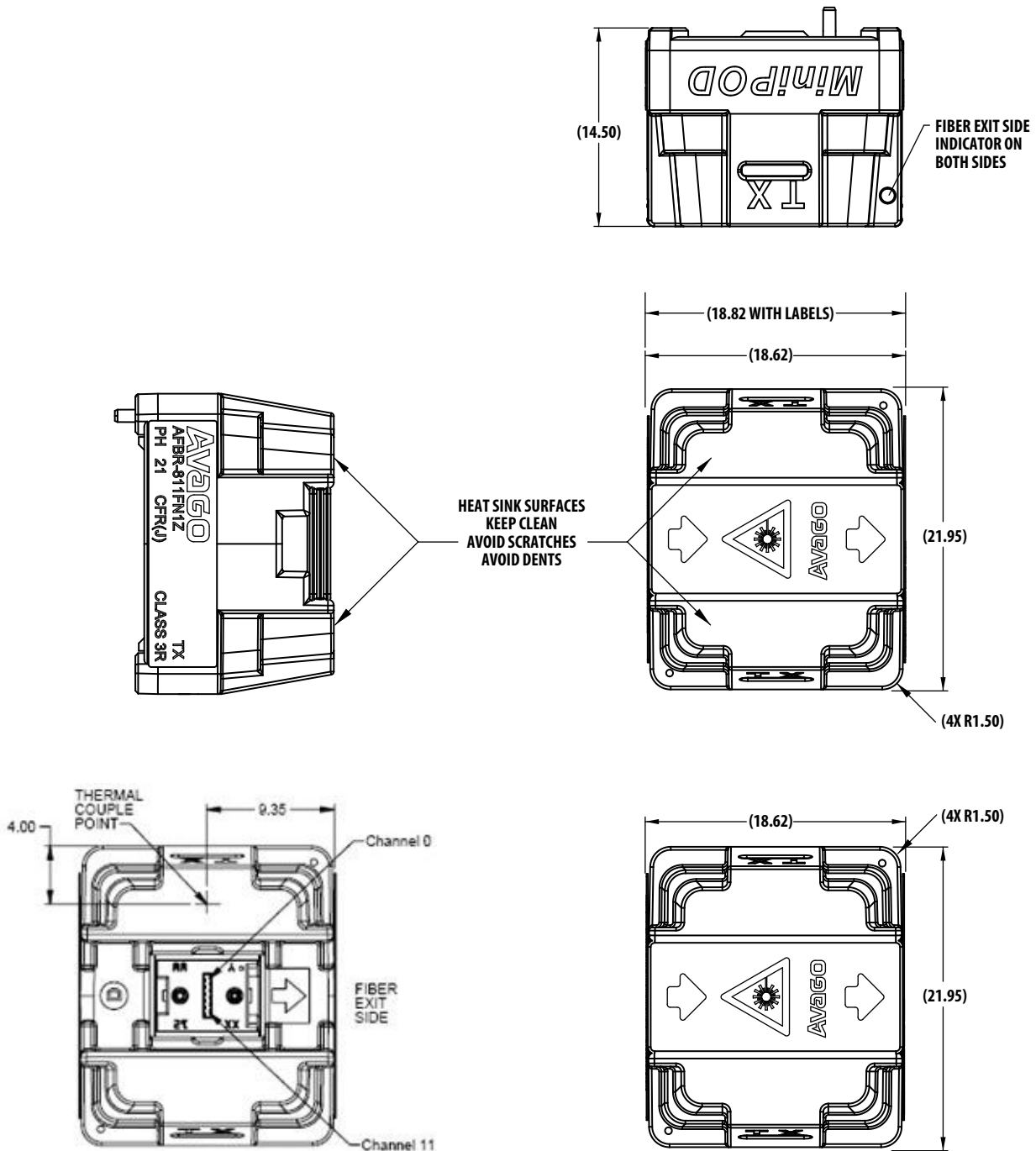
Channel 11

CHANNEL LOCATIONS ARE THE SAME FOR "TX" AND "RX"

(18.62)

(4X R1.50)

(21.95)

Figure 20. Package Dimensions 1 (mm)
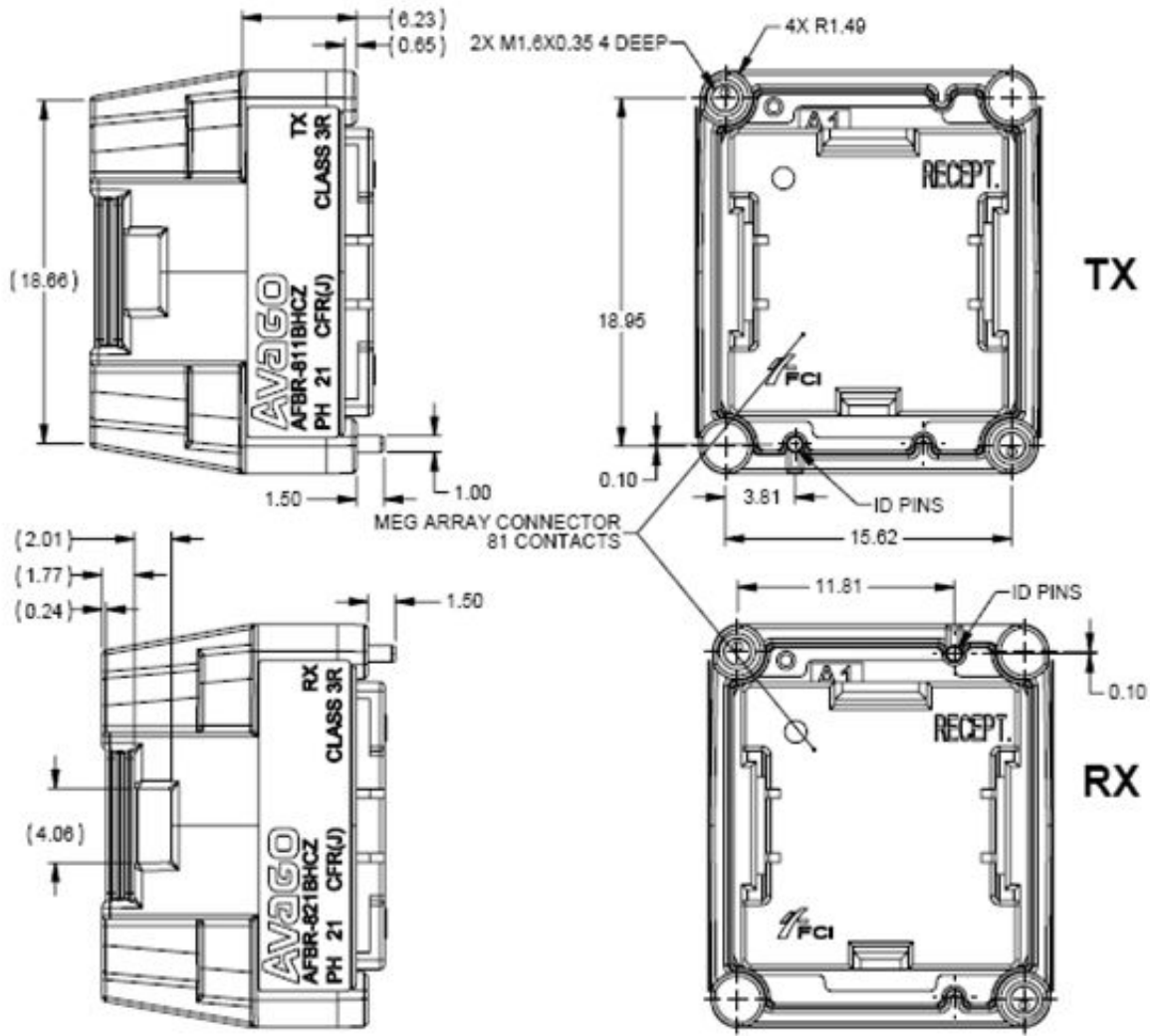
Figure 21. Package Dimensions 2 (mm)

Package Mechanical Outline – Round Cable Housing
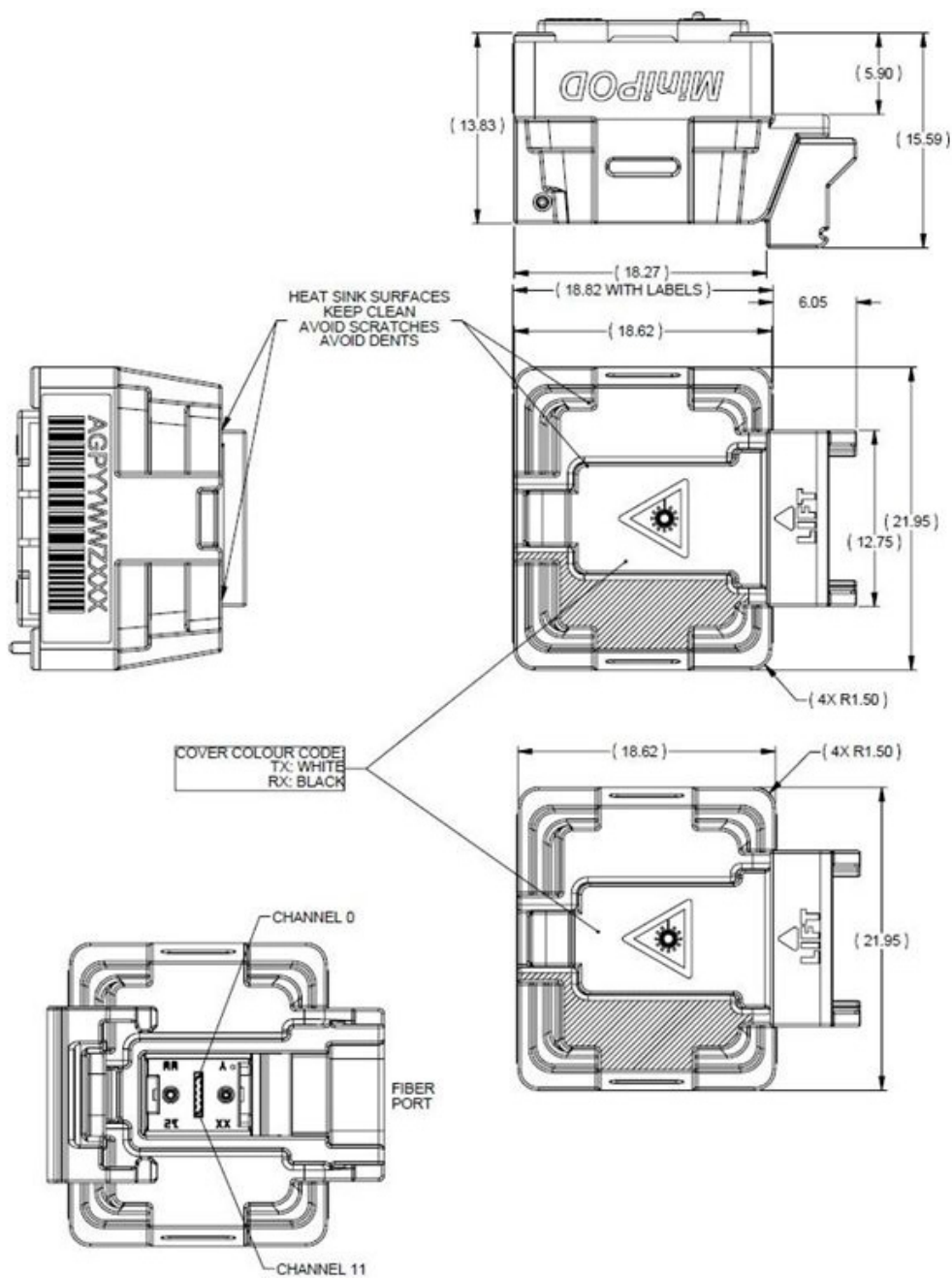
Figure 22. Package Dimensions 1 (in mm)
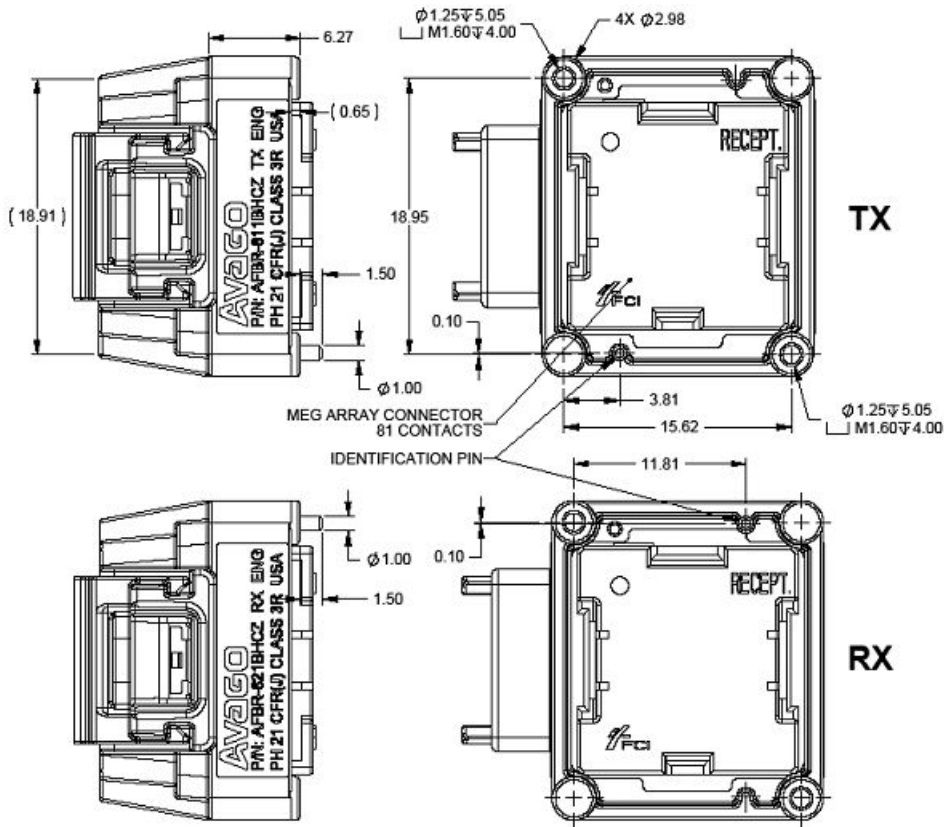
Figure 23. Package Dimensions 2 (in mm)
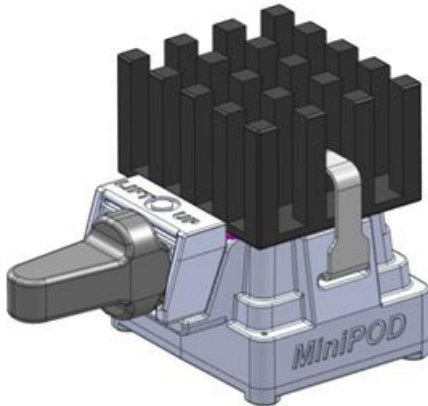
Figure 24. Heatsink Option (x = H in part number)
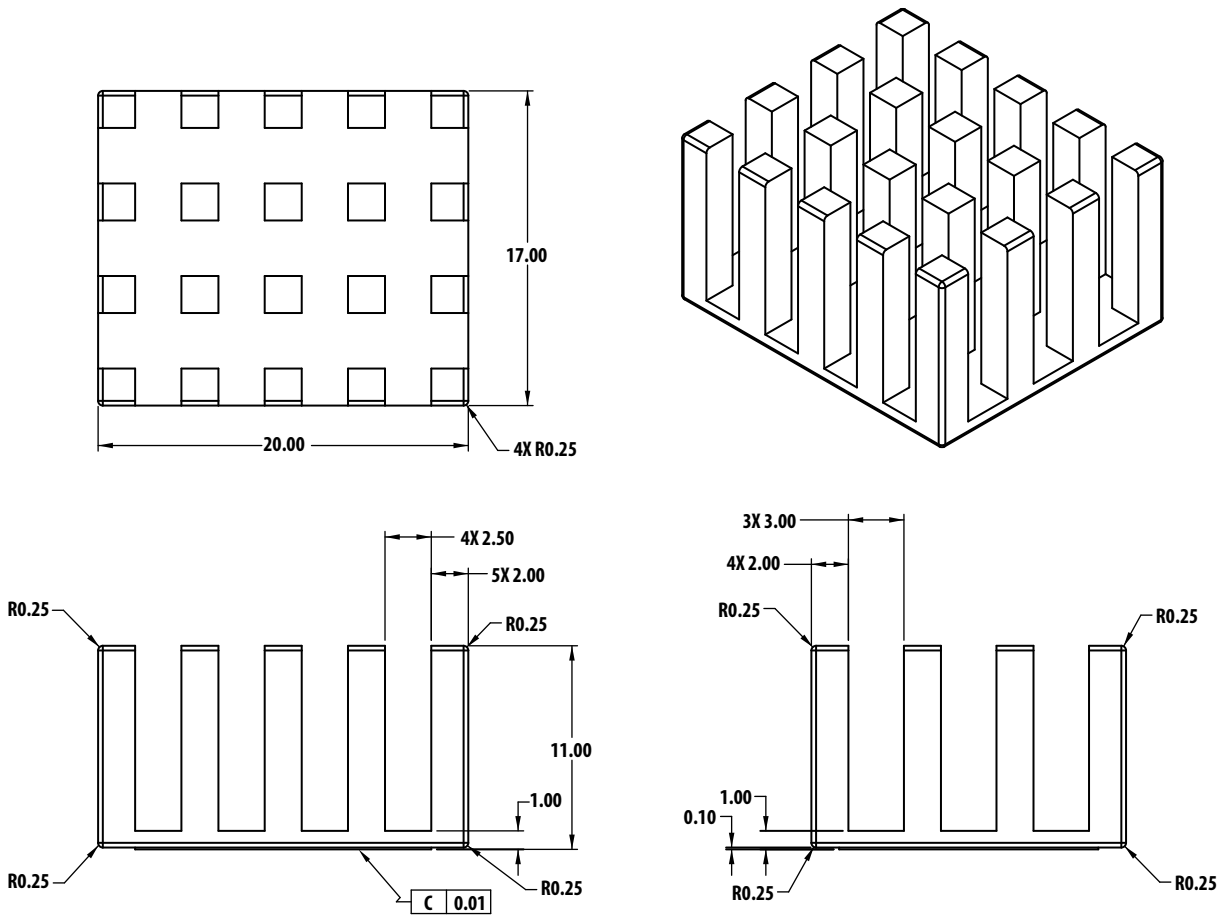
Figure 25. Heatsink Drawing (dimensions in mm)
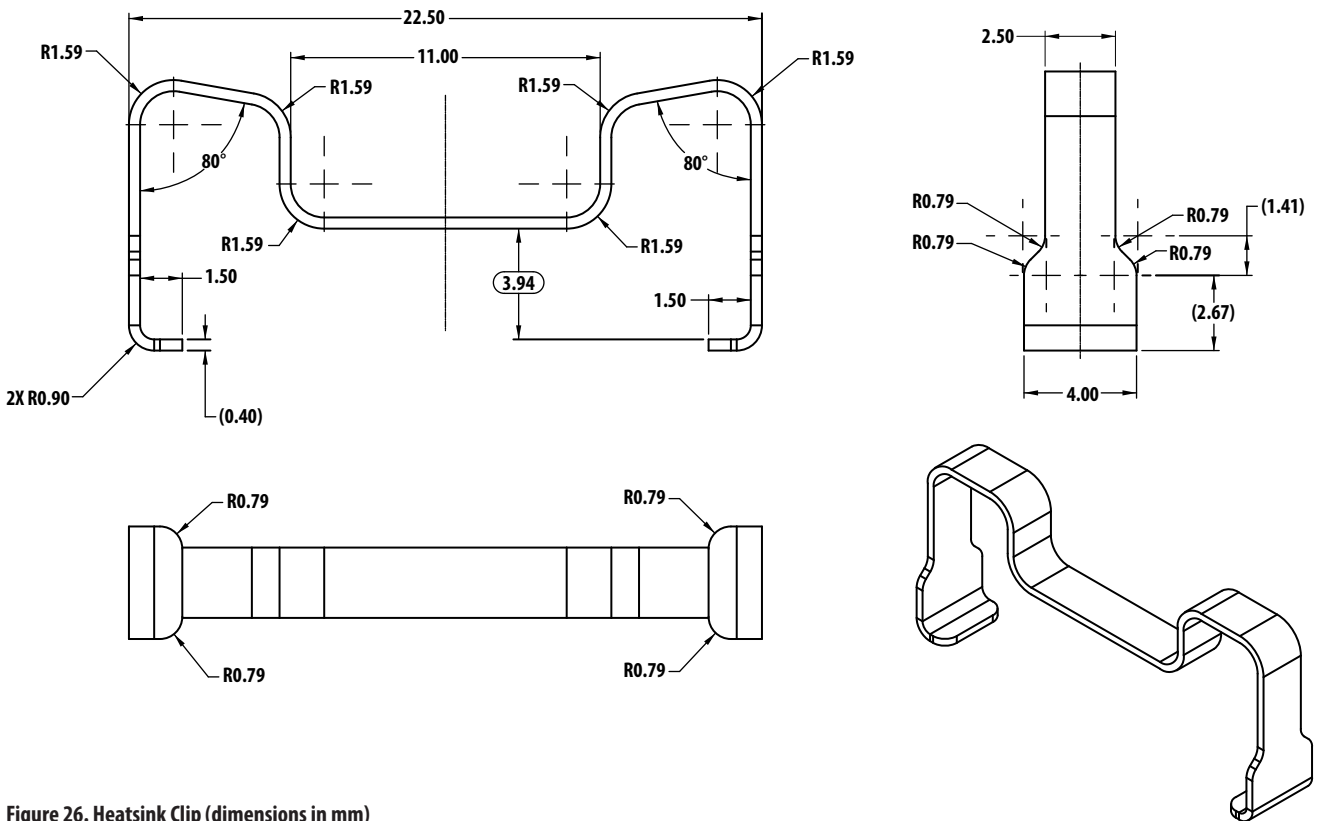
Figure 26. Heatsink Clip (dimensions in mm)

100N Maximum compressive load on the housing
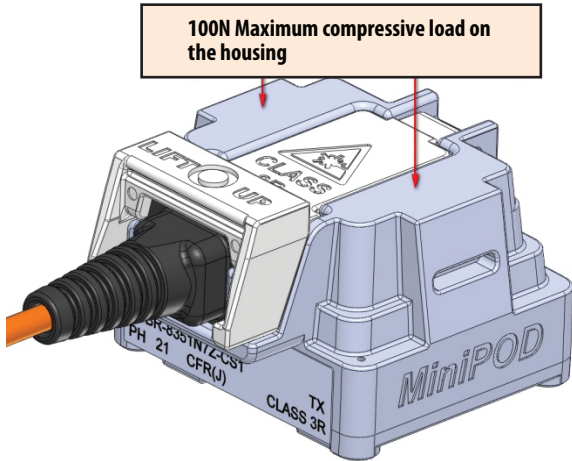
Figure 27. Module Compression Force

50N Maximum side load

50N Maximum side load
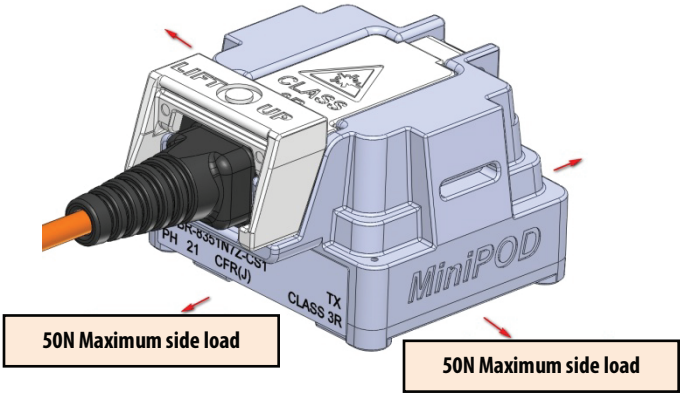
Figure 28. Module Side Force

2.2N Short Duration*
0.98N Long Term**
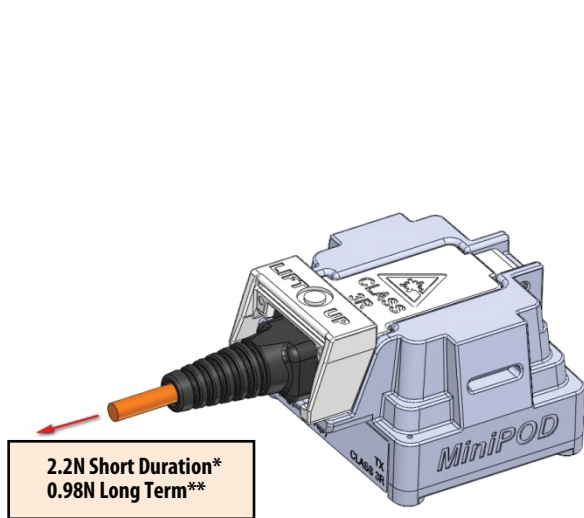
Figure 29. Fiber Pull Force
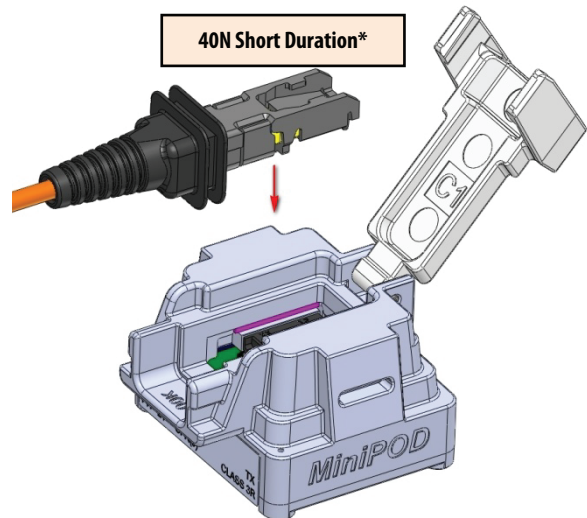
40N Short Duration*

Figure 30. PRIZM Insertion Force

* Short duration is <15 seconds.
** Long term (>5 minutes), exceeding this force long term could cause the optical light output power to drop or Rx sensitivity to diminish, which is not recoverable.

Avago Technologies Confidential. Restricted under NDA
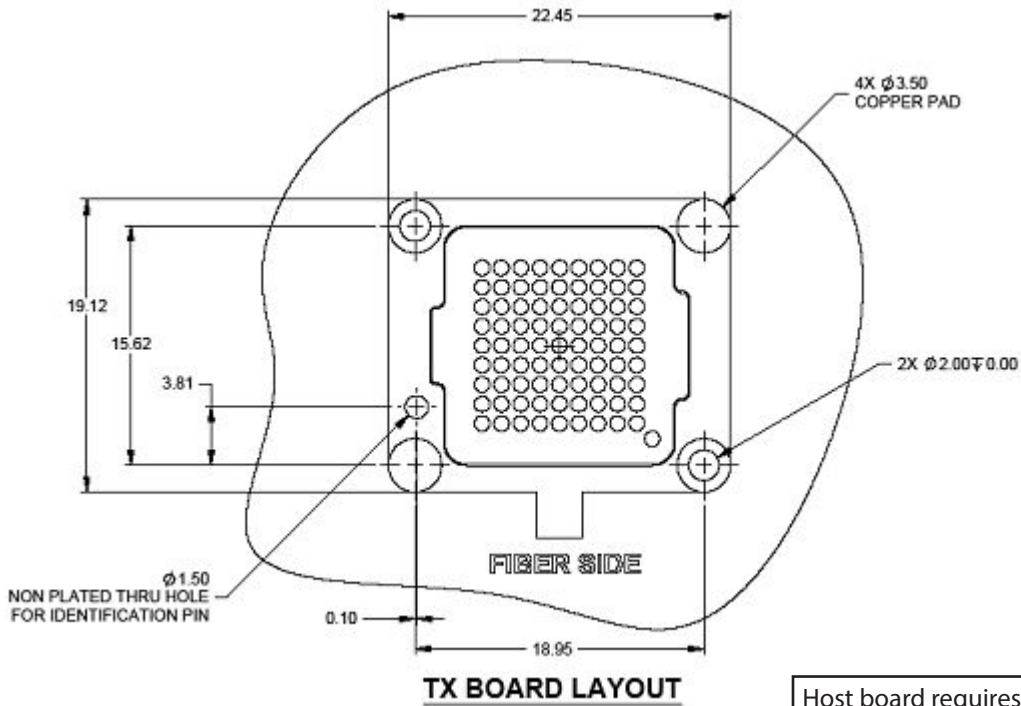
Host PCB Layout

Figure 31. TX Host PCB Layout

> Host board requires FCI P/N 55714
> 9×9 pin 4mm plug connector
> (Recommend 55714-202LF)
>
> http://portal.fciconnect.com/Comergent
> //fci/drawing/55714.pdf
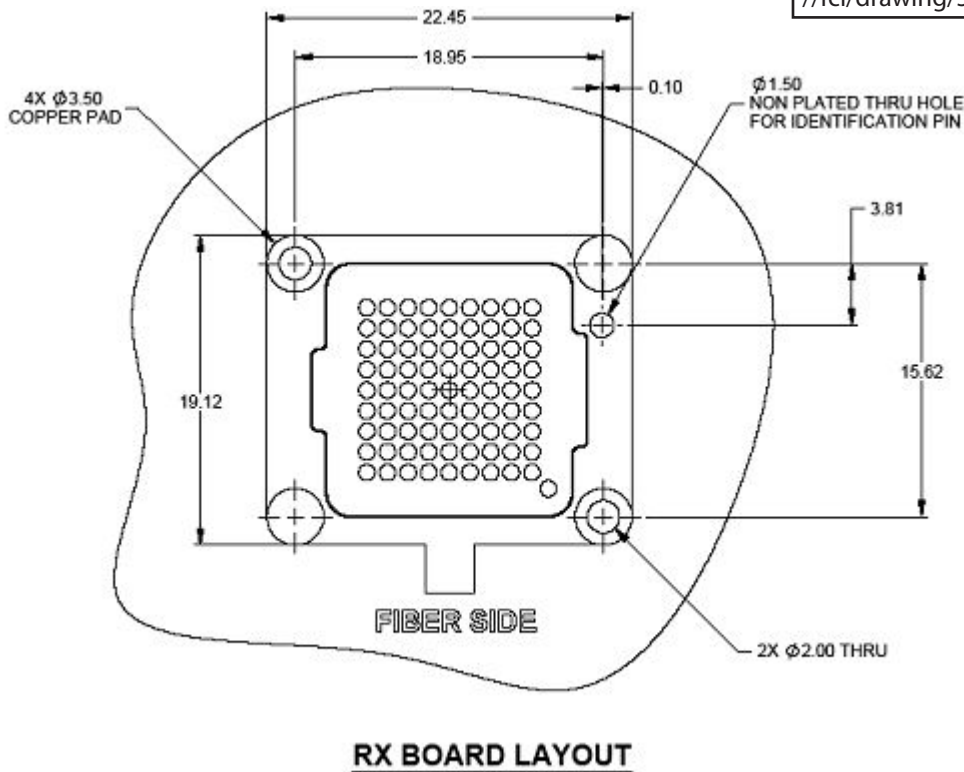
Figure 32. RX Host PCB Layout

Avago Technologies Confidential. Restricted under NDA

Optics Inspection and Cleaning

Optical inspection shall be conducted at class 100k or better environment. ESD must be taken care during the operation.

Perform first pass inspection at 30× magnification under a low power scope (e.g., LEICA GZ6E scope with fluorescent ring white lighting) for optical opening with exposed glass substrate surface.

If the surface is contaminated with foreign debris or particles, use an air gun with clean ionized dry air or nitrogen supply (pressure at ~ 5 kg/cm^2) to blow directly into the optical opening (no cotton swabs, no liquid solvents on the optics). Inspect under scope again. Repeat if necessary.

If the module requires further verification, perform second pass inspection at 80X or higher power. Set focus on the top surface ONLY of the glass substrate and complete inspection for the exposed area. If there is unacceptable contamination, the module may be routed back once for cleaning with ionized air.

The surface of the lenses should not be physically touched. Further detailed assembly specifications can be found in the Avago document titled "PRIZM® LightTurn® Connector – to – MiniPOD™ Parallel Optic Module Assembly Recommendations". Please contact the Avago sales representative for further information.

Control Interface and Memory Map

The control interface combines dedicated signal lines for address inputs, Adr[2:0], interrupt output, IntL, and reset input, ResetL, with two-wire serial, TWS, interface clock, SCL, and data, SDA, signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. In general, TWS bus timing and protocols follow the implementation popularized in Atmel Two-wire Serial EEPROMs. For additional details see, e.g., Atmel AT24C01A. Note the difference in write cycle time as described below.

If the sequence of module actions is important, at least 100 ms wait between each functional change must be used. A functional change is a 1 or 2 byte write affecting one function. For example, if a channel is disabled and then enabled in the next write, a 100 ms wait period is needed after the disable to ensure it is effective and that the subsequent write or read is acknowledged. If insufficient wait time is allowed, the write or read following the initial write will receive a NACK (no-acknowledge). Reads to any location and writes to the page select registers x5i:127 and x6i:127 do not count as functional changes

and do not require any wait time before the next read or write transaction.

The address signals, Adr2, Adr1 and Adr0, provide the ability to program the TWS bus address of the module.

The TX module address has the binary form 0101hjkx, where h, j and k correspond to Adr2, Adr1 and Adr0, respectively and x corresponds to the Read/Write command bit. Modules will respond to TWS bus addresses in the range of 50h[1] to 5Fh (hereafter 5ih) depending upon the state of Adr2, Adr1 and Adr0.

The RX module address has the binary form 0110hjkx, where h, j and k correspond to Adr2, Adr1 and Adr0, respectively and x corresponds to the Read/Write command bit. Modules will respond to TWS bus addresses in the range of 60h[2] to 6Fh (hereafter 6ih) depending upon the state of Adr2, Adr1 and Adr0.

An interrupt signal, IntL, is used to alert the host of a loss of input signal (LOS), transmitter fault conditions and/or assertion of any monitor flag. This reduces the need for dedicated status signal lines and polling the status and monitor registers while maintaining timely alerts to significant events. IntL can be programmed (page 01h byte 225 bit 0) to either pulse or static mode with static as the default mode.

A dedicated module reset signal, ResetL, is provided in case the TWS interface becomes dysfunctional. When ResetL is asserted, the outputs are disabled, TWS interface commands are inhibited and the module returns to factory default settings except Non-volatile Read-Write (RW) registers which retain the last write. A module register (memory map except the non-volatile registers) reset can also be initiated over the TWS interface (TX page 5ih or RX page 6ih byte 91, bit 0). A TWS reset can be initiated by nine SCL clock cycles with SDA high in each cycle and creating a start condition.

With the TWS interface the user can read a status register (byte 2 for TX page 5ih, RX page 6i) to see if data is available in the monitor registers, if the module has generated an IntL that has not been cleared and global status reports for loss of signal and fault conditions.

LOS, TX fault and/or monitor flag registers can be accessed to check the status of individual channels or which channel may have generated a recent IntL. LOS, TX fault and flag bits remain set (latched) after assertion even in the event the condition changes and operation resumes until cleared by the read operation of the associated registers or reset by ResetL or the TWS module reset function.

---

1. In terms ##h, the h indicates that ## is hexadecimal, if ##b, b indicates binary and if ##, then decimal.
2. In terms ##h, the h indicates that ## is hexadecimal, if ##b, b indicates binary and if ##, then decimal.

Avago Technologies Confidential. Restricted under NDA

The user can read the present value of the various monitors. For transmitters and receivers, internal module temperature and supply voltages are reported. For transmitters, monitors provide for each channel laser bias current and laser light output power (LOP) information. For receivers, input power (Pave) is monitored for each channel. In addition, elapsed operating time is reported. All monitor items are two-byte fields and to maintain coherency, the host must access these with single two-byte read sequences. For each monitored item, alarm thresholds are established. If an item moves past a threshold, a flag is set, and, provided the item is not masked, IntL is asserted. The threshold settings are available in the upper memory page, 01h.

The user can select either a pulse or static mode for the interrupt signal IntL and initiate a module register reset. The user is provided the ability to disable individual channels. For transmitters, equalization levels can be independently set for individual channels. For receivers, output signal amplitude, de-emphasis levels and rate select can be independently set for individual channels. In the upper page, 01h, control field the user can invert the truth of the differential inputs for individual transmitter channel and for the differential outputs of individual receiver channels. In addition, the user can disable the output squelch function on an individual channel basis for both transmitters and receivers. For transmitters the user can, on an individual channel basis, activate a margin mode that reduces the output optical modulation amplitude for the channel.

Most non-volatile control registers are located in the upper page 01(h). Other non-volatile functions include the IntL mode selection bit, input and output polarity flip bits, transmitter equalization control bits, receiver output amplitude control and receiver output de-emphasis control. Entries into these registers will retain the last write for supply voltage cycles and for ResetL and module register resets.

Volatile functions include module register reset, channel disable, squelch disable and margin activation.

A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, TX fault and monitor flag. Mask fields for LOS, TX fault and module monitors are in the lower memory page, 5ih for TX and 6ih for RX, and the mask field for the channel monitors are in the upper page 01h. Entries in the mask fields are volatile.

Page 00h, based on the Serial ID pages of XFP and QSFP, provides module identity and information regarding the capabilities of the module.

Avago Technologies Confidential. Restricted under NDA

The following characteristics are defined over the Recommended Operating Conditions, unless otherwise noted. Typical values are for $T_c = 40\ °C$, $V_{cc33} = 3.435\ V$ and $V_{cc25} = 2.625\ V$.

Parameter	Symbol	Min	Typ	Max	Units	Reference
LVTTL Input Voltage High Threshold	Vihttl	2			V	1
LVTTL Input Voltage Low Threshold	Vilttl			0.8	V	1
LVTTL Output Pull-up Current	Ioputtl	80		250	µA	Pull-up to 3.3 V
LVTTL Output Pull-down Current	Ioputtl	80		250	µA	Pull-down to 0.0 V
Address Assert Time			6.6	100	ms	2
Interrupt Assert Time	$t_{INTL\ ON}$		180	300	ms	3
Interrupt Pulse Width	$t_{INTL\ PW}$	5	28	50	µs	4
Interrupt De-assert Time	$t_{INTL\ OFF}$		20	500	µs	5
Reset Assert Time	$t_{RSTL\ ON}$		0.2	100	µs	6
Reset De-assert Time	$t_{RSTL\ OFF}$		350	2000	ms	7
Initialization Time TWS Interfaces				2000	ms	
Data Ready Time	t_{data}			2000	ms	8
Tx Fault Assert Time	$t_{Txfault,ON}$			200	ms	9
Flag Assert Time	$t_{flag,ON}$			200	ms	10
Mask Assert Time	$t_{mask,OFF}$			100	ms	11
Mask Deassert Time	$t_{mask,ON}$			100	ms	12
Select Change Time	$t_{ratesel}$			100	ms	13
TWS Data In Set Up Time	$t_{SU:SDA}$	0.10			µs	14
TWS Data In Hold Time	$t_{HD:SDA}$	0			µs	15
TWS Clock Low to Data Out Valid	t_{AA}	0.10		0.90	µs	16
TWS Data Out Hold Time	t_{DH}	100			ns	17
TWS Data Output Rise Time	$t_{r\ SDA}$			0.30	µs	Measured between 0.8 V and 2.0 V
TWS Data Output Fall Time	$t_{f\ SDA}$			0.30	µs	
TWS Interface Timing	See Atmel Two-Wire Serial EEPROM, e.g., AT24C01A. **Note difference in Write Cycle Time**					
TWS Write Cycle Time (up to 2 sequential bytes)	t_{WC}	100			ms	
Serial Interface Clock Holdoff – "Clock Stretching"	T_clock_hold			500	µs	18
Endurance (Write cycles)			50,000		cycles	19

Notes:
1. 3.3 V LVTTL compatible control inputs. This includes ADR[2:0] pins.
2. Is the module response time from a change in module address, Adr[2:0], to response to TWS communication using the new address.
3. This is the module response time from occurrence of interrupt generating event to IntL assertion, V_{out}:IntL = Vol.
4. Pulse or static level can be selected for IntL. Static mode is default. See Memory Map.
5. This is the module response time from clear on read operation, measured from falling SCL edge after stop bit of read transaction, until Vout:IntL = Voh where IntL is in static mode.
6. Assertion of ResetL activates a complete module reset, i.e. module returns to factory default and non-volatile control settings. While ResetL is Low, TX and RX outputs are disabled and the module does not respond to the TWS interface.
7. This is the response time from ResetL de-assertion to resumption of operation.
8. Time from power on to Data Not Ready (Byte 2, bit 0) deasserted and Int_L asserted.
9. Time from Tx Fault state to Tx Fault bit set (value = 1b) and Int_L asserted
10. Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and Int_L asserted
11. Time from mask bit set (value = 1b) until associated Int_L assertion is inhibited.
12. Time from mask bit cleared (value = 0b) until associated Int_L operation resumes.
13. Time from change of state of Application or Rate Select bit until transmitter or receiver bandwidth is in conformance with appropriate specification
14. Data In Set Up Time is measured from Vil(max)SDA or Vih(min)SDA to Vil(max)SCL.
15. Data In Hold Time is measured from Vil(max)SCL to Vil(max)SDA or Vih(min)SDA.
16. Clock Low to Data Out Time is measured from Vil(max)SCL to Vol(max)SDA or Voh(min)SDA.
17. Data Out Hold Time is measured from Vil(max)SCL to Vol(max)SDA or Voh(min)SDA.
18. Maximum time the modules may hold the SCL line low before continuing with a read or write operation.
19. 50 K write cycles at 70 °C. Applies to non-volatile control registers in memory map.

Avago Technologies Confidential. Restricted under NDA

Management Interface Timing Specification
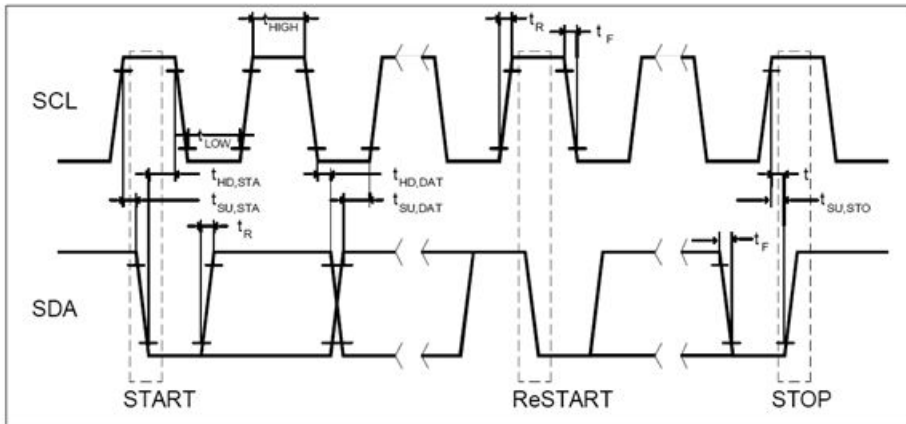
Figure 33. 2-wire Serial Interface Timing Diagram

Field Upgradable Firmware

Boot loader is a programming tool that enables MiniPOD modules to be firmware upgraded in the field over the TWS interface. Further details on how to use this capability are available from your Avago Sales Representative.

Memory Map Overview

The memory is structured as a single address, multiple page approach after that in the XFP MSA and adapted by QSFP MSA for multi-channel transceivers. Figure 34 presents an overview of the memory structure showing a lower page (5ih for TX and 6i for RX) and two upper pages (00h and 01h). As with XFP and QSFP, time sensitive, dynamic and/or high interest information are contained in the base, i.e. lower, page. Here the upper page 00h contains the serial id information, again following the style of XFP and QSFP. The 01h upper table contains static threshold information, configuration controls and flag masks.

Unless otherwise stated all reserved bytes are coded 00h and all reserved bits are coded 0b. Non-volatile read-write bits are labeled RWn and volatile read-write bits are labeled RWv.

Byte	Type	Lower Memory Page 5ih for TX, 6i for RX
0	RO	Identifier
1-2	RO	Status
3-27	RO	Interrupts Flags: LOS, Fault, Monitor
28-39	RO	Module Monitors (internal temperature, Vcc33, Vcc25
40-87	RO	Channel Monitors (TX bias, TX Output Power, RX Input Power)
88-89	RO	Elapsed Operating Time
90	RWn	Reserved
91-105	RWv	Volatile Controls (Reset, CH Diasble, CH Squelch Diable, TX Margin Enable, RX Rate Select)
106-117	RWv	Masks: LOS, Fault, Module Flags
118-126	RWv	Reserved
127	RWv	Upper Page Select Byte

RO	Read Only
RWv	Read/Write volatile
RWn	Read/Write non-volatile

Byte	Type	Upper Memory Page 00h
128-129	RO	Identifiers
130	RO	Description: Power Supplies
131	RO	Description: Max Case Temp
132-133	RO	Description: Min/Max Signal Rate
134-137	RO	Description: Wavelength
138-143	RO	Description: Supported Functions
144-151	RO	Reserved
152-170	RO	Vendor Information: Name and OUI
171-188	RO	Vendor Information: PN and PN rev
189-204	RO	Vendor Information: SN
205-212	RO	Vendor Information: Date Code
213-222	RO	Vendor Information: Customer Specific
223	RO	Checksum
224-239	RWv	Reserved
240	RO	Reserved
241-253	RO	Vendor Specific
254-255	RO	Reserved

Byte	Type	Upper Memory Page 01h
128-175	RO	Module Thresholds
176-223	RO	Channel Threholds
224	RO	Checksum
225.243	RWn	Non-volatile Controls (IntL Mode, CH Polarity, TX Equalization, RX De-emphasis and Output Amplitude)
244-255	RWv	Masks: Channel Monitor Flags

Figure 34. Two-Wire Serial Address 5ih (TX) or 6ih (RX) Page Structure

Avago Technologies Confidential. Restricted under NDA

Digital Monitoring Interface

Through TWS interface, the host can fetch the monitoring data as summarized in the previous section. The following table summarizes the function and the specifications.

Digital Monitoring Specifications

Monitor Parameter	Unit	Tolerance		DMI Range*		Alarm Setting		Comment
		min	max	min	max	min	max	
Vcc33	volt	-0.1	+0.1	3.035	3.565	3.035	3.565	Test point at module MEG-Array connector under module low power condition
Vcc25	volt	-0.1	+0.1	2.275	2.725	2.275	2.725	
Temperature	C	-5	+5	-5	95	-5	95	Internal IC temperature at module low power condition
TX Bias current	mA	-1	+1	0	11	2	10	1
TX Light Output Power	dB/dBm	- 3	+3	-9	+2.4	-9	+3	at TP2
RX Light Input Power	dB/dBm	- 3	+3	-10	+2.4	-10	+3	at TP3

*   Within DMI range, the tolerance is guaranteed. The modules still reports data if the operating condition is out of the DMI range, but the tolerance is not guaranteed.

Notes:
1. TX bias DMI report accuracy not guaranteed when TX squelch is disabled, and LOS is asserted, i.e. no valid electrical inputs into TX.

Avago Technologies Confidential. Restricted under NDA

TX Memory Map 5ih Lower Page

Details of the base or lower page of the memory map for a transmitter follow.

Address			
Byte	Bit	Type	Field Name/Description
0	all	RO	Type Identifier: Coded 00h for unspecified
1	all	RO	Reserved Status: Coded 00h
2	7-4	RO	Reserved: Coded 0000b
2	3	RO	Fault Status: Coded 1 when a Fault flag (bytes 11 and 12 of this page) is asserted for any channel, else 0. Clears when Fault flags are cleared.
2	2	RO	LOS Status: Coded 1 when a LOS flag (bytes 9 and 10 of this page) is asserted for any channel, else 0. Clears when LOS flags are cleared.
2	1	RO	IntL Status: Coded 1 for asserted IntL. Clears to 0 when all flags including LOS and Fault are cleared.
2	0	RO	Data Not Ready: Coded 1 until data is available in monitor registers. Coded 0 in normal operation.
3-8	all	RO	Reserved Flags: Coded 00h
9	7-4	RO	Reserved: Coded 0000b
9	3	RO	LOS Latched TX Channel 11: Coded 1 when asserted, Latched, Clears on Read.
9	2	RO	LOS Latched TX Channel 10: Coded 1 when asserted, Latched, Clears on Read.
9	1	RO	LOS Latched TX Channel 9: Coded 1 when asserted, Latched, Clears on Read.
9	0	RO	LOS Latched TX Channel 8: Coded 1 when asserted, Latched, Clears on Read.
10	7	RO	LOS Latched TX Channel 7: Coded 1 when asserted, Latched, Clears on Read.
10	6	RO	LOS Latched TX Channel 6: Coded 1 when asserted, Latched, Clears on Read.
10	5	RO	LOS Latched TX Channel 5: Coded 1 when asserted, Latched, Clears on Read.
10	4	RO	LOS Latched TX Channel 4: Coded 1 when asserted, Latched, Clears on Read.
10	3	RO	LOS Latched TX Channel 3: Coded 1 when asserted, Latched, Clears on Read.
10	2	RO	LOS Latched TX Channel 2: Coded 1 when asserted, Latched, Clears on Read.
10	1	RO	LOS Latched TX Channel 1: Coded 1 when asserted, Latched, Clears on Read.
10	0	RO	LOS Latched TX Channel 0: Coded 1 when asserted, Latched, Clears on Read.
11	7-4	RO	Reserved: Coded 0000b
11	3	RO	Fault Latched TX Channel 11: Coded 1 when asserted, Latched, Clears on Read.
11	2	RO	Fault Latched TX Channel 10: Coded 1 when asserted, Latched, Clears on Read.
11	1	RO	Fault Latched TX Channel 9: Coded 1 when asserted, Latched, Clears on Read.
11	0	RO	Fault Latched TX Channel 8: Coded 1 when asserted, Latched, Clears on Read.
12	7	RO	Fault Latched TX Channel 7: Coded 1 when asserted, Latched, Clears on Read.
12	6	RO	Fault Latched TX Channel 6: Coded 1 when asserted, Latched, Clears on Read.
12	5	RO	Fault Latched TX Channel 5: Coded 1 when asserted, Latched, Clears on Read.
12	4	RO	Fault Latched TX Channel 4: Coded 1 when asserted, Latched, Clears on Read.
12	3	RO	Fault Latched TX Channel 2: Coded 1 when asserted, Latched, Clears on Read.
12	2	RO	Fault Latched TX Channel 2: Coded 1 when asserted, Latched, Clears on Read.
12	1	RO	Fault Latched TX Channel 1: Coded 1 when asserted, Latched, Clears on Read.
12	0	RO	Fault Latched TX Channel 0: Coded 1 when asserted, Latched, Clears on Read.
13	7	RO	High Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
13	6	RO	Low Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
13	5-0	RO	Reserved
14	7	RO	High Internal 3.3 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
14	6	RO	Low Internal 3.3 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
14	5-4	RO	Reserved
14	3	RO	High Internal 2.5 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
14	2	RO	Low Internal 2.5 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
14	1-0	RO	Reserved
15	all	RO	Reserved: Coded 00h

Avago Technologies Confidential. Restricted under NDA

Address			
Byte	Bit	Type	Field Name/Description
16	7	RO	High TX Bias Current Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read.
16	6	RO	Low TX Bias Current Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read.
16	5-4	RO	Reserved
16	3	RO	High TX Bias Current Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read.
16	2	RO	Low TX Bias Current Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read.
16	1-0	RO	Reserved
17	7	RO	High TX Bias Current Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read.
17	6	RO	Low TX Bias Current Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read.
17	5-4	RO	Reserved
17	3	RO	High TX Bias Current Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read.
17	2	RO	Low TX Bias Current Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read.
17	1-0	RO	Reserved
18	7	RO	High TX Bias Current Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read.
18	6	RO	Low TX Bias Current Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read.
18	5-4	RO	Reserved
18	3	RO	High TX Bias Current Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read.
18	2	RO	Low TX Bias Current Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read.
18	1-0	RO	Reserved
19	7	RO	High TX Bias Current Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read.
19	6	RO	Low TX Bias Current Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read.
19	5-4	RO	Reserved
19	3	RO	High TX Bias Current Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read.
19	2	RO	Low TX Bias Current Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read.
19	1-0	RO	Reserved
20	7	RO	High TX Bias Current Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read.
20	6	RO	Low TX Bias Current Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read.
20	5-4	RO	Reserved
20	3	RO	High TX Bias Current Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read.
20	2	RO	Low TX Bias Current Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read.
20	1-0	RO	Reserved
21	7	RO	High TX Bias Current Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read.
21	6	RO	Low TX Bias Current Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read.
21	5-4	RO	Reserved
21	3	RO	High TX Bias Current Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read.
21	2	RO	Low TX Bias Current Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read.
21	1-0	RO	Reserved
22	7	RO	High TX Power Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read.
22	6	RO	Low TX Power Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read.
22	5-4	RO	Reserved
22	3	RO	High TX Power Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read.
22	2	RO	Low TX Power Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read.
22	1-0	RO	Reserved
23	7	RO	High TX Power Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read.
23	6	RO	Low TX Power Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read.
23	5-4	RO	Reserved
23	3	RO	High TX Power Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read.
23	2	RO	Low TX Power Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read.
23	1-0	RO	Reserved

Avago Technologies Confidential. Restricted under NDA

Address Byte	Bit	Type	Field Name/Description
24	7	RO	High TX Power Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read.
24	6	RO	Low TX Power Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read.
24	5-4	RO	Reserved
24	3	RO	High TX Power Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read.
24	2	RO	Low TX Power Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read.
24	1-0	RO	Reserved
25	7	RO	High TX Power Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read.
25	6	RO	Low TX Power Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read.
25	5-4	RO	Reserved
25	3	RO	High TX Power Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read.
25	2	RO	Low TX Power Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read.
25	1-0	RO	Reserved
26	7	RO	High TX Power Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read.
26	6	RO	Low TX Power Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read.
26	5-4	RO	Reserved
26	3	RO	High TX Power Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read.
26	2	RO	Low TX Power Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read.
26	1-0	RO	Reserved
27	7	RO	High TX Power Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read.
27	6	RO	Low TX Power Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read.
27	5-4	RO	Reserved
27	3	RO	High TX Power Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read.
27	2	RO	Low TX Power Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read.
27	1-0	RO	Reserved
28	all	RO	Internal Temperature Monitor MSB: Integer part coded in signed 2's complement. Tolerance is ±3° C.
29	all	RO	Internal Temperature Monitor LSB: Fractional part in units of 1°/256 coded in binary.
30-31	all	RO	Reserved: Coded 00h
32-33	all	RO	Internal 3.3 Vcc Monitor: Voltage in 100 μV units coded as 16 bit unsigned integer, Byte 32 is MSB. Tolerance is ± 0.1V.
34-35	all	RO	Internal 2.5 Vcc Monitor: Voltage in 100 μV units coded as 16 bit unsigned integer, Byte 34 is MSB. Tolerance is ± 0.1V.
36-39	all	RO	Reserved Monitor: Coded 00h
40-41	all	RO	TX Bias Current Monitor[1] Channel 11: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 40 is MSB. Tolerance is ± 1 mA.
42-43	all	RO	TX Bias Current Monitor Channel 10: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 42 is MSB. Tolerance is ± 1 mA
44-45	all	RO	TX Bias Current Monitor Channel 9: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 44 is MSB. Tolerance is ± 1 mA
46-47	all	RO	TX Bias Current Monitor Channel 8: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 46 is MSB. Tolerance is ± 1 mA
48-49	all	RO	TX Bias Current Monitor Channel 7: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 48 is MSB. Tolerance is ± 1 mA
50-51	all	RO	TX Bias Current Monitor Channel 6: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 50 is MSB. Tolerance is ± 1 mA
52-53	all	RO	TX Bias Current Monitor Channel 5: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 52 is MSB. Tolerance is ± 1 mA
54-55	all	RO	TX Bias Current Monitor Channel 4: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 54 is MSB. Tolerance is ± 1 mA

Note:
1. DMI Vcc is measured reference to the internal voltage, not the Y measurement point on the reference Vcc drawing

Avago Technologies Confidential. Restricted under NDA

Address			
Byte	Bit	Type	Field Name/Description
56-57	all	RO	TX Bias Current Monitor Channel 3: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 56 is MSB. Tolerance is ± 1 mA
58-59	all	RO	TX Bias Current Monitor Channel 2: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 58 is MSB. Tolerance is ± 1 mA
60-61	all	RO	TX Bias Current Monitor Channel 1: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 60 is MSB. Tolerance is ± 1 mA
62-63	all	RO	TX Bias Current Monitor Channel 0: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 62 is MSB. Tolerance is ± 1 mA
64-65	all	RO	TX Light Output Monitor Channel 11: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 64 is MSB. Tolerance is ± 3dB.
66-67	all	RO	TX Light Output Monitor Channel 10: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 66 is MSB. Tolerance is ± 3 dB.
68-69	all	RO	TX Light Output Monitor Channel 9: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 68 is MSB. Tolerance is ± 3 dB
70-71	all	RO	TX Light Output Monitor Channel 8: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 70 is MSB. Tolerance is ± 3 dB.
72-73	all	RO	TX Light Output Monitor Channel 7: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 72 is MSB. Tolerance is ± 3 dB.
74-75	all	RO	TX Light Output Monitor Channel 6: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 74 is MSB. Tolerance is ± 3 dB.
76-77	all	RO	TX Light Output Monitor Channel 5: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 76 is MSB. Tolerance is ± 3dB.
78-79	all	RO	TX Light Output Monitor Channel 4: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 78 is MSB. Tolerance is ± 3 dB.
80-81	all	RO	TX Light Output Monitor Channel 3: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 80 is MSB. Tolerance is ± 3 dB.
82-83	all	RO	TX Light Output Monitor Channel 2: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 82 is MSB. Tolerance is ± 3 dB.
84-85	all	RO	TX Light Output Monitor Channel 1: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 84 is MSB. Tolerance is ± 3dB.
86-87	all	RO	TX Light Output Monitor Channel 0: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 86 is MSB. Tolerance is ± 3 dB
88-89	all	RO	Elapsed (Power-on) Operating Time: Elapsed time in 2 hour units coded as 16 bit unsigned integer, Byte 88 is MSB, Tolerance is ± 10%
90	all	RWn	Reserved Control: Coded 00h
91	7-1	RWv	Reserved: Coded 0000000b
91	0	RWv	Transmitter Reset: Writing 1 return all registers except non-volatile RW to factory default values. Reads 0 after operation.
92	7-4	RWv	Reserved: Coded 0000b
92	3	RWv	TX Channel 11 Disable: Writing 1 deactivates the optical output, Default is 0.
92	2	RWv	TX Channel 10 Disable: Writing 1 deactivates the optical output, Default is 0.
92	1	RWv	TX Channel 9 Disable: Writing 1 deactivates the optical output, Default is 0.
92	0	RWv	TX Channel 8 Disable: Writing 1 deactivates the optical output, Default is 0.
93	7	RWv	TX Channel 7 Disable: Writing 1 deactivates the optical output, Default is 0.
93	6	RWv	TX Channel 6 Disable: Writing 1 deactivates the optical output, Default is 0.
93	5	RWv	TX Channel 5 Disable: Writing 1 deactivates the optical output, Default is 0.
93	4	RWv	TX Channel 4 Disable: Writing 1 deactivates the optical output, Default is 0.
93	3	RWv	TX Channel 3 Disable: Writing 1 deactivates the optical output, Default is 0.
93	2	RWv	TX Channel 2 Disable: Writing 1 deactivates the optical output, Default is 0.
93	1	RWv	TX Channel 1 Disable: Writing 1 deactivates the optical output, Default is 0.
93	0	RWv	TX Channel 0 Disable: Writing 1 deactivates the optical output, Default is 0.

Avago Technologies Confidential. Restricted under NDA

Address			
Byte	Bit	Type	Field Name/Description
94	7-4	RWv	Reserved: Coded 0000b
94	3	RWv	Squelch Disable Channel 11: Writing 1 inhibits squelch for the channel, Default is 0.
94	2	RWv	Squelch Disable Channel 10: Writing 1 inhibits squelch for the channel, Default is 0.
94	1	RWv	Squelch Disable Channel 9: Writing 1 inhibits squelch for the channel, Default is 0.
94	0	RWv	Squelch Disable Channel 8: Writing 1 inhibits squelch for the channel, Default is 0.
95	7	RWv	Squelch Disable Channel 7: Writing 1 inhibits squelch for the channel, Default is 0.
95	6	RWv	Squelch Disable Channel 6: Writing 1 inhibits squelch for the channel, Default is 0.
95	5	RWv	Squelch Disable Channel 5: Writing 1 inhibits squelch for the channel, Default is 0.
95	4	RWv	Squelch Disable Channel 4: Writing 1 inhibits squelch for the channel, Default is 0.
95	3	RWv	Squelch Disable Channel 3: Writing 1 inhibits squelch for the channel, Default is 0.
95	2	RWv	Squelch Disable Channel 2: Writing 1 inhibits squelch for the channel, Default is 0.
95	1	RWv	Squelch Disable Channel 1: Writing 1 inhibits squelch for the channel, Default is 0.
95	0	RWv	Squelch Disable Channel 0: Writing 1 inhibits squelch for the channel, Default is 0.
96-98	all	RWv	Reserved: Coded 00h
99	7-4	RWv	Reserved: Coded 0000b
99	3	RWv	Margin Activation Channel 11: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
99	2	RWv	Margin Activation Channel 10: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
99	1	RWv	Margin Activation Channel 9: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
100	0	RWv	Margin Activation Channel 8: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
100	7	RWv	Margin Activation Channel 7: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
100	6	RWv	Margin Activation Channel 6: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
100	5	RWv	Margin Activation Channel 5: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
100	4	RWv	Margin Activation Channel 4: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
100	3	RWv	Margin Activation Channel 3: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
100	2	RWv	Margin Activation Channel 2: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
100	1	RWv	Margin Activation Channel 1: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
100	0	RWv	Margin Activation Channel 0: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0.
101	7–0	RWv	Reserved: Coded 00h
102-105	all	RWv	Reserved Controls: Coded 00h
106-111	all	RWv	Reserved Masks: Coded 00h
112	7-4	RWv	Reserved: Coded 0000b
112	3	RWv	Mask LOS TX Channel 11: Writing 1 Prevents IntL generation, Default = 0
112	2	RWv	Mask LOS TX Channel 10: Writing 1 Prevents IntL generation, Default = 0
112	1	RWv	Mask LOS TX Channel 9: Writing 1 Prevents IntL generation, Default = 0
112	0	RWv	Mask LOS TX Channel 8: Writing 1 Prevents IntL generation, Default = 0

| Address | | | |
Byte	Bit	Type	Field Name/Description
113	7	RWv	Mask LOS TX Channel 7: Writing 1 Prevents IntL generation, Default = 0
113	6	RWv	Mask LOS TX Channel 6: Writing 1 Prevents IntL generation, Default = 0
113	5	RWv	Mask LOS TX Channel 5: Writing 1 Prevents IntL generation, Default = 0
113	4	RWv	Mask LOS TX Channel 4: Writing 1 Prevents IntL generation, Default = 0
113	3	RWv	Mask LOS TX Channel 3: Writing 1 Prevents IntL generation, Default = 0
113	2	RWv	Mask LOS TX Channel 2: Writing 1 Prevents IntL generation, Default = 0
113	1	RWv	Mask LOS TX Channel 1: Writing 1 Prevents IntL generation, Default = 0
113	0	RWv	Mask LOS TX Channel 0: Writing 1 Prevents IntL generation, Default = 0
114	7-4	RWv	Reserved: Coded 0000b
114	3	RWv	Mask Fault TX Channel 11: Writing 1 Prevents IntL generation, Default = 0
114	2	RWv	Mask Fault TX Channel 10: Writing 1 Prevents IntL generation, Default = 0
114	1	RWv	Mask Fault TX Channel 9: Writing 1 Prevents IntL generation, Default = 0
114	0	RWv	Mask Fault TX Channel 8: Writing 1 Prevents IntL generation, Default = 0
115	7	RWv	Mask Fault TX Channel 7: Writing 1 Prevents IntL generation, Default = 0
115	6	RWv	Mask Fault TX Channel 6: Writing 1 Prevents IntL generation, Default = 0
115	5	RWv	Mask Fault TX Channel 5: Writing 1 Prevents IntL generation, Default = 0
115	4	RWv	Mask Fault TX Channel 4: Writing 1 Prevents IntL generation, Default = 0
115	3	RWv	Mask Fault TX Channel 3: Writing 1 Prevents IntL generation, Default = 0
115	2	RWv	Mask Fault TX Channel 2: Writing 1 Prevents IntL generation, Default = 0
115	1	RWv	Mask Fault TX Channel 1: Writing 1 Prevents IntL generation, Default = 0
115	0	RWv	Mask Fault TX Channel 0: Writing 1 Prevents IntL generation, Default = 0
116	7	RWv	Mask High Internal Temperature Alarm: Writing 1 Prevents IntL generation, Default = 0
116	6	RWv	Mask Low Internal Temperature Alarm: Writing 1 Prevents IntL generation, Default = 0
116	5-0	RWv	Reserved
117	7	RWv	Mask High Internal 3.3 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0
117	6	RWv	Mask Low Internal 3.3 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0
117	5-4	RWv	Reserved
117	3	RWv	Mask High Internal 2.5 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0
117	2	RWv	Mask Low Internal 2.5 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0
117	1-0	RWv	Reserved
118-122	all	RWn	Reserved
123-126	all	RWv	Reserved: Coded 00h
127	all	RWv	Page Select Byte

Avago Technologies Confidential. Restricted under NDA

TX Memory Map 00h Upper Page

Transmitter serial ID page 00h entries and a description of the registers follow.

| Address | | | | |
Byte	Bit	Code	Type	Field Name/Description
128	all	00h	RO	Type Identifier: Coded 00h for unspecified. See SFF-8472 for reference
129	all	01000010b	RO	Module Description: Coded for < 2.0 W max, Controlled Launch
130	all	11000000b	RO	Required Power Supplies: Coded for 3.3 V and 2.5 V supplies
131	all	01010101b	RO	Max Short-term Operating Case Temperature in °C: Coded for 85 °C
132	all	00001100b	RO	Min Bit Rate in 100 Mb/s units: Coded for 1250 Mb/s
133	all	01100111b	RO	Max Bit Rate in 100 Mb/s units: Coded for 10312 Mb/s
134-135	all	42h 04h	RO	Nominal Laser Wavelength (Wavelength in nm = value / 20): Coded for 845 nm
136-137	all	0Bh BBh	RO	Wavelength deviation from nominal (Wavelength tolerance in nm = ± value / 200): Coded for 15 nm
138	all	11001000b	RO	Supported Flags/Actions: Coded for TX Fault, TX LOS, Output Squelch for LOS, Alarm Flags
139	all	11000101b	RO	Supported Monitors: Coded for TX Bias, TX LOP, Internal Temp, Elapsed Time
140	all	01100000b	RO	Supported Monitors: Coded for 3.3 V, 2.5 V
141	all	10100010b	RO	Supported Controls: Coded for Ch Disable, Squelch Disable, Input Equalization
142	all	00001011b	RO	Supported Controls: Coded for Margin Mode, Ch Polarity Flip, Module Addressing
143	all	00h	RO	Supported Functions
144-151	all	00h	RO	Reserved
152-167	all	41h 56h 41h 47h 4Fh 20h 20h x10	RO	Vendor Name in ASCII: Coded "AVAGO" for Avago Technologies, Spaces (20h) for unused characters. Left justified.
168-170	all	00h 17h 6Ah	RO	Vendor OUI (IEEE ID): Coded "00h 17h 6Ah" for Avago Technologies
171-186	all	41h 46h 42h 52h 2Dh 38h 31h 31h 46h 4Eh 33h 5Ah 20h 20h 20h 20h	RO	Vendor Part Number in ASCII: "AFBR-811FN3Z" or "AFBR-811RN3Z". Left justified with spaces (20h) for unused bytes
187-188	all	20h 20h	RO	Vendor Revision Number in ASCII: Coded with spaces (20h)
189-204	all		RO	Vendor Serial Number (ASCII): Varies by unit. Left justified with space (20h) for unused bytes
205-212	all		RO	Vendor Date Code YYYYMMDD (ASCII)
213-222	all		RO	Customer Specific Area.
223	all		RO	Check sum addresses 128 through 222
224-255	all		RO	Vendor Specific

TX Memory Map 01h Upper Page

Details of transmitter upper page 01h follow.

Address Byte	Bit	Type	Field Name/Description
128	all	RO	Internal Temperature High Alarm Threshold MSB: Integer part coded in signed 2's complement
129	all	RO	Internal Temperature High Alarm Threshold LSB: Fractional part in units of 1°/256 coded in binary.
130	all	RO	Internal Temperature Low Alarm Threshold MSB: Integer part coded in signed 2's complement
131	all	RO	Internal Temperature Low Alarm Threshold LSB: Fractional part in units of 1°/256 coded in binary.
132-143	all	RO	Reserved: Coded 00h
144-145	all	RO	Internal 3.3 Vcc High Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB.
146-147	all	RO	Internal 3.3 Vcc Low Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB.
148-151	all	RO	Reserved
152-153	all	RO	Internal 2.5 Vcc High Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB.
154-155	all	RO	Internal 2.5 Vcc Low Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB.
156-159	all	RO	Reserved
160-175	all	RO	Thresholds Reserved: Coded 00h
176-177	all	RO	TX Bias Current All Channels High Alarm Threshold: Current in 2 μA units coded as 16 bit unsigned integer, low address is MSB.
178-179	all	RO	TX Bias Current All Channels Low Alarm Threshold: Current in 2 μA units coded as 16 bit unsigned integer, low address is MSB.
180-183	all	RO	Reserved
184-185	all	RO	TX Optical Power All Channels High Alarm Threshold: Optical power in 0.1 μW units coded as 16 bit unsigned integer, low address is MSB.
186-187	all	RO	TX Optical Power All Channels Low Alarm Threshold: Optical power in 0.1 μW units coded as 16 bit unsigned integer, low address is MSB.
188-223	all	RO	Thresholds Reserved: Coded 00h
224	all	RO	Check sum: Low order 8 bits of the sum of all bytes from 128 through 223 inclusive
225	7-1	RWn	Reserved: Coded 0000000b
225	0	RWn	IntL Pulse/Static Option: Writing 1 sets IntL to Static mode, Default is 1 for Static mode
226	7-4	RWn	Reserved: Coded 0000b
226	3	RWn	Input Polarity Flip Channel 11: Writing 1 inverts truth of the differential input pair, Default is 0.
226	2	RWn	Input Polarity Flip Channel 10: Writing 1 inverts truth of the differential input pair, Default is 0.
226	1	RWn	Input Polarity Flip Channel 9: Writing 1 inverts truth of the differential input pair, Default is 0.
226	0	RWn	Input Polarity Flip Channel 8: Writing 1 inverts truth of the differential input pair, Default is 0.
227	7	RWn	Input Polarity Flip Channel 7: Writing 1 inverts truth of the differential input pair, Default is 0.
227	6	RWn	Input Polarity Flip Channel 6: Writing 1 inverts truth of the differential input pair, Default is 0.
227	5	RWn	Input Polarity Flip Channel 5: Writing 1 inverts truth of the differential input pair, Default is 0.
227	4	RWn	Input Polarity Flip Channel 4: Writing 1 inverts truth of the differential input pair, Default is 0.
227	3	RWn	Input Polarity Flip Channel 3: Writing 1 inverts truth of the differential input pair, Default is 0.
227	2	RWn	Input Polarity Flip Channel 2: Writing 1 inverts truth of the differential input pair, Default is 0.
227	1	RWn	Input Polarity Flip Channel 1: Writing 1 inverts truth of the differential input pair, Default is 0.
227	0	RWn	Input Polarity Flip Channel 0: Writing 1 inverts truth of the differential input pair, Default is 0.
228	7-4	RWn	TX Input Equalization Control Channel 11: See Code Description on page 42. Default = 0010b
228	3-0	RWn	TX Input Equalization Control Channel 10: See Code Description on page 42. Default = 0010b

Address			
Byte	Bit	Type	Field Name/Description
229	7-4	RWn	TX Input Equalization Control Channel 9: See Code Description on page 42. Default = 0010b
229	3-0	RWn	TX Input Equalization Control Channel 8: See Code Description on page 42. Default = 0010b
230	7-4	RWn	TX Input Equalization Control Channel 7: See Code Description on page 42. Default = 0010b
230	3-0	RWn	TX Input Equalization Control Channel 6: See Code Description on page 42. Default = 0010b
231	7-4	RWn	TX Input Equalization Control Channel 5: See Code Description on page 42. Default = 0010b
231	3-0	RWn	TX Input Equalization Control Channel 4: See Code Description on page 42. Default = 0010b
232	7-4	RWn	TX Input Equalization Control Channel 3: See Code Description on page 42. Default = 0010b
232	3-0	RWn	TX Input Equalization Control Channel 2: See Code Description on page 42. Default = 0010b
233	7-4	RWn	TX Input Equalization Control Channel 1: See Code Description on page 42. Default = 0010b
233	3-0	RWn	TX Input Equalization Control Channel 0: See Code Description on page 42. Default = 0010b
234-243	all	RWn	Reserved Controls: Coded 00h
244	7	RWv	Mask High TX Bias Current Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0
244	6	RWv	Mask Low TX Bias Current Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0
244	5-4	RWv	Reserved
244	3	RWv	Mask High TX Bias Current Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0
244	2	RWv	Mask Low TX Bias Current Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0
244	1-0	RWv	Reserved
245	7	RWv	Mask High TX Bias Current Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0
245	6	RWv	Mask Low TX Bias Current Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0
245	5-4	RWv	Reserved
245	3	RWv	Mask High TX Bias Current Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0
245	2	RWv	Mask Low TX Bias Current Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0
245	1-0	RWv	Reserved
246	7	RWv	Mask High TX Bias Current Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0
246	6	RWv	Mask Low TX Bias Current Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0
246	5-4	RWv	Reserved
246	3	RWv	Mask High TX Bias Current Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0
246	2	RWv	Mask Low TX Bias Current Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0
246	1-0	RWv	Reserved
247	7	RWv	Mask High TX Bias Current Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0
247	6	RWv	Mask Low TX Bias Current Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0
247	5-4	RWv	Reserved
247	3	RWv	Mask High TX Bias Current Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0
247	2	RWv	Mask Low TX Bias Current Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0
247	1-0	RWv	Reserved
248	7	RWv	Mask High TX Bias Current Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0
248	6	RWv	Mask Low TX Bias Current Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0
248	5-4	RWv	Reserved
248	3	RWv	Mask High TX Bias Current Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0
248	2	RWv	Mask Low TX Bias Current Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0
248	1-0	RWv	Reserved
249	7	RWv	Mask High TX Bias Current Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0
249	6	RWv	Mask Low TX Bias Current Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0
249	5-4	RWv	Reserved
249	3	RWv	Mask High TX Bias Current Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0
249	2	RWv	Mask Low TX Bias Current Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0
249	1-0	RWv	Reserved

Avago Technologies Confidential. Restricted under NDA

Address			
Byte	Bit	Type	Field Name/Description
250	7	RWv	Mask High TX Power Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0
250	6	RWv	Mask Low TX Power Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0
250	5-4	RWv	Reserved
250	3	RWv	Mask High TX Power Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0
250	2	RWv	Mask Low TX Power Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0
250	1-0	RWv	Reserved
251	7	RWv	Mask High TX Power Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0
251	6	RWv	Mask Low TX Power Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0
251	5-4	RWv	Reserved
251	3	RWv	Mask High TX Power Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0
251	2	RWv	Mask Low TX Power Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0
251	1-0	RWv	Reserved
252	7	RWv	Mask High TX Power Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0
252	6	RWv	Mask Low TX Power Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0
252	5-4	RWv	Reserved
252	3	RWv	Mask High TX Power Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0
252	2	RWv	Mask Low TX Power Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0
252	1-0	RWv	Reserved
253	7	RWv	Mask High TX Power Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0
253	6	RWv	Mask Low TX Power Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0
253	5-4	RWv	Reserved
253	3	RWv	Mask High TX Power Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0
253	2	RWv	Mask Low TX Power Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0
253	1-0	RWv	Reserved
254	7	RWv	Mask High TX Power Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0
254	6	RWv	Mask Low TX Power Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0
254	5-4	RWv	Reserved
254	3	RWv	Mask High TX Power Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0
254	2	RWv	Mask Low TX Power Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0
254	1-0	RWv	Reserved
255	7	RWv	Mask High TX Power Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0
255	6	RWv	Mask Low TX Power Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0
255	5-4	RWv	Reserved
255	3	RWv	Mask High TX Power Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0
255	2	RWv	Mask Low TX Power Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0
255	1-0	RWv	Reserved

Transmitter Input Equalization Control Code Description

Control registers 228 through 233 permit input equalization control. Four bit code blocks (either bits 7 through 4 or 3 through 0 where bit 7 or 3 is the MSB) are assigned to each channel. Codes 1xxx are reserved.[1] Code 0111 calls for full scale equalization, code 0000 calls for no equalization, and intermediate code values provide intermediate levels of equalization.

The following table summarizes the normalized equalization setting effects (TX IC equalizer only)

EQ Setting		"111"	"110"	"101"	"100"	"011"	"010"	"001"	"000"
Peak vs. Midband	dB	16.7	13.9	11.6	8.8	6.1	3.9	2.2	0.4
Peak	dB	6.1	5.6	5	4.1	3.05	2.1	1.3	0.3
Midband	dB	-10.6	-8.3	-6.6	-4.7	-3.05	-1.8	-0.9	-0.1

Note:
1. Writes of 1xxxb are ignored by the module

Avago Technologies Confidential. Restricted under NDA

RX Memory Map 6ih Lower Page

Details of the base or lower page of the memory map for a receiver follow.

| Address | | | |
Byte	Bit	Type	Field Name/Description
0	all	RO	Type Identifier: Coded 00h for unspecified
1	all	RO	Reserved Status: Coded 00h
2	7-3	RO	Reserved: Coded 000000b
2	2	RO	LOS Status: Coded 1 when a LOS flag (bytes 9 and 10 of this page) is asserted for any channel, else 0. Clears when LOS flags are cleared.
2	1	RO	IntL Status: Coded 1 for asserted IntL. Clears to 0 when all flags including LOS are cleared.
2	0	RO	Data Not Ready: Coded 1 until data is available in monitor registers. Coded 0 in normal operation.
3 - 8	all	RO	Reserved Flags: Coded 00h
9	7-4	RO	Reserved: Coded 0000b
9	3	RO	LOS Latched RX Channel 11: Coded 1 when asserted, Latched, Clears on Read.
9	2	RO	LOS Latched RX Channel 10: Coded 1 when asserted, Latched, Clears on Read.
9	1	RO	LOS Latched RX Channel 9: Coded 1 when asserted, Latched, Clears on Read.
9	0	RO	LOS Latched RX Channel 8: Coded 1 when asserted, Latched, Clears on Read.
10	7	RO	LOS Latched RX Channel 7: Coded 1 when asserted, Latched, Clears on Read.
10	6	RO	LOS Latched RX Channel 6: Coded 1 when asserted, Latched, Clears on Read.
10	5	RO	LOS Latched RX Channel 5: Coded 1 when asserted, Latched, Clears on Read.
10	4	RO	LOS Latched RX Channel 4: Coded 1 when asserted, Latched, Clears on Read.
10	3	RO	LOS Latched RX Channel 3: Coded 1 when asserted, Latched, Clears on Read.
10	2	RO	LOS Latched RX Channel 2: Coded 1 when asserted, Latched, Clears on Read.
10	1	RO	LOS Latched RX Channel 1: Coded 1 when asserted, Latched, Clears on Read.
10	0	RO	LOS Latched RX Channel 0: Coded 1 when asserted, Latched, Clears on Read.
11-12	all	RO	Reserved: Coded 00h
13	7	RO	High Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
13	6	RO	Low Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
13	5-0	RO	Reserved
14	7	RO	High Internal 3.3 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
14	6	RO	Low Internal 3.3 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
14	5-4	RO	Reserved
14	3	RO	High Internal 2.5 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
14	2	RO	Low Internal 2.5 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.
14	1-0	RO	Reserved
15-21	all	RO	Reserved: Coded 00h
22	7	RO	High RX Power Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read.
22	6	RO	Low RX Power Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read.
22	5-4	RO	Reserved
22	3	RO	High RX Power Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read.
22	2	RO	Low RX Power Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read.
22	1-0	RO	Reserved
23	7	RO	High RX Power Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read.
23	6	RO	Low RX Power Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read.
23	5-4	RO	Reserved
23	3	RO	High RX Power Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read.
23	2	RO	Low RX Power Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read.
23	1-0	RO	Reserved

Avago Technologies Confidential. Restricted under NDA

Address			
Byte	Bit	Type	Field Name/Description
24	7	RO	High RX Power Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read.
24	6	RO	Low RX Power Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read.
24	5-4	RO	Reserved
24	3	RO	High RX Power Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read.
24	2	RO	Low RX Power Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read.
24	1-0	RO	Reserved
25	7	RO	High RX Power Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read.
25	6	RO	Low RX Power Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read.
25	5-4	RO	Reserved
25	3	RO	High RX Power Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read.
25	2	RO	Low RX Power Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read.
25	1-0	RO	Reserved
26	7	RO	High RX Power Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read.
26	6	RO	Low RX Power Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read.
26	5-4	RO	Reserved
26	3	RO	High RX Power Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read.
26	2	RO	Low RX Power Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read.
26	1-0	RO	Reserved
27	7	RO	High RX Power Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read.
27	6	RO	Low RX Power Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read.
27	5-4	RO	Reserved
27	3	RO	High RX Power Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read.
27	2	RO	Low RX Power Alarm Latched Channel 01: Coded 1 when asserted, Latched, Clears on Read.
27	1-0	RO	Reserved
28	all	RO	Internal Temperature Monitor MSB: Integer part coded in signed 2's complement. Tolerance is ±3° C.
29	all	RO	Internal Temperature Monitor LSB: Fractional part in units of 1°/256 coded in binary.
30-31	all	RO	Reserved: Coded 00h
32-33	all	RO	Internal 3.3 Vcc Monitor: Voltage in 100 μV units coded as 16 bit unsigned integer, Byte 32 is MSB. Tolerance is ±0.1 V.
34-35	all	RO	Internal 2.5 Vcc Monitor: Voltage in 100 μV units coded as 16 bit unsigned integer, Byte 34 is MSB. Tolerance is ±0.1 V.
36-63	all	RO	Reserved: Code 00h.
64-65	all	RO	RX Optical Input, PAVE, Monitor Channel 11: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 64 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
66-67	all	RO	RX Optical Input, PAVE, Monitor Channel 10: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 66 is MSB. Tolerance is ± 3 dB for -10 to +2.4 dBm range.
68-69	all	RO	RX Optical Input, PAVE, Monitor Channel 9: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 68 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
70-71	all	RO	RX Optical Input, PAVE, Monitor Channel 8: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 70 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
72-73	all	RO	RX Optical Input, PAVE, Monitor Channel 7: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 72 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
74-75	all	RO	RX Optical Input, PAVE, Monitor Channel 6: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 74 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
76-77	all	RO	RX Optical Input, PAVE, Monitor Channel 5: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 76 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
78-79	all	RO	RX Optical Input, PAVE, Monitor Channel 4: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 78 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.

Avago Technologies Confidential. Restricted under NDA

Address			
Byte	Bit	Type	Field Name/Description
80-81	all	RO	RX Optical Input, PAVE, Monitor Channel 3: Optical power in 0.1 µW units coded as 16 bit unsigned integer, Byte 80 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
82-83	all	RO	RX Optical Input, PAVE, Monitor Channel 2: Optical power in 0.1 µW units coded as 16 bit unsigned integer, Byte 82 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
84-85	all	RO	RX Optical Input, PAVE, Monitor Channel 1: Optical power in 0.1 µW units coded as 16 bit unsigned integer, Byte 84 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
86-87	all	RO	RX Optical Input, PAVE, Monitor Channel 0: Optical power in 0.1 µW units coded as 16 bit unsigned integer, Byte 86 is MSB. Tolerance is ±3 dB for -10 to +2.4 dBm range.
88-89	all	RO	Elapsed (Power-on) Operating Time: Elapsed time in 2 hour units coded as 16 bit unsigned integer, Byte 88 is MSB, Tolerance is ± 10%
90	all	RWn	Reserved: Coded 00h
91	7-1	RWv	Reserved: Coded 0000000b
91	0	RWv	Receiver Reset: Writing 1 return all registers except non-volatile RW to factory default values. Reads 0 after operation.
92	7-4	RWv	Reserved: Coded 0000b
92	3	RWv	RX Channel 11 Disable: Writing 1 deactivates the electrical output, Default is 0.
92	2	RWv	RX Channel 10 Disable: Writing 1 deactivates the electrical output, Default is 0.
92	1	RWv	RX Channel 9 Disable: Writing 1 deactivates the electrical output, Default is 0.
92	0	RWv	RX Channel 8 Disable: Writing 1 deactivates the electrical output, Default is 0.
93	7	RWv	RX Channel 7 Disable: Writing 1 deactivates the electrical output, Default is 0.
93	6	RWv	RX Channel 6 Disable: Writing 1 deactivates the electrical output, Default is 0.
93	5	RWv	RX Channel 5 Disable: Writing 1 deactivates the electrical output, Default is 0.
93	4	RWv	RX Channel 4 Disable: Writing 1 deactivates the electrical output, Default is 0.
93	3	RWv	RX Channel 3 Disable: Writing 1 deactivates the electrical output, Default is 0.
93	2	RWv	RX Channel 2 Disable: Writing 1 deactivates the electrical output, Default is 0.
93	1	RWv	RX Channel 1 Disable: Writing 1 deactivates the electrical output, Default is 0.
93	0	RWv	RX Channel 0 Disable: Writing 1 deactivates the electrical output, Default is 0.
94	7-4	RWv	Reserved: Coded 0000b
94	3	RWv	Squelch Disable Channel 11: Writing 1 inhibits squelch for the channel, Default is 0.
94	2	RWv	Squelch Disable Channel 10: Writing 1 inhibits squelch for the channel, Default is 0.
94	1	RWv	Squelch Disable Channel 9: Writing 1 inhibits squelch for the channel, Default is 0.
94	0	RWv	Squelch Disable Channel 8: Writing 1 inhibits squelch for the channel, Default is 0.
95	7	RWv	Squelch Disable Channel 7: Writing 1 inhibits squelch for the channel, Default is 0.
95	6	RWv	Squelch Disable Channel 6: Writing 1 inhibits squelch for the channel, Default is 0.
95	5	RWv	Squelch Disable Channel 5: Writing 1 inhibits squelch for the channel, Default is 0.
95	4	RWv	Squelch Disable Channel 4: Writing 1 inhibits squelch for the channel, Default is 0.
95	3	RWv	Squelch Disable Channel 3: Writing 1 inhibits squelch for the channel, Default is 0.
95	2	RWv	Squelch Disable Channel 2: Writing 1 inhibits squelch for the channel, Default is 0.
95	1	RWv	Squelch Disable Channel 1: Writing 1 inhibits squelch for the channel, Default is 0.
95	0	RWv	Squelch Disable Channel 0: Writing 1 inhibits squelch for the channel, Default is 0.
96	7-6	RWv	Rate Select Channel 11: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
96	5-4	RWv	Rate Select Channel 10: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
96	3-2	RWv	Rate Select Channel 9: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
96	1-0	RWv	Rate Select Channel 8: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00

Avago Technologies Confidential. Restricted under NDA

Address			
Byte	**Bit**	**Type**	**Field Name/Description**
97	7-6	RWv	Rate Select Channel 7: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
97	5-4	RWv	Rate Select Channel 6: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
97	3-2	RWv	Rate Select Channel 5: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
97	1-0	RWv	Rate Select Channel 4: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
98	7-6	RWv	Rate Select Channel 3: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
98	5-4	RWv	Rate Select Channel 2: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
98	3-2	RWv	Rate Select Channel 1: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
98	1-0	RWv	Rate Select Channel 0: Write 00 for max. BW (QDR 10 Gbps application), 01 for DDR and SDR BW (5 and 2.5 Gbps applications), rest reserved. Default is 00
99-105	all	RWv	Reserved: Coded 00h
106-111	all	RWv	Reserved: Coded 00h
112	7-4	RWv	Reserved: Coded 0000b
112	3	RWv	Mask LOS RX Channel 11: Writing 1 Prevents IntL generation, Default = 0
112	2	RWv	Mask LOS RX Channel 10: Writing 1 Prevents IntL generation, Default = 0
112	1	RWv	Mask LOS RX Channel 9: Writing 1 Prevents IntL generation, Default = 0
112	0	RWv	Mask LOS RX Channel 8: Writing 1 Prevents IntL generation, Default = 0
113	7	RWv	Mask LOS RX Channel 7: Writing 1 Prevents IntL generation, Default = 0
113	6	RWv	Mask LOS RX Channel 6: Writing 1 Prevents IntL generation, Default = 0
113	5	RWv	Mask LOS RX Channel 5: Writing 1 Prevents IntL generation, Default = 0
113	4	RWv	Mask LOS RX Channel 4: Writing 1 Prevents IntL generation, Default = 0
113	3	RWv	Mask LOS RX Channel 3: Writing 1 Prevents IntL generation, Default = 0
113	2	RWv	Mask LOS RX Channel 2: Writing 1 Prevents IntL generation, Default = 0
113	1	RWv	Mask LOS RX Channel 1: Writing 1 Prevents IntL generation, Default = 0
113	0	RWv	Mask LOS RX Channel 0: Writing 1 Prevents IntL generation, Default = 0
114-115	all	RWv	Reserved: Coded 00h
116	7	RWv	Mask Internal High Temperature Alarm: Writing 1 Prevents IntL generation, Default = 0
116	6	RWv	Mask Internal Low Temperature Alarm: Writing 1 Prevents IntL generation, Default = 0
116	5-0	RWv	Reserved
117	7	RWv	Mask Internal High 3.3 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0
117	6	RWv	Mask Internal Low 3.3 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0
117	5-4	RWv	Reserved
117	3	RWv	Mask Internal High 2.5 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0
117	2	RWv	Mask Internal Low 2.5 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0
117	1-0	RWv	Reserved
118-122	all	RWn	Reserved
123-126	all	RWv	Reserved: Coded 00h
127	all	RWv	Page Select Byte

RX Memory Map 00h Upper Page

Receiver serial ID page 00h entries and a description of the registers follow.

| Address | | Contents | | |
Byte	Bit	Code	Type	Field Name/Description
128	all	00h	RO	Type Identifier: Coded 00h for unspecified. See SFF-8472 for reference
129	all	00000000b	RO	Module Description: Coded for < 1.5 W
130	all	11000000b	RO	Required Power Supplies: Coded for 3.3 V and 2.5 V supplies
131	all	01010101b	RO	Max Short-Term Operating Case Temperature in °C: Coded for 85°C
132	all	00001100b	RO	Min Bit Rate in 100 Mb/s units: Coded for 1250 Mb/s
133	all	1100111b	RO	Max Bit Rate in 100 Mb/s units: Coded for 10312 Mb/s
134-135	all	00h	RO	Nominal Laser Wavelength (Wavelength in nm = value / 20): Coded 00h for RX
136-137	all	00h	RO	Wavelength deviation from nominal (tolerance in nm = ± value / 200): Coded 00h for RX
138	all	00101000b	RO	Supported Flags/Actions: Coded for RX LOS, Output Squelch for LOS, Alarm Flags
139	all	00110101b	RO	Supported Monitors: Coded for RX Input, Pave, Internal Temp, Elapsed Time
140	all	01100000b	RO	Supported Monitors: Coded for 3.3 V, 2.5 V
141	all	10101000b	RO	Supported Controls: Coded for Ch Disable, Squelch Disable, Rate Select
142	all	10100011b	RO	Supported Controls: Coded for RX Amplitude, RX De-emphasis, Ch Polarity Flip, Addressing
143	all	00h	RO	Supported Functions
144-151	all	00h	RO	Reserved
152-167	all	41h 56h 41h 47h 4Fh 20h 20h x10	RO	Vendor Name in ASCII: Coded "AVAGO" for Avago Technologies, Spaces (20h) for unused characters. Left justified.
168-170	all	00h 17h 6Ah	RO	Vendor OUI (IEEE ID): Coded "00h 17h 6Ah" for Avago Technologies
171-186	all	41h 46h 42h 52h 2Dh 38h 32h 31h 46h 4Eh 33h 5Ah 20h 20h 20h 20h	RO	Vendor Part Number in ASCII: "AFBR-821FN3Z " or : "AFBR-821RN3Z . Left justified with spaces (20h) for unused bytes
187-188	all	20h 20h	RO	Vendor Revision Number in ASCII: Coded with spaces (20h)
189-204	all		RO	Vendor Serial Number (ASCII): Varies by unit. Left justified with space (20h) for unused bytes
205-212	all		RO	Vendor Date Code YYYYMMDD (ASCII)
213-222	all		RO	Customer Specific Area.
223	all		RO	Check sum addresses 128 through 222
224-255	all		RO	Vendor Specific

RX Memory Map 01h Upper Page

Details of receiver upper page 01h follow.

Address			
Byte	**Bit**	**Type**	**Field Name/Description**
128	all	RO	Internal Temperature High Alarm Threshold MSB: Integer part coded in signed 2's complement
129	all	RO	Internal Temperature High Alarm Threshold LSB: Fractional part in units of 1°/256 coded in binary.
130	all	RO	Internal Temperature Low Alarm Threshold MSB: Integer part coded in signed 2's complement
131	all	RO	Internal Temperature Low Alarm Threshold LSB: Fractional part in units of 1°/256 coded in binary.
132-143	all	RO	Reserved
144-145	all	RO	Internal 3.3 Vcc High Alarm Threshold: Voltage in 100 µV units coded as 16 bit unsigned integer, low address is MSB.
146-147	all	RO	Internal 3.3 Vcc Low Alarm Threshold: Voltage in 100 µV units coded as 16 bit unsigned integer, low address is MSB.
148-151	all	RO	Reserved
152-153	all	RO	Internal 2.5 Vcc High Alarm Threshold: Voltage in 100 µV units coded as 16 bit unsigned integer, low address is MSB.
154-155	all	RO	Internal 2.5 Vcc Low Alarm Threshold: Voltage in 100 µV units coded as 16 bit unsigned integer, low address is MSB.
156-175	all	RO	Module Thresholds Reserved: Coded 00h
176-183	all	RO	Channel Thresholds Reserved: Coded 00h
184-185	all	RO	RX Optical Power All Channels High Alarm Threshold: Optical power in 0.1 µW units coded as 16 bit unsigned integer, low address is MSB.
186-187	all	RO	RX Optical Power All Channels Low Alarm Threshold: Optical power in 0.1 µW units coded as 16 bit unsigned integer, low address is MSB.
188-223	all	RO	Thresholds Reserved: Coded 00h
224	all	RO	Check sum: Low order 8 bits of the sum of all bytes from 128 through 223 inclusive
225	7-1	RWn	Reserved: Coded 0000000b
225	0	RWn	IntL Pulse/Static Option: Writing 1 sets IntL to Static mode, Default is 1 for Static mode
226	7-4	RWn	Reserved: Coded 0000b
226	3	RWn	Output Polarity Flip Channel 11: Writing 1 inverts truth of the differential output pair, Default is 0.
226	2	RWn	Output Polarity Flip Channel 10: Writing 1 inverts truth of the differential output pair, Default is 0.
226	1	RWn	Output Polarity Flip Channel 9: Writing 1 inverts truth of the differential output pair, Default is 0.
226	0	RWn	Output Polarity Flip Channel 8: Writing 1 inverts truth of the differential output pair, Default is 0.
227	7	RWn	Output Polarity Flip Channel 7: Writing 1 inverts truth of the differential output pair, Default is 0.
227	6	RWn	Output Polarity Flip Channel 6: Writing 1 inverts truth of the differential output pair, Default is 0.
227	5	RWn	Output Polarity Flip Channel 5: Writing 1 inverts truth of the differential output pair, Default is 0.
227	4	RWn	Output Polarity Flip Channel 4: Writing 1 inverts truth of the differential output pair, Default is 0.
227	3	RWn	Output Polarity Flip Channel 3: Writing 1 inverts truth of the differential output pair, Default is 0.
227	2	RWn	Output Polarity Flip Channel 2: Writing 1 inverts truth of the differential output pair, Default is 0.
227	1	RWn	Output Polarity Flip Channel 1: Writing 1 inverts truth of the differential output pair, Default is 0.
227	0	RWn	Output Polarity Flip Channel 0: Writing 1 inverts truth of the differential output pair, Default is 0.
228	7-4	RWn	RX Output Amplitude Control: Channel 11. See Code Description on page 50. Default = 0100b
228	3-0	RWn	RX Output Amplitude Control: Channel 10. See Code Description on page 50. Default = 0100b
229	7-4	RWn	RX Output Amplitude Control: Channel 9. See Code Description on page 50. Default = 0100b
229	3-0	RWn	RX Output Amplitude Control: Channel 8. See Code Description on page 50. Default = 0100b
230	7-4	RWn	RX Output Amplitude Control: Channel 7. See Code Description on page 50. Default = 0100b
230	3-0	RWn	RX Output Amplitude Control: Channel 6. See Code Description on page 50.Default = 0100b

Address			
Byte	**Bit**	**Type**	**Field Name/Description**
231	7-4	RWn	RX Output Amplitude Control: Channel 5. See Code Description on page 50. Default = 0100b
231	3-0	RWn	RX Output Amplitude Control: Channel 4. See Code Description on page 50. Default = 0100b
232	7-4	RWn	RX Output Amplitude Control: Channel 3. See Code Description on page 50. Default = 0100b
232	3-0	RWn	RX Output Amplitude Control: Channel 2. See Code Description on page 50. Default = 0100b
233	7-4	RWn	RX Output Amplitude Control: Channel 1. See Code Description on page 50. Default = 0100b
233	3-0	RWn	RX Output Amplitude Control: Channel 0. See Code Description on page 50. Default = 0100b
234	7-4	RWn	RX Output De-emphasis Control: Channel 11. See Code Description on page 50. Default = 0011b
234	3-0	RWn	RX Output De-emphasis Control: Channel 10. See Code Description on page 50. Default = 0011b
235	7-4	RWn	RX Output De-emphasis Control: Channel 9. See Code Description on page 50. Default = 0011b
235	3-0	RWn	RX Output De-emphasis Control: Channel 8. See Code Description on page 50. Default = 0011b
236	7-4	RWn	RX Output De-emphasis Control: Channel 7. See Code Description on page 50. Default = 0011b
236	3-0	RWn	RX Output De-emphasis Control: Channel 6. See Code Description on page 50. Default = 0011b
237	7-4	RWn	RX Output De-emphasis Control: Channel 5. See Code Description on page 50. Default = 0011b
237	3-0	RWn	RX Output De-emphasis Control: Channel 4. See Code Description on page 50. Default = 0011b
238	7-4	RWn	RX Output De-emphasis Control: Channel 3. See Code Description on page 50. Default = 0011b
238	3-0	RWn	RX Output De-emphasis Control: Channel 2. See Code Description on page 50. Default = 0011b
239	7-4	RWn	RX Output De-emphasis Control: Channel 1. See Code Description on page 50. Default = 0011b
239	3-0	RWn	RX Output De-emphasis Control: Channel 0. See Code Description on page 50. Default = 0011b
240-243	all	RWn	Reserved Controls: Coded 00h
244-249	all	RWv	Reserved Masks: Coded 00h
250	7	RWv	Mask High RX Power Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0
250	6	RWv	Mask Low RX Power Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0
250	5-4	RWv	Reserved
250	3	RWv	Mask High RX Power Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0
250	2	RWv	Mask Low RX Power Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0
250	1-0	RWv	Reserved
251	7	RWv	Mask Bt High RX Power Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0
251	6	RWv	Mask Low RX Power Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0
251	5-4	RWv	Reserved
251	3	RWv	Mask High RX Power Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0
251	2	RWv	Mask Low RX Power Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0
251	1-0	RWv	Reserved
252	7	RWv	Mask High RX Power Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0
252	6	RWv	Mask Low RX Power Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0
252	5-4	RWv	Reserved
252	3	RWv	Mask High RX Power Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0
252	2	RWv	Mask Low RX Power Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0
252	1-0	RWv	Reserved
253	7	RWv	Mask High RX Power Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0
253	6	RWv	Mask Low RX Power Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0
253	5-4	RWv	Reserved
253	3	RWv	Mask High RX Power Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0
253	2	RWv	Mask Low RX Power Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0
253	1-0	RWv	Reserved

Address			
Byte	Bit	Type	Field Name/Description
254	7	RWv	Mask High RX Power Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0
254	6	RWv	Mask Low RX Power Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0
254	5-4	RWv	Reserved
254	3	RWv	Mask High RX Power Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0
254	2	RWv	Mask Low RX Power Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0
254	1-0	RWv	Reserved
255	7	RWv	Mask High RX Power Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0
255	6	RWv	Mask Low RX Power Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0
255	5-4	RWv	Reserved
255	3	RWv	Mask High RX Power Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0
255	2	RWv	Mask Low RX Power Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0
255	1-0	RWv	Reserved

Receiver Output Amplitude Control Code Description

Control registers 228 through 233 permit output signal peak amplitude selection. Four bit code blocks (either bits 7 through 4 or 3 through 0 where bit 7 or 3 is the MSB) are assigned to each channel. Codes 1xxx are reserved. Code 0111 calls for full scale peak signal amplitude and code 0000 calls for minimum signal amplitude. See table below for receiver output amplitude control settings.

Code	Receiver Output Amplitude – Default De-emphasis				Reference
	Min	Nom	Max	Units	
1xxxb					Reserved
0111b	640	800	960	mVppd	Full Scale
0110b	560	700	840	mVppd	
0101b	480	600	720	mVppd	
0100b	400	500	600	mVppd	Default setting
0011b	320	400	480	mVppd	
0010b	240	300	360	mVppd	
0001b	150	200	250	mVppd	
0000b	70	100	130	mVppd	

Receiver Output De-emphasis Control Code Description

Control registers 234 through 239 permit output de-emphasis selection. Four bit code blocks (either bits 7 through 4 or 3 through 0 where bit 7 or 3 is the MSB) are assigned to each channel. Codes 1xxx are reserved.[1] Code 0111 calls for full scale, 100% de-emphasis and code 0000 calls for no de-emphasis. Intermediate code values yield intermediate de-emphasis levels. The total dynamic range of de-emphasis control is 6 dB.

Note:
1. Writes of 1xxxb are ignored by the module

Code	De-emphasis %	Reference
1xxxb		Reserved
0111b	100	Full Scale
0110b		
0101b		
0100b		
0011b		Default setting
0010b		
0001b		
0000b	0	

Serial ID 00h Upper Page Description

Description of Serial ID page 00h codes follows.

Byte 128 Module Type

Address		Field Name/Description
Byte	Code	Module Type
128		Type Identifier: See SFF-8472 for reference, also SFP and XFP MSA, Coded 00h if unspecified.

Byte 129 Module Description

Address			
Byte	Bit	Code	Field Name/Description
129	7-6	00b	Power Class 1: Module Power Consumption < 1.5 W
	7-6	01b	Power Class 2: Module Power Consumption < 2.0 W
	7-6	10b	Power Class 3: Module Power Consumption < 2.5 W
	7-6	11b	Power Class 4: Module Power Consumption < 3.5 W
	5		Coded 1 for TX CDR provided; else coded 0
	4		Coded 1 for RX CDR provided; else coded 0
	3		Coded 1 for Required Reference Clock; else coded 0
	2		Coded 1 for Page 02 provided; else coded 0
	1		Coded 1 for Controlled Launch Transmitter (TIA 492AAAC); else coded 0
	0		Reserved

Byte 130 Module Description: Required Power Supplies

Address			
Byte	Bit	Code	Field Name/Description
130	7		3.3 V, Coded 1 if required, else coded 0.
	6		2.5 V, Coded 1 if required, else coded 0.
	5		1.8 V, Coded 1 if required, else coded 0.
	4		Vo Supply, Coded 1 if required, else coded 0.
	3		Variable Supply, Coded 1 if required, else coded 0.
	2-0		Reserved

Byte 131 Module Description: Max Recommended Operating Case Temperature

Address		Field Name/Description
Byte	Code	Module Type
131		Max Tc = binary value x 1.0° C

Byte 132 Module Description Min Signal Rate per channel

Address		Field Name/Description
Byte	Code	Module Type
132	00h	Unknown/unspecified
	rest	Min Signal Rate = binary value x 100 Mb/s

Byte 133 Module Description Max Signal Rate per channel

Address		Field Name/Description
Byte	Code	Module Type
133	00h	Unknown/unspecified Min Signal Rate = binary value x 100 Mb/s

Byte 134 - 137 Module Description Wavelength and Tolerance

Address		Field Name/Description
Byte	Code	Module Type
134-135		Nominal Center Wavelength: Wavelength in nm = binary value / 20, Coded 00b if unspecified/unused.
136-137		Wavelength Tolerance: Tolerance in nm = ± binary value / 200, Coded 00b if unspecified/unused.

Byte 138 Supported Functions – Flags/Actions

Address			
Byte	Bit	Code	Field Name/Description
138	7		Coded 1 for TX Fault Flag provided, else coded 0
	6		Coded 1 for TX LOS Flag provided, else coded 0
	5		Coded 1 for RX LOS Flag provided, else coded 0
	4		Coded 1 for CDR LOL Flag provided, else coded 0
	3		Coded 1 for Output Squelch for LOS provided, else coded 0
	2		Coded 1 for Monitor Alarm and Warning Flags provided, coded 0 for Monitor Alarm Flags provided
	1-0		Reserved

Byte 139 – 140 Supported Functions – Monitors

Address			
Byte	Bit	Code	Field Name/Description
139	7		Coded 1 for TX Bias Monitor, else coded 0
139	6		Coded 1 for TX LOP Monitor, else coded 0
139	5		Coded 1 for individual RX Input Power Monitors, coded 0 for single-channel or group monitor[1]
139	4		Coded 1 for RX Input Power reported as Pave, coded 0 for reported as OMA 21
139	3		Coded 1 for Case Temperature Monitor, else coded 0
139	2		Coded 1 for Internal Temperature Monitor, else coded 0
139	1		Coded 1 for Peak Temperature Monitor, else coded 0
139	0		Coded 1 for Elapsed Time Monitor, else coded 0
140	7		Coded 1 for BER Monitor, else coded 0
140	6		Coded 1 for Internal 3.3 V Vcc Monitor, else coded 0
140	5		Coded 1 for Internal 2.5 V Vcc Monitor, else coded 0
140	4		Coded 1 for Internal 1.8 V Vcc Monitor, else coded 0
140	3		Coded 1 for Internal Vo Vcc Monitor, else coded 0
140	2		Coded 1 for TEC current Monitor, else coded 0
140	1-0		Reserved

Note:
1. Address bit not applicable to TX modules, which will be coded with 0.

Byte 141 Supported Functions – Controls

Address			
Byte	Bit	Code	Field Name/Description
141	7-6	00	Channel Disable Control not provided/unspecified
	7-6	01	Global Channel Disable Control implemented
	7-6	10	Individual and independent Channel Disable Control implemented
	7-6	11	Reserved
	5-4	00	Squelch Disable Control not provided/unspecified
	5-4	01	Global Squelch Disable Control implemented
	5-4	10	Individual and independent Channel Squelch Control implemented
	5-4	11	Reserved
	3-2	00	Rate Select Control not provided/unspecified
	3-2	01	Global Rate Select Control implemented
	3-2	10	Individual and independent Rate Select Control implemented
	3-2	11	Reserved
	1-0	00	TX Input Equalization Control not provided/unspecified
	1-0	01	Global TX Input Equalization Control implemented
	1-0	10	Individual and independent TX Input Equalization Control implemented
	1-0	11	Reserved

Byte 142 Supported Functions – Controls

Address			
Byte	Bit	Code	Field Name/Description
142	7-6	00	RX Output Amplitude Control not provided/unspecified
	7-6	01	Global RX Output Amplitude Control implemented
	7-6	10	Individual and independent RX Output Amplitude Control implemented
	7-6	11	Reserved
	5-4	00	RX Output De-emphasis Control not provided/unspecified
	5-4	01	Global RX Output De-emphasis Control implemented
	5-4	10	Individual and independent RX Output De-emphasis Control implemented
	5-4	11	Reserved
	3		Coded 1 for TX Margin Mode provided, else coded 0
	2		Coded 1 for Channel Reset Control provided, else coded 0
	1		Coded 1 for Channel Polarity Flip Control provided, else coded 0
	0		Coded 1 for Module Addressing Control provided, else coded 0

Avago Technologies Confidential. Restricted under NDA

Byte 143 Supported Functions

Address		Code	Field Name/Description
Byte	Bit		
143	7		Coded 1 for FEC Control, else coded 0
	6		Coded 1 for PEC Control, else coded 0
	5		Coded 1 for JTAG Control, else coded 0
	4		Coded 1 for AC-JTAG Control, else coded 0
	3		Coded 1 for BIST, else coded 0
	2		Coded 1 for TEC Temperature Control, else coded 0
	1		Coded 1 for Sleep/Sensor Mode Set Control provided, else coded 0
	0		Coded 1 for CDR Bypass Control provided, else coded 0

Byte144 – 151 Reserved

Address		Field Name/Description
Byte	Code	Module Type
144-151		Reserved: Coded 00h

Byte 152 – 221 Vendor Information

Address		Code	Field Name/Description
Byte	Bit		
152-167			Vendor Name ASCII – 16 bytes. Left justified with space (20h) for unused bytes
168-170			Vendor OUI – 3 bytes; Unspecified where coded all zeroes
171-186			Vendor Part Number ASCII – 16 bytes. Left justified with space (20h) for unused bytes
187-188			Vendor Revision Number ASCII – 2 bytes
189-204			Vendor Serial Number ASCII – 16 bytes. Left justified with space (20h) for unused bytes
205-212			Vendor Date Code ASCII – 8 bytes; coded YYYYMMDD
213-222			Customer Specific Area – 10 bytes; Left justified with space (20h) for unused bytes

Byte 223 Check Sum for bytes 128 through 222

Address		Field Name/Description
Byte	Code	Module Type
223		Check Code – 1 byte: Low order 8 bits of the sum of all bytes from 128 through 222 inclusive.

Byte 224 – 255 Vendor Specific

Address		Code	Field Name/Description
Byte	Bit		
224-239			
240-253			Vendor Specific – 14 bytes
254-255	All		Reserved

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

Avago
T E C H N O L O G I E S

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for foxconn *manufacturer:*

Other Similar products are found below :

AFBR-709DMZ JPD1030-N521-4F 2EGL4997-B2DM-4F AFCT-57F3ATMZ AFBR-57R6AEZ 3H993921-4M41-02H DZ11A51-H8R1-4F AFCT-739ASMZ 3H993321-4M41-01H DT00151-H1A2-4F AFBR-89CEDZ UH51543-BW11-7F 2EG14917-D2D8-4F JFM38U11-B313-4F LU25683-A001-9H UEA11121-8FS6-4F LD1807F-S54TD UB11123-8Z4-7F AS0B226-S99Q-7H 2EG08217-D2D-DF WNMEL00-84N00-EH AFBR-5715APZ HM3512E-P2 DT10121-H4W2-4F AS0A621-HARN-7H AS0A621-HASN-7H AFBR-79EIPZ-F5 AFCT-5961ATLZ AS0A621-H2S6-7H ASAA821-EARB0-7H WQ21823-DES1-7F ABCU-5740ARZ AS0BC21-S40BE-7H AFBR-5715PZ AFBR-59R5LZ AFBR-57R5APZ AFBR-57R6APZ UEA1112C-4HK1-4H AS0B326-S78N-7F