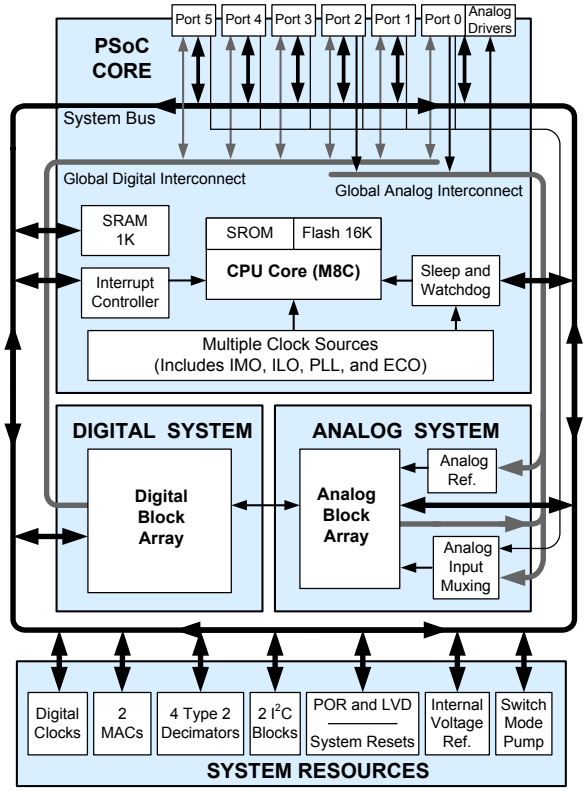
CY8C28243/CY8C28403/CY8C28413
CY8C28433/CY8C28445/CY8C28452
CY8C28513/CY8C28545
CY8C28623/CY8C28643/CY8C28645

PSoC® Programmable System-on-Chip™

Features

- Varied resource options within one PSoC® device group
- Powerful Harvard-architecture processor
  - M8C processor speeds up to 24 MHz
  - 8 × 8 Multiply, 32-bit accumulate
  - Low power at high speed
  - Operating voltage: 3.0 V to 5.25 V
  - Operating voltages down to 1.5 V Using on-chip switched mode pump (SMP)
  - Industrial temperature range: –40 °C to +85 °C
- Advanced reconfigurable peripherals (PSoC Blocks)
  - Up to 12 rail-to-rail analog PSoC blocks provide:
    - Up to 14-bit ADCs
    - Up to 9-bit DACs
    - Programmable gain amplifiers
    - Programmable filters and comparators
    - Multiple ADC configurations
    - Dedicated SAR ADC, up to 142 ksps with sample and hold
    - Up to 4 synchronized or independent delta-sigma ADCs for advanced applications
  - Up to 4 limited type E analog blocks provide:
    - Dual channel capacitive sensing capability
    - Comparators with programmable DAC reference
    - Up to 10-bit single-slope ADCs
  - Up to 12 digital PSoC blocks provide:
    - 8- to 32-bit timers and counters, 8- and 16-bit pulse-width modulators (PWMs)
    - Shift register, CRC, and PRS modules
    - Up to 3 full-duplex UARTs
    - Up to 6 half-duplex UARTs
    - Multiple variable data length SPI™ masters or slaves
    - Connectable to all GPIOs
  - Complex peripherals by combining blocks
- Precision, programmable clocking
  - Internal ±2.5% 24/48 MHz main oscillator
  - Optional 32.768 kHz crystal for precise on-chip clocks
  - Optional external oscillator, up to 24 MHz
  - Internal low speed, low power oscillator for watchdog and sleep functionality
- Flexible on-chip memory
  - 16 KB flash program storage 50,000 erase/write cycles
  - 1-KB SRAM data storage
  - In-system serial programming (ISSP™)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Programmable Pin configurations
  - 25 mA sink, 10 mA drive on all GPIOs
  - Pull-up, pull-down, high Z, strong, or open-drain drive modes on all GPIOs
  - Analog input on all GPIOs
  - 30 mA analog outputs on GPIOs
  - Configurable interrupt on all GPIOs
- Additional system resources
  - Up to two hardware I^2C resources
    - Each resource implements slave, master, or multi-master modes
    - Operation between 0 and 400 kHz
  - Watchdog and Sleep timers
  - User-configurable low voltage detection
  - Flexible internal voltage references
  - Integrated supervisory circuit
  - On-chip precision voltage reference
- Complete development tools
  - Free development software (PSoC Designer™)
  - Full featured in-circuit emulator, and programmer
  - Full speed emulation
  - Flexible and functional breakpoint structure
  - 128 KB trace memory

Logic Block Diagram



Contents

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

Note: For CY8C28xxx devices related Application note please click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C28xxx devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

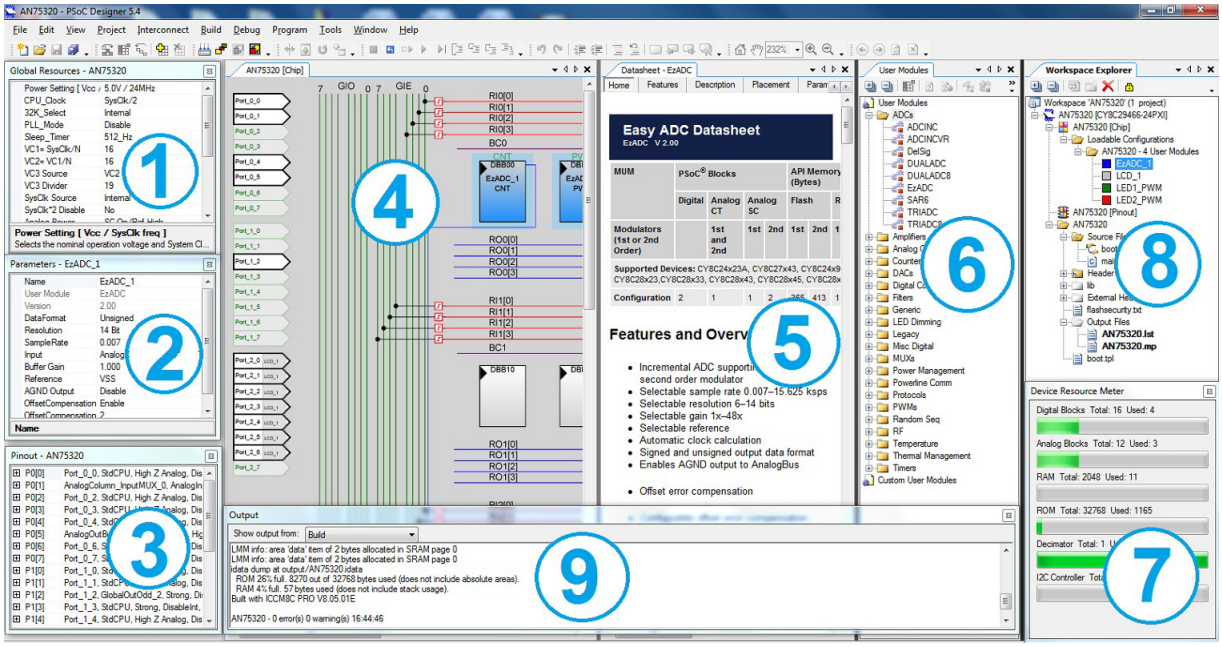
PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



PSoC Functional Overview

The PSoC family consists of many devices with On-Chip Controllers. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog blocks, digital blocks, and interconnections. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. In addition, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The CY8C28xxx group of PSoC devices described in this datasheet have multiple resource configuration options available. Therefore, not every resource mentioned in this datasheet is available for each CY8C28xxx subgroup. The CY8C28x45 subgroup has a full feature set of all resources described. There are six more segmented subgroups that allow designers to use a device with only the resources and functionality necessary for a specific application. See Table 2 on page 9 to determine the resources available for each CY8C28xxx subgroup. The same information is also presented in more detail in the Ordering Information section.

The architecture for this specific PSoC device family, as shown in the Logic Block Diagram on page 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. The configurable global bus system allows all the device resources to be combined into a complete custom system. PSoC CY8C28xxx family devices have up to six I/O ports that connect to the global digital and analog interconnects, providing access to up to 12 digital blocks and up to 16 analog blocks.

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general Purpose I/O (GPIO). The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microcontroller.

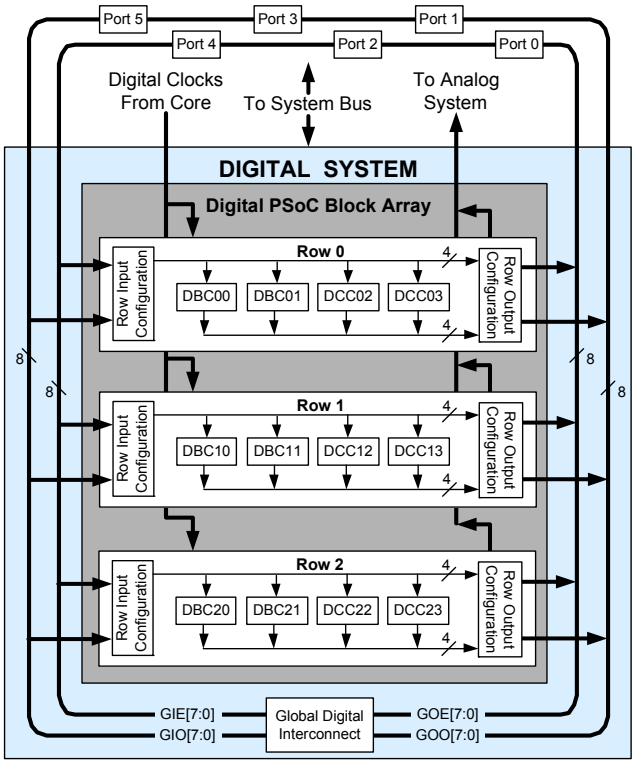
Memory encompasses 16K bytes of Flash for program storage, 1K bytes of SRAM for data storage. The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 2.5% over temperature and voltage. A low power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and watch dog timer (WDT). The 32.768 kHz external crystal oscillator (ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL.

PSoC GPIOs provide connections to the CPU, and digital and analog resources. Each pin's drive mode may be selected from 8 options, which allows great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of up to 12 configurable digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to create 8, 16, 24, and 32-bit peripherals, which are called user modules. The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin.

Figure 2. Digital System Block Diagram[1]



Digital peripheral configurations include:

- PWMs (8- and 16-bit, One-shot and Multi-shot capability)
- PWMs with Dead band/Kill (8- and 16-bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- Full-duplex 8-bit UARTs (up to 3) with selectable parity
- Half-duplex 8-bit UARTs (up to 6) with selectable parity
- Variable length SPI slave and master
  - Up to 6 total slaves and masters (8-bit)
  - Supports 8 to 16 bit operation
- I^2C slave, master, or multi-master (up to 2 available as System Resources)
- IrDA (up to 3)
- Pseudo Random Sequence Generators (8 to 32 bit)
- Cyclical Redundancy Checker/Generator (16 bit)
- Shift Register (2 to 32 bit)

Note
1. CY8C28x52 devices do not have digital block row 2. They have two digital rows with eight total digital blocks.

The Analog System

The Analog System is composed of up to 16 configurable analog blocks, each containing an opamp circuit that allows the creation of complex analog signal flows. Some devices in this PSoC family have an analog multiplex bus that can connect to every GPIO pin. This bus can also connect to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing.

Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (6 to 14-bit resolution, up to 4, selectable as Incremental or Delta Sigma)
- Dedicated 10-bit SAR ADC with sample rates up to 142 ksps
- Synchronized, simultaneous Delta Sigma ADCs (up to 4)
- Filters (2 to 8 pole band-pass, low pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 6, with 16 selectable thresholds)
- DACs (up to 4, with 6 to 9-bit resolution)
- Multiplying DACs (up to 4, with 6 to 9-bit resolution)
- High current output drivers (up to 4 with 30 mA drive)
- 1.3 V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Figure 3. Analog System Block Diagram for CY8C28x45 and CY8C28x52 Devices

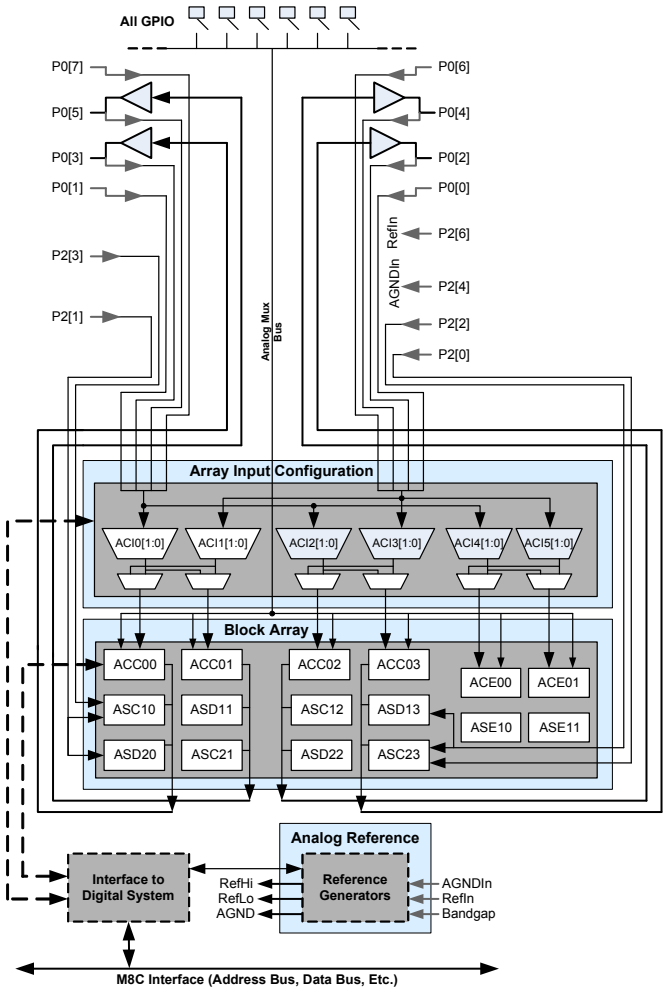


Figure 4. Analog System Block Diagram for CY8C28x43 Devices

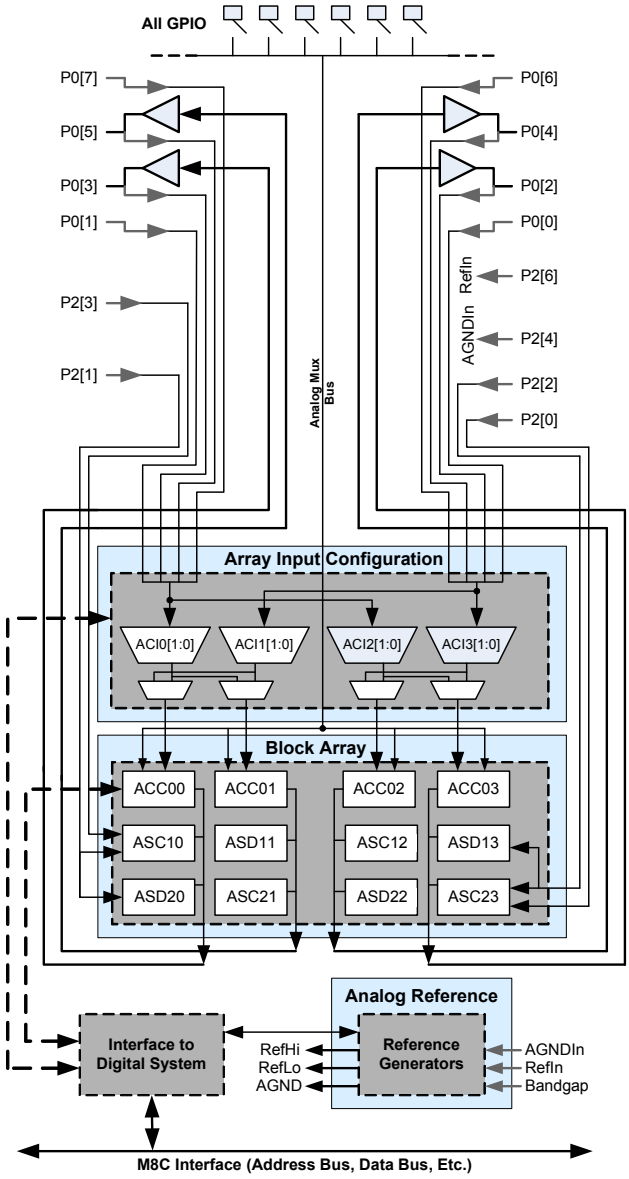


Figure 5. Analog System Block Diagram for CY8C28x33 Devices

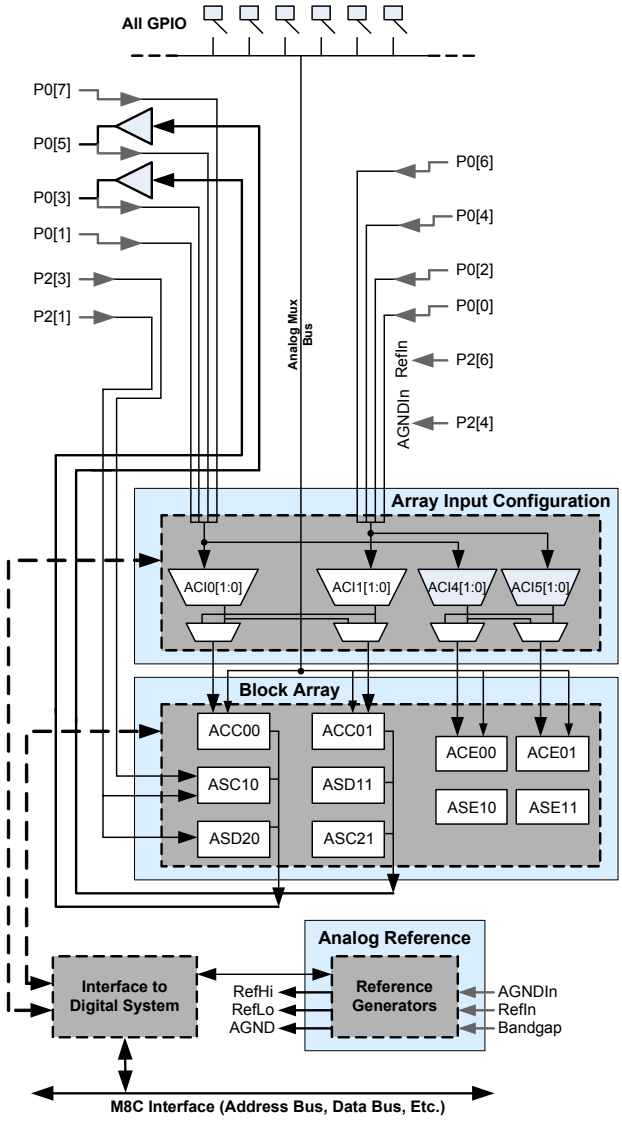


Figure 6. Analog System Block Diagram for CY8C28x23 Devices

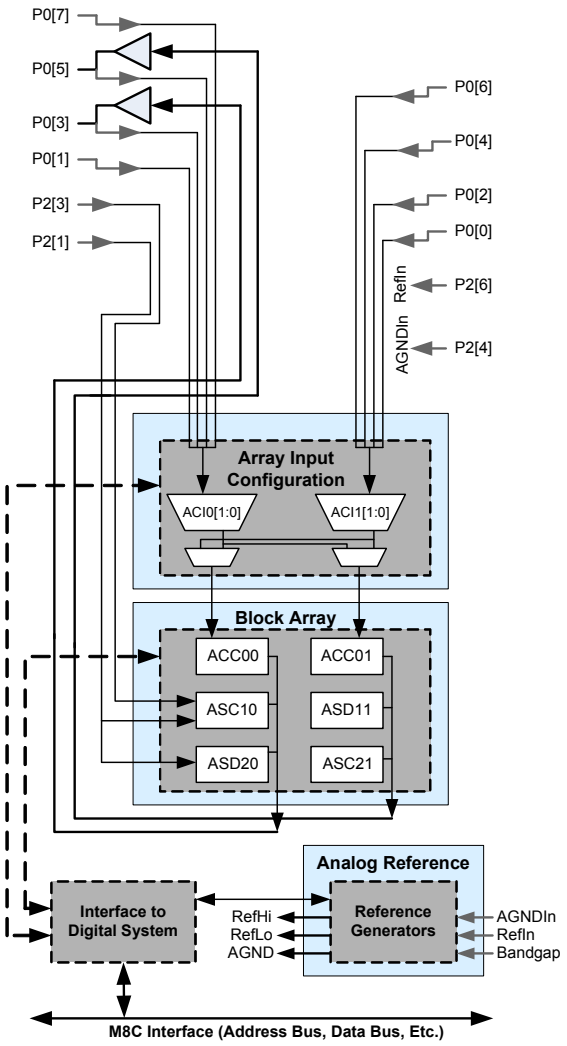
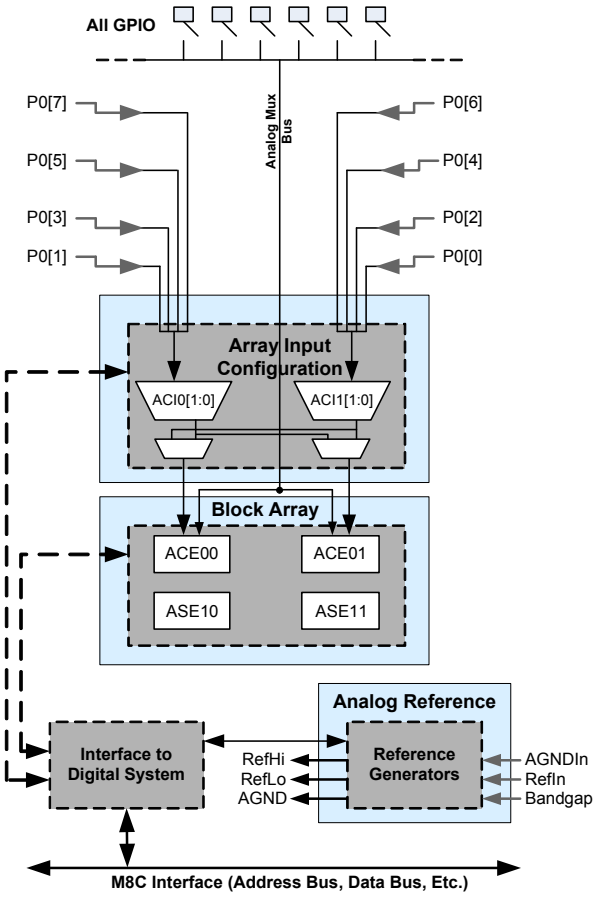


Figure 7. Analog System Block Diagram for CY8C28x13 Devices



System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, multiple decimators, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- Up to four decimators provide custom hardware filters for digital signal processing applications such as Delta-Sigma ADCs and CapSense capacitive sensor measurement.
- Up to two I^2C resources provide 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported. I^2C resources have hardware address detection capability.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.5 V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in this table.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[2]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[2]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[2]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[2]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[2]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[2,3]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[2,3]	up to 2 K	up to 32 K

Notes
2. Limited analog functionality.
3. Two analog blocks and one CapSense®.

The devices covered by this datasheet all have the same architecture, specifications, and ratings. However, the amount of some hardware resources varies from device to device within the group. The following table lists resources available for the specific device subgroups covered by this datasheet.

Table 2. CY8C28xxx Device Characteristics

PSoC Part Number	CapSense	Digital Blocks	Regular Analog Blocks	Limited Analog Blocks	HW I^2C	Decimators	Digital I/O	Analog Inputs	Analog Outputs	Analog Mux Buses
CY8C28x03	N	12	0	0	2	0	up to 24	up to 8	0	0
CY8C28x13	Y	12	0	4	1	2	up to 40	up to 40	0	2
CY8C28x23	N	12	6	0	2	2	up to 44	up to 10	2	0
CY8C28x33	Y	12	6	4	1	4	up to 40	up to 40	2	2
CY8C28x43	N	12	12	0	2	4	up to 44	up to 44	4	2
CY8C28x45	Y	12	12	4	2	4	up to 44	up to 44	4	2
CY8C28x52	Y	8	12	4	1	4	up to 24	up to 24	4	2

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pinouts

This section describes, lists, and illustrates the CY8C28xxx PSoC device pins and pinout configurations.

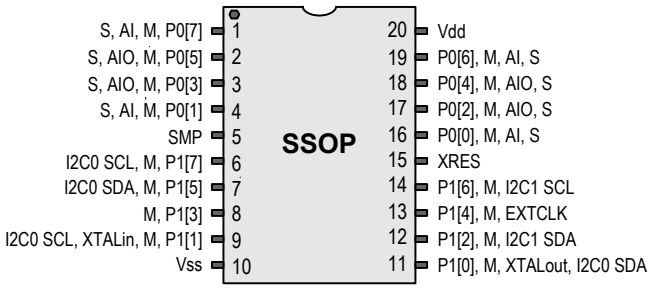
The CY8C28xxx PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

20-pin Part Pinout

Table 3. 20-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
5	Output		SMP	Switch Mode Pump (SMP) connection to external components.
6	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
7	I/O	M	P1[5]	I2C0 Serial Data (SDA).
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
10	Power		V_{SS}	Ground connection.
11	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
12	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
13	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
14	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
15	Input		XRES	Active high external reset with internal pull-down.
16	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
17	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
18	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
19	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
20	Power		V_{DD}	Supply voltage.

CY8C28243 20-pin PSoC Device



LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

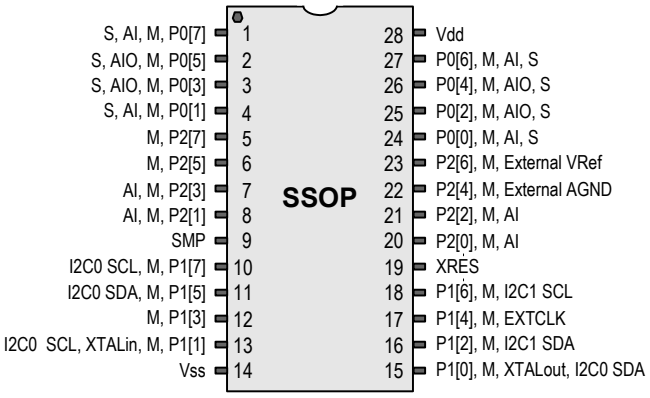
Notes
4. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices for details.
5. CY8C28x52 and CY8C28x23 devices do not have a SAR ADC. Therefore, this pin does not function as a SAR ADC input for these devices.
6. CY8C28x13 and CY8C28x03 devices do not have any analog output buffers. Therefore, this pin does not function as an analog column output for these devices.
7. CY8C28x52, CY8C28x13, and CY8C28x33 devices only have one I2C block. Therefore, this GPIO does not function as an I2C pin for these devices.
8. CY8C28x33, CY8C28x23, CY8C28x13, and CY8C28x03 devices do not have an analog output buffer for this pin. Therefore, this pin does not function as an analog column output for these devices.

28-pin Part Pinout

Table 4. 28-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	I, M	P2[3]	Direct switched capacitor block input.[9]
8	I/O	I, M	P2[1]	Direct switched capacitor block input.[9]
9	Output		SMP	Switch Mode Pump (SMP) connection to external components.
10	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
11	I/O	M	P1[5]	I2C0 Serial Data (SDA).
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
14	Power		V_{SS}	Ground connection.
15	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
16	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
17	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
18	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
19	Input		XRES	Active high external reset with internal pull-down.
20	I/O	I, M	P2[0]	Direct switched capacitor block input.[10]
21	I/O	I, M	P2[2]	Direct switched capacitor block input.[10]
22	I/O	M	P2[4]	External Analog Ground (AGND).
23	I/O	M	P2[6]	External Voltage Reference (VRef).
24	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
25	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
26	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
27	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
28	Power		V_{DD}	Supply voltage.

CY8C28403, CY8C28413, CY8C28433, CY8C28445, and CY8C28452 28-pin PSoC Devices



LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input

Notes
9. This pin is not a direct switched capacitor block analog input for CY8C28x03 and CY8C28x13 devices.
10. This pin is not a direct switched capacitor block analog input for CY8C28x03, CY8C28x13, CY8C28x23, and CY8C28x33 devices.

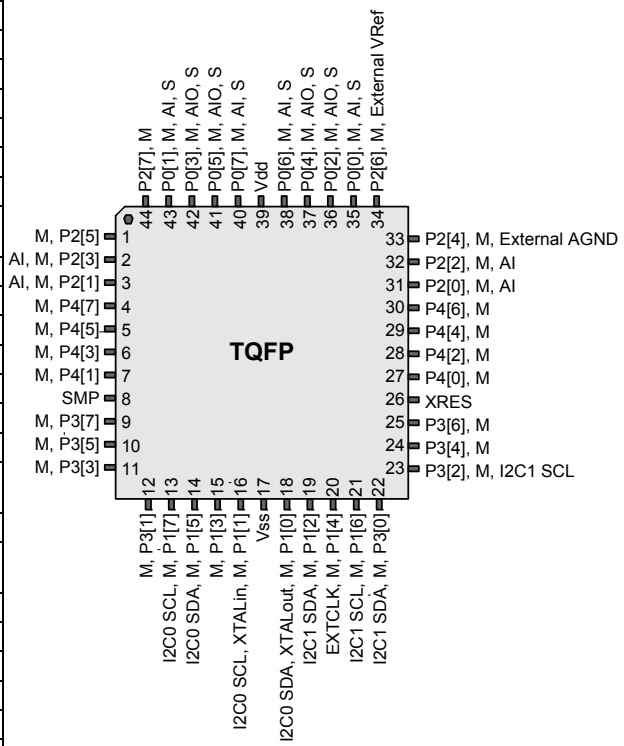
44-pin Part Pinout

Table 5. 44-pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	M	P2[5]	
2	I/O	I, M	P2[3]	Direct switched capacitor block input.[9]
3	I/O	I, M	P2[1]	Direct switched capacitor block input.[9]
4	I/O	M	P4[7]	
5	I/O	M	P4[5]	
6	I/O	M	P4[3]	
7	I/O	M	P4[1]	
8	Output		SMP	Switch Mode Pump (SMP) connection to external components.
9	I/O	M	P3[7]	
10	I/O	M	P3[5]	
11	I/O	M	P3[3]	
12	I/O	M	P3[1]	
13	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
14	I/O	M	P1[5]	I2C0 Serial Data (SDA).
15	I/O	M	P1[3]	
16	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
17	Power		V_{SS}	Ground connection.
18	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
19	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
20	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
21	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
22	I/O	M	P3[0]	I2C1 Serial Data (SDA).[7]
23	I/O	M	P3[2]	I2C1 Serial Clock (SCL).[7]
24	I/O	M	P3[4]	
25	I/O	M	P3[6]	
26	Input		XRES	Active high external reset with internal pull-down.
27	I/O	M	P4[0]	
28	I/O	M	P4[2]	
29	I/O	M	P4[4]	
30	I/O	M	P4[6]	
31	I/O	I, M	P2[0]	Direct switched capacitor block input.[10]
32	I/O	I, M	P2[2]	Direct switched capacitor block input.[10]
33	I/O	M	P2[4]	External Analog Ground (AGND).
34	I/O	M	P2[6]	External Voltage Reference (VRef).
35	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
36	I/O	I/O, M S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
37	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
38	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
39	Power		V_{DD}	Supply voltage.
40	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
41	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
42	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
43	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
44	I/O		P2[7]	

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

CY8C28513, and CY8C28545
44-pin PSoC Devices

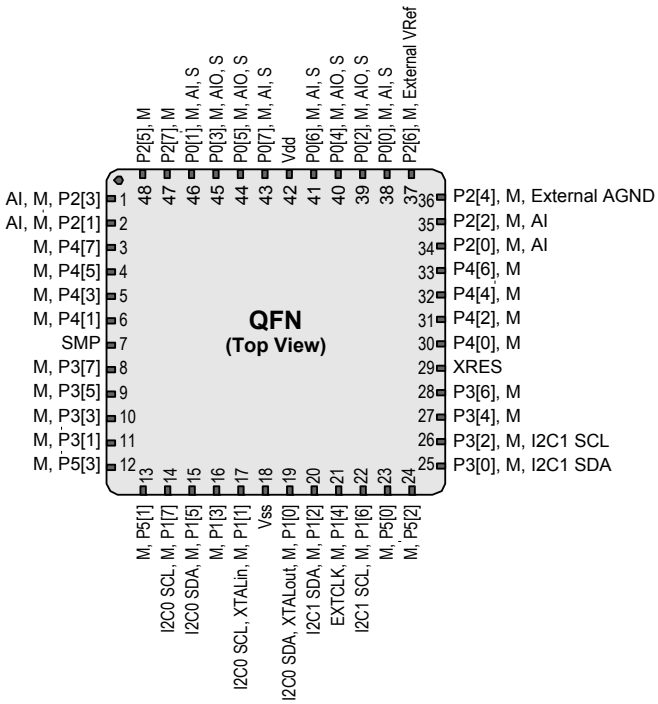


48-pin Part Pinout

Table 6. 48-pin Part Pinout (QFN[11])

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input.[9]
2	I/O	I, M	P2[1]	Direct switched capacitor block input.[9]
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	Output		SMP	Switch Mode Pump (SMP) connection to external components.
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[3]	
13	I/O	M	P5[1]	
14	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
15	I/O	M	P1[5]	I2C0 Serial Data (SDA).
16	I/O	M	P1[3]	
17	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
18	Power		V_{SS}	Ground connection.
19	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
20	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
21	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
22	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
23	I/O	M	P5[0]	
24	I/O	M	P5[2]	
25	I/O	M	P3[0]	I2C1 Serial Data (SDA).[7]
26	I/O	M	P3[2]	I2C1 Serial Clock (SCL).[7]
27	I/O	M	P3[4]	
28	I/O	M	P3[6]	
29	Input		XRES	Active high external reset with internal pull-down.
30	I/O	M	P4[0]	
31	I/O	M	P4[2]	
32	I/O	M	P4[4]	
33	I/O	M	P4[6]	
34	I/O	I, M	P2[0]	Direct switched capacitor block input.[10]
35	I/O	I, M	P2[2]	Direct switched capacitor block input.[10]
36	I/O	M	P2[4]	External Analog Ground (AGND).
37	I/O	M	P2[6]	External Voltage Reference (VRef).
38	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
39	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
40	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]

CY8C28623, CY8C28643, and CY8C28645
48-pin PSoC Devices



Pin No.	Type		Pin Name	Description
	Digital	Analog		
41	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
42	Power		V_{DD}	Supply voltage.
43	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
44	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
45	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
46	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
47	I/O	M	P2[7]	
48	I/O	M	P2[5]	

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

Note
11. The QFN package has a center pad that must be connected to ground (V_{SS})

56-pin Part Pinout

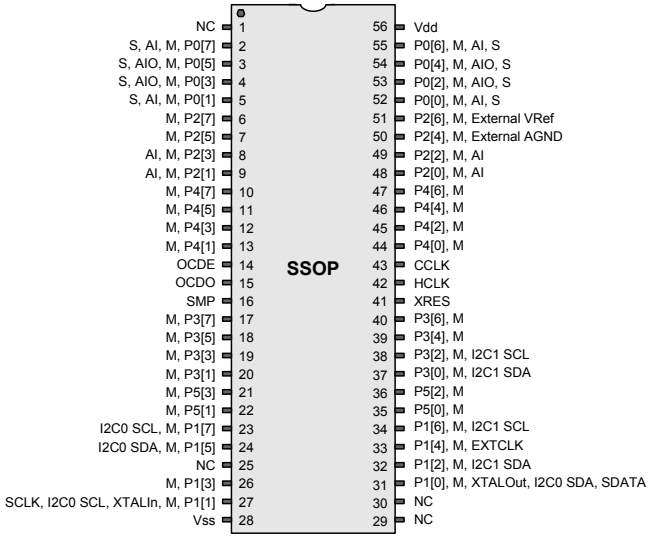
The 56-pin SSOP part is for the CY8C28000 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7. 56-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1			NC	No connection.
2	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.
3	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.
4	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.
5	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.
6	I/O	M	P2[7]	
7	I/O	M	P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input.
9	I/O	I	P2[1]	Direct switched capacitor block input.
10	I/O	M	P4[7]	
11	I/O	M	P4[5]	
12	I/O	I, M	P4[3]	
13	I/O	I, M	P4[1]	
14	OCD	M	OCDE	OCD even data I/O.
15	OCD	M	OCDO	OCD odd data output.
16	Output		SMP	Switch Mode Pump (SMP) connection to required external components.
17	I/O	M	P3[7]	
18	I/O	M	P3[5]	
19	I/O	M	P3[3]	
20	I/O	M	P3[1]	
21	I/O	M	P5[3]	
22	I/O	M	P5[1]	
23	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
24	I/O	M	P1[5]	I2C0 Serial Data (SDA).
25			NC	No connection.
26	I/O	M	P1[3]	
27	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
28	Power		V_{SS}	Ground connection.
29			NC	No connection.
30			NC	No connection.
31	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
32	I/O	M	P1[2]	I2C1 Serial Data (SDA).
33	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
34	I/O	M	P1[6]	I2C1 Serial Clock (SCL).
35	I/O	M	P5[0]	
36	I/O	M	P5[2]	
37	I/O	M	P3[0]	I2C1 Serial Data (SDA).
38	I/O	M	P3[2]	I2C1 Serial Clock (SCL).
39	I/O	M	P3[4]	
40	I/O	M	P3[6]	

CY8C28000 56-pin PSoC Device



Not for Production

Table 7. 56-pin Part Pinout (SSOP) *(continued)*

Pin No.	Type		Pin Name	Description
	Digital	Analog		
41	Input		XRES	Active high external reset with internal pull-down.
42	OCD	M	HCLK	OCD high speed clock output.
43	OCD	M	CCLK	OCD CPU clock output.
44	I/O	M	P4[0]	
45	I/O	M	P4[2]	
46	I/O	M	P4[4]	
47	I/O	M	P4[6]	
48	I/O	I, M	P2[0]	Direct switched capacitor block input.
49	I/O	I, M	P2[2]	Direct switched capacitor block input.
50	I/O	M	P2[4]	External Analog Ground (AGND).
51	I/O	M	P2[6]	External Voltage Reference (VRef).
52	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.
53	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.
54	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.
55	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.
56	Power		V_{DD}	Supply voltage.

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, M = Analog Mux Bus Input, and OCD = On-Chip Debug.

Register Reference

This section lists the registers of the CY8C28xxx PSoC devices. For detailed register information, reference the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices.

Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

CY8C28xxx PSoC devices have a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank of registers CPU instructions access. When the XIO bit is set the registers in Bank 1 are accessed by CPU instructions. When the XIO bit is cleared the registers in Bank 0 are accessed by CPU instructions.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 8. CY8C28x03 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#		80		RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W		81		RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW		82		RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#		83		RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#		84		RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W		85		RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW		86		RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#		87		RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
PRT4GS	12	RW		52			92			D2	
PRT4DM2	13	RW		53			93		IDX_PP	D3	RW
PRT5DR	14	RW		54			94		MVR_PP	D4	RW
PRT5IE	15	RW		55			95		MVW_PP	D5	RW
PRT5GS	16	RW		56			96		I2C0_CFG	D6	RW
PRT5DM2	17	RW		57			97		I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#		60			A0		INT_MSK0	E0	RW
DBC00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBC00DR2	22	RW		62			A2		INT_VC	E2	RC
DBC00CR0	23	#		63			A3		RES_WDT	E3	W
DBC01DR0	24	#		64			A4		I2C1_SCR	E4	#
DBC01DR1	25	W		65			A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW		66			A6			E6	
DBC01CR0	27	#	I2C1_DR	67	RW		A7			E7	
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RDI0RI	B0	RW		F0	
DBC10DR1	31	W		71		RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR0	33	#		73		RDI0LT0	B3	RW		F3	
DBC11DR0	34	#		74		RDI0LT1	B4	RW		F4	
DBC11DR1	35	W		75		RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR0	37	#		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 9. CY8C28x03 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51			91		GDI_E_IN	D1	RW
PRT4IC0	12	RW		52			92		GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94			D4	
PRT5DM1	15	RW		55			95			D5	
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW		60		GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW		61		GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW		62		GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW		63		GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW		64		RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW		E5	
DBC01OU	26	RW		66		RTC_S	A6	RW		E6	
DBC01CR1	27	RW		67		RTC_CR	A7	RW		E7	
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW		69		SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW		6A		SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW		EC	
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 10. CY8C28x13 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#		80		RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W		81		RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW		82		RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#		83		RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#		84		RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W		85		RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW		86		RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#		87		RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
PRT4GS	12	RW		52			92			D2	
PRT4DM2	13	RW		53			93		IDX_PP	D3	RW
PRT5DR	14	RW		54			94		MVR_PP	D4	RW
PRT5IE	15	RW		55			95		MVW_PP	D5	RW
PRT5GS	16	RW		56			96		I2C0_CFG	D6	RW
PRT5DM2	17	RW		57			97		I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#		60		DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW		62		DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#		63		DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#		64			A4			E4	
DBC01DR1	25	W		65			A5			E5	
DBC01DR2	26	RW		66			A6		DEC_CR0*	E6	RW
DBC01CR0	27	#		67			A7		DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RDI0RI	B0	RW		F0	
DBC10DR1	31	W		71		RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR0	33	#		73		RDI0LT0	B3	RW		F3	
DBC11DR0	34	#		74		RDI0LT1	B4	RW		F4	
DBC11DR1	35	W		75		RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR0	37	#		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 11. CY8C28x13 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C	RW		CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW		60		GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW		61		GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW		62		GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW		63		GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW		64		RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW		66		RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW		67		RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW		69		SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74	RW	RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 12. CY8C28x23 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4		I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#		A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW		A7		DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 13. CY8C28x23 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW		81		RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW		82		RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94	RW	DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A		DEC_CR5	9A	RW		DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW		E5	
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW		E6	
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW		E7	
DCC02FN	28	RW		68			A8		IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCC02OU	2A	RW		6A			AA		BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW		AB		ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW		71		RDI0SYN	B1	RW		F1	
DBC10OU	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 14. CY8C28x33 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 15. CY8C28x33 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 16. CY8C28x43 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#	ASC12CR0	88	RW		C8	
PRT2IE	09	RW	DCC22DR1	49	W	ASC12CR1	89	RW		C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW	ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#	ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW	DCC23DR0	4C	#	ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW	DCC23DR1	4D	W	ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW	ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC	I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC	I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW	DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 17. CY8C28x43 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW		E5	
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW		E6	
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW		E7	
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 18. CY8C28x45 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#	ASC12CR0	88	RW		C8	
PRT2IE	09	RW	DCC22DR1	49	W	ASC12CR1	89	RW		C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW	ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#	ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW	DCC23DR0	4C	#	ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW	DCC23DR1	4D	W	ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW	ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC	I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC	I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW	DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 19. CY8C28x45 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C	RW		CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 20. CY8C28x52 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 21. CY8C28x52 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43		ACE_AMD_CR1	83	RW		C3	
PRT1DM0	04	RW		44			84			C4	
PRT1DM1	05	RW		45		ACE_PWM_CR	85	RW		C5	
PRT1IC0	06	RW		46		ACE_ADC0_CR	86	RW		C6	
PRT1IC1	07	RW		47		ACE_ADC1_CR	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49		ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW		4A		ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW		4B		ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D		ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW		4E		ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW		4F		ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW		AA		BDG_TR	EA	RW
DCC02CR1	2B	RW		6B			AB		ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW		AC		MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW		71		RDI0SYN	B1	RW		F1	
DBC10OU	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

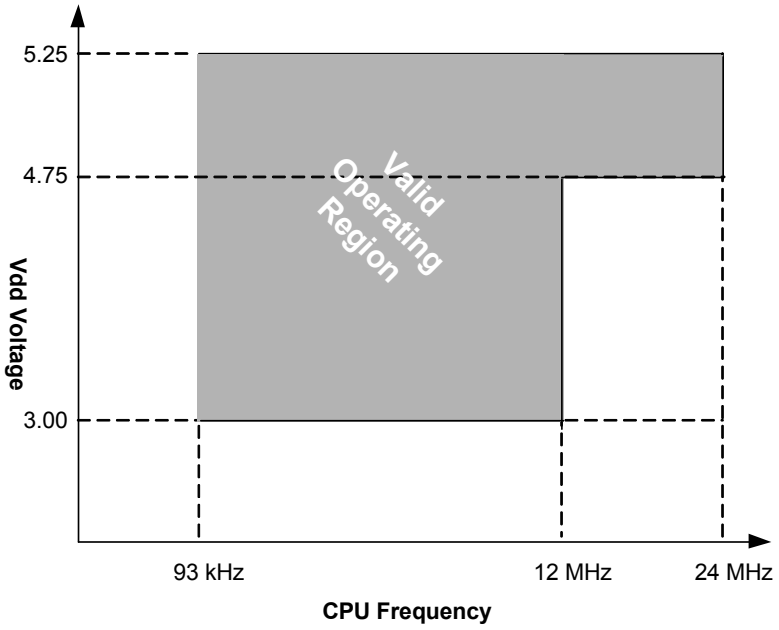
Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C28xxx PSoC devices. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http//www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications for devices running at greater than 12 MHz are valid for –40 °C ≤ T_A ≤ 70 °C and T_J ≤ 82 °C.

Figure 8. Voltage versus CPU Frequency



Absolute Maximum Ratings

Table 22. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See Package label	°C	
$t_{BAKETIME}$	Bake time	See package label	-	72	Hours	
T_A	Ambient temperature with power applied	-40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	-0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	-25	–	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	-50	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 23. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	-40	–	+85	°C	
T_J	Junction temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 72. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.00	–	5.25	V	
I_{DD}	Supply current	–	8	14	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DD3}	Supply current	–	5	9	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DDP}	Supply current when IMO = 6 MHz using SLIMO mode=1	–	2	3	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT.[12]	–	3	10	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C.
I_{SBH}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT at high temperature.[12]	–	4	25	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, sleep timer, WDT, and external crystal.[12]	–	4	13	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C.
I_{SBXTLH}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and external crystal at high temperature.[12]	–	5	26	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
I_{SBRTC}	Current consumed by RTC during sleep	–	0.5	1	µA	Extra current consumed by the RTC during sleep. This number is typical at 25 °C and 5 V.
V_{REF}	Reference voltage (Bandgap)	1.280	1.300	1.320	V	Trimmed for appropriate V_{DD}.
I_{SXRES}	Supply current with XRES asserted 5 V	–	0.65	3	mA	Max is peak current after XRES; Typical value is the steady state current value. T_A = 25 °C.
	Supply current with XRES asserted 3.3 V	-	0.4	1.5	mA	

Note
12. Standby (sleep) current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD} – 1.0 V, see the limitations of the total current in the note for V_{OH}.
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25.
V_{IH}	Input high level	2.1	–	–	V	V_{DD} = 3.0 to 5.25.
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 26. 5 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOACT}	Input Offset Voltage CT Block (absolute value) Power = Low, Opamp bias = High Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 1.6 1.3 1.2	 8 8 8	 mV mV mV	
V_{OSOA}	Input Offset Voltage SC and AGND Opamps (absolute value)	–	1	6	mV	Applies to High and Low Opamp bias.
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high Opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common Mode Rejection Ratio Power = Low Power = Medium Power = High	 60 60 60	 – – –	 – – –	 dB dB dB	
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	 60 60 80	 – – –	 – – –	 dB dB dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 200 400 700 1400 2400 4600	 300 600 1100 2000 3600 7700	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	60	–	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 27. 3.3 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOACT}	Input Offset Voltage CT Blocks (absolute value) Power = Low, Opamp bias = High Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 1.65 1.32 –	 8 8 –	 mV mV mV	
V_{OSOA}	Input Offset Voltage SC and AGND (absolute value)	–	1	6	mV	Applies to High and Low Opamp bias.
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common Mode Rejection Ratio Power = Low Power = Medium Power = High	 50 50 50	 – – –	 – – –	 dB dB dB	
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	 60 60 80	 – – –	 – – –	 dB dB dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High is 5 V only	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High	 – – –	 – – –	 0.2 0.2 0.2	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 200 400 700 1400 2400 4600	 300 600 1000 2000 3600 7500	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	50	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25\ V)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

DC Type-E Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of the Limited Type E Analog PSoC blocks.

Table 28. 5 V DC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	For 0.2 V < V_{IN} < V_{DD} – 1.2 V.
		–	2.5	20	mV	For V_{IN} = 0 to 0.2 V and V_{IN} > V_{DD} – 1.2 V.
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}[13]	Input leakage current (Port 0 Analog Pins)	–	200	–	nA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0.0	–	V_{DD}	V	
I_{SOA}	Amplifier supply current	–	10	30	µA	

Table 29. 3.3 V DC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	For 0.2 V < V_{IN} < V_{DD} – 1.2 V.
		–	2.5	20	mV	For V_{IN} = 0 to 0.2 V and V_{IN} > V_{DD} – 1.2 V.
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}[13]	Input leakage current (Port 0 Analog Pins)	–	200	–	nA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0	–	V_{DD}	V	
I_{SOA}	Amplifier supply current	–	10	30	µA	

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 30. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1	V	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	
I_{SLPC}	LPC supply current	–	10	40	µA	

Note
13. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. 5 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	20	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 0.5 × V_{DD} + 1.3 0.5 × V_{DD} + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.0) ≤ V_{OUT} ≤ (0.5 × V_{DD} + 0.9).

Table 32. 3.3 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	20	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 – –	 – –	 $0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	47	64	–	dB	$(0.5 \times V_{DD} - 1.0) \le V_{OUT} \le (0.5 \times V_{DD} + 0.9)$.

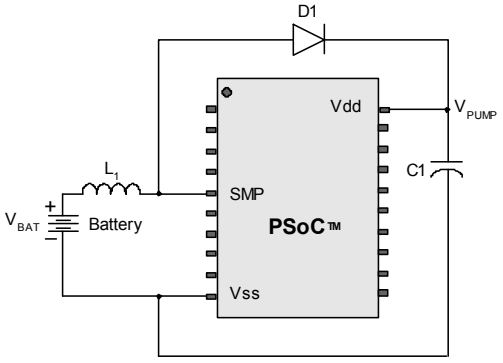
DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 33. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5 V	5 V output voltage	4.75	5.0	5.25	V	Configuration of footnote.[14] Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP} 3 V	3 V output voltage	3.00	3.25	3.60	V	Configuration of footnote.[14] Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
I_{PUMP}	Available output current V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V	 8 5	 – –	 – –	 mA mA	Configuration of footnote.[14] SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 5.0 V.
V_{BAT}5 V	Input voltage range from battery	1.8	–	5.0	V	Configuration of footnote.[14] SMP trip voltage is set to 5.0 V.
V_{BAT}3 V	Input voltage range from battery	1.5	–	3.3	V	Configuration of footnote.[14] SMP trip voltage is set to 3.25 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	2.6	–	–	V	Configuration of footnote.[14]
ΔV_{PUMP_Line}	Line regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configuration of footnote.[14] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 40 on page 52.
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configuration of footnote.[14] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 40 on page 52.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration of footnote.[14] Load is 5mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote.[14] Load is 5 mA. SMP trip voltage is set to 3.25 V.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Figure 9. Basic Switch Mode Pump Circuit



Note
14. L_1 = 2 µH inductor, C_1 = 10 µF capacitor, D_1 = Schottky diode. See Figure 9.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 34. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.214	$V_{DD}/2$ + 1.279	$V_{DD}/2$ + 1.341	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.018	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.01	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.301	$V_{DD}/2$ – 1.273	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 0.228	$V_{DD}/2$ + 1.284	$V_{DD}/2$ + 1.344	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.015	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.011	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.303	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.287	$V_{DD}/2$ + 1.345	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.276	V

Note
15. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.055	P2[4] + P2[6] – 0.019	P2[4] + P2[6] + 0.019	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.035	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.05	P2[4] + P2[6] – 0.015	P2[4] + P2[6] + 0.021	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.001	P2[4] – P2[6] + 0.031	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.048	P2[4] + P2[6] – 0.013	P2[4] + P2[6] + 0.022	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] – 0.001	P2[4] – P2[6] + 0.031	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.047	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.023	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.036	P2[4] – P2[6] – 0.002	P2[4] – P2[6] + 0.030	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.028	V_{DD} – 0.010	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.002	V_{DD}/2 + 0.012	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.008	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.021	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.001	V_{DD}/2 + 0.012	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.005	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.019	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.001	V_{DD}/2 + 0.012	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.004	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.017	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.001	V_{DD}/2 + 0.013	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.003	V

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b011	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	3 × Bandgap	3.736	3.887	4.030	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.598	2.667	V
		V_{REFLO}	Ref low	Bandgap	1.265	1.302	1.335	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	3 × Bandgap	3.747	3.894	4.034	V
		V_{AGND}	AGND	2 × Bandgap	2.528	2.601	2.668	V
		V_{REFLO}	Ref low	Bandgap	1.264	1.302	1.335	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	3 × Bandgap	3.749	3.897	4.035	V
		V_{AGND}	AGND	2 × Bandgap	2.529	2.602	2.668	V
		V_{REFLO}	Ref low	Bandgap	1.264	1.302	1.335	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	3 × Bandgap	3.751	3.899	4.037	V
		V_{AGND}	AGND	2 × Bandgap	2.530	2.603	2.669	V
		V_{REFLO}	Ref low	Bandgap	1.264	1.302	1.335	V
0b100	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.483 – P2[6]	2.578 – P2[6]	2.669 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.598	2.666	V
		V_{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.512 – P2[6]	2.602 – P2[6]	2.684 – P2[6]	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 – P2[6]	2.586 – P2[6]	2.673 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.528	2.601	2.668	V
		V_{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.510 – P2[6]	2.602 – P2[6]	2.685 – P2[6]	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.498 – P2[6]	2.589 – P2[6]	2.674 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.529	2.601	2.668	V
		V_{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.509 – P2[6]	2.601 – P2[6]	2.685 – P2[6]	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 – P2[6]	2.591 – P2[6]	2.675 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.530	2.603	2.669	V
		V_{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.508 – P2[6]	2.601 – P2[6]	2.686 – P2[6]	V

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.218	P2[4] + 1.283	P2[4] + 1.344	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.329	P2[4] – 1.297	P2[4] – 1.265	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.225	P2[4] + 1.287	P2[4] + 1.346	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.330	P2[4] – 1.301	P2[4] – 1.271	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.226	P2[4] + 1.288	P2[4] + 1.346	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.330	P2[4] – 1.302	P2[4] – 1.272	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.227	P2[4] + 1.289	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.303	P2[4] – 1.273	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.597	2.674	V
		V_{AGND}	AGND	Bandgap	1.263	1.302	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.014	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.508	2.595	2.675	V
		V_{AGND}	AGND	Bandgap	1.263	1.302	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.008	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.508	2.595	2.676	V
		V_{AGND}	AGND	Bandgap	1.263	1.302	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.005	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.508	2.596	2.677	V
		V_{AGND}	AGND	Bandgap	1.263	1.302	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.003	V

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b111	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	3.2 × Bandgap	4.056	4.155	4.222	V
		V_{AGND}	AGND	1.6 × Bandgap	2.012	2.083	2.168	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.01	V_{SS} + 0.035	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	3.2 × Bandgap	4.061	4.153	4.223	V
		V_{AGND}	AGND	1.6 × Bandgap	2.023	2.082	2.145	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.022	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	3.2 × Bandgap	4.063	4.154	4.224	V
		V_{AGND}	AGND	1.6 × Bandgap	2.020	2.083	2.152	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	3.2 × Bandgap	4.061	4.154	4.225	V
		V_{AGND}	AGND	1.6 × Bandgap	2.026	2.081	2.140	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V

Table 35. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.223	$V_{DD}/2$ + 1.283	$V_{DD}/2$ + 1.343	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.013	$V_{DD}/2$ – 0.003	$V_{DD}/2$ + 0.005	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.270	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.345	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.008	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.005	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.271	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.232	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.008	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.006	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.272	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.233	$V_{DD}/2$ + 1.291	$V_{DD}/2$ + 1.347	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.006	$V_{DD}/2$	$V_{DD}/2$ + 0.006	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.272	V

Table 35. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.045	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.016	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.019	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.023	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.036	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.013	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.021	P2[4] – P2[6] – 0.001	P2[4] – P2[6] + 0.021	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.034	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.013	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.023	P2[4] – P2[6] – 0.002	P2[4] – P2[6] + 0.016	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.033	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.014	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] – 0.003	P2[4] – P2[6] + 0.020	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.008	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.035	V_{DD}/2 – 0.001	V_{DD}/2 + 0.031	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.0165 V	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.035	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.031	V_{DD}/2 – 0.001	V_{DD}/2 + 0.028	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.012	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.044	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.052	V_{DD}/2	V_{DD}/2 + 0.046	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.014	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.036	V_{DD} – 0.004	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.032	V_{DD}/2	V_{DD}/2 + 0.029	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.012	V
0b011	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

Table 35. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.226	P2[4] + 1.286	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.323	P2[4] – 1.293	P2[4] –1.262	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.232	P2[4] + 1.29	P2[4] + 1.344	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.296	P2[4] – 1.267	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.233	P2[4] + 1.291	P2[4] + 1.345	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.298	P2[4] – 1.269	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.234	P2[4] + 1.292	P2[4] +1.345	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.299	P2[4] – 1.270	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.504	2.595	2.672	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.013	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.593	2.674	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.008	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.594	2.675	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.007	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.507	2.595	2.675	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.005	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 36. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.24	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 37. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	400	Ω	V_{DD} ≥ 3.0 V
R_{VSS}	Resistance of Initialization Switch to V_{SS}	–	–	800	Ω	

DC SAR10 ADC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 38. DC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
INL_{SAR10}	Integral nonlinearity for VREF ≥ 3 V	–2.5	–	2.5	LSB	10-bit resolution
	Integral nonlinearity for VREF < 3 V	–5	–	5	LSB	10-bit resolution
DNL_{SAR10}	Differential nonlinearity for VREF ≥ 3 V	–1.5	–	1.5	LSB	10-bit resolution
	Differential nonlinearity for VREF < 3 V	–4	–	4	LSB	10-bit resolution
I_{SAR10}	Active current consumption	0.08	0.5	0.497	mA	
$I_{VREFSAR10}$	Input current into P2[5] when configured as the SAR10 ADC's VREF input.	–	–	0.5	mA	The internal voltage reference buffer is disabled in this configuration.
$V_{VREFSAR10}$	Input reference voltage at P2[5] when configured as the SAR10 ADC's external voltage reference.	2.7	–	V_{DD} – 0.3 V	V	When VREF is buffered inside the SAR10 ADC, the voltage level at P2[5] (when configured as the external reference voltage) must always be at least 300 mV less than the chip supply voltage level on the V_{DD} pin. ($V_{VREFSAR10}$ < (V_{DD} – 300 mV)).
$V_{OSSAR10}$	Offset voltage	5	7.7	10	mV	
SAR_{IMP}	SAR input impedence	–	1.64	–	MΩ	Frequency dependant = 1/ Fs °C. 142.9 kHz (maximum) and Cin = 4.28 pF (typical)

DC IDAC Specifications

Table 39. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_INL	Integral nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_Gain	Gain per bit – Range 1 (91 µA)	283	357	447	nA	Measured at full scale
	Gain per bit – Range 2 (318 µA)	985	1250	1532	nA	
	Gain per bit – Range 3 (637 µA)	1959	2500	3056	nA	
IDACOffset	Offset at Code 0 vs LSB Ideal – Range 1 (91 µA)		2.0%	20%	%	Measured as a % of LSB (Current @ Code 0)/(LSB Ideal Current)
	Offset at Code 0 vs LSB Ideal – Range 2 (318 µA)		1.0%	10%	%	
	Offset at Code 0 vs LSB Ideal – Range 3 (637 µA)		1.0%	10%	%	

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices, for more information on the VLT_CR register.

Table 40. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} Value for PPOR Trip (positive ramp)					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0R}	PORLEV[1:0] = 00b	–	2.91	2.985	V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	4.49	V	
V_{PPOR2R}	PORLEV[1:0] = 10b	–	4.55	4.65	V	
	V_{DD} Value for PPOR Trip (negative ramp)					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.82	2.90	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	4.49	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.64	V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.83	2.91	3.00[16]	V	
V_{LVD1}	VM[2:0] = 001b	2.93	3.01	3.10	V	
V_{LVD2}	VM[2:0] = 010b	3.04	3.12	3.21	V	
V_{LVD3}	VM[2:0] = 011b	3.90	3.99	4.09	V	
V_{LVD4}	VM[2:0] = 100b	4.38	4.47	4.58	V	
V_{LVD5}	VM[2:0] = 101b	4.54	4.63	4.74[17]	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.71	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.80	4.92	V	
	V_{DD} Value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.93	3.01	3.10	V	
V_{PUMP1}	VM[2:0] = 001b	3.00	3.08	3.17	V	
V_{PUMP2}	VM[2:0] = 010b	3.16	3.24	3.33	V	
V_{PUMP3}	VM[2:0] = 011b	4.09	4.17	4.28	V	
V_{PUMP4}	VM[2:0] = 100b	4.53	4.62	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.61	4.71	4.82	V	
V_{PUMP6}	VM[2:0] = 110b	4.70	4.80	4.91	V	
V_{PUMP7}	VM[2:0] = 111b	4.88	4.98	5.10	V	

Notes
16. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
17. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 41. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	3	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply Voltage for Flash write operation	3	–	5.25	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.21	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000[18]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[19]	1,800,000	–	–	–	Erase/write cycles. Must be programmed and read at the same voltage to meet this.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Notes

18. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
19. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

DC I^2C Specifications

Table 42 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 42. DC I^2C Specifications[20]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V
V_{OLI2C}	Output low level	–	–	0.4	V	at sink current of 3 mA
		–	–	0.6	V	at sink current of 6 mA

Note
20. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 43. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6[21]	MHz	Trimmed. Utilizing factory trim values. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[21]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. SLIMO Mode = 1.
F_{CPU1}	CPU Frequency (5 V Nominal)	0.091	24	24.6[21]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F_{CPU2}	CPU Frequency (3.3 V Nominal)	0.091	12	12.3[22]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F_{BLK5}	Digital PSoC Block Frequency	0	–	49.2[21, 23]	MHz	4.75 V< V_{DD} <5.25 V
F_{BLK33}	Digital PSoC Block Frequency	0	24	24.6[23]	MHz	3.0 V<V_{DD}<3.6 V
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	Trimmed. Utilizing factory trim values.
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	Internal Low Speed Oscillator Untrimmed Frequency	5	–	100	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference manual for details on timing this.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Multiple (x732) of crystal frequency.
$t_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$t_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{DD} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.

Notes
21. 4.75 V < V_{DD} < 5.25 V.
22. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
23. See the individual user module datasheets for information on maximum frequencies for user modules.

Table 43. AC Chip-Level Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
t_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[24,25]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum Frequency of Signal on Row Input or Row Output.	–	–	12.3	MHz	
$SR_{POWERUP}$	Supply Ramp Time	0	–	–	µs	
$t_{POWERUP}$	Time for POR Release to Code Execution	–	16	100	ms	
t_{jit_IMO} [26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1300	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1300	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	200	800	ps	
t_{jit_PLL} [26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1100	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	400	2800	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	200	1400	ps	

Notes
24. 4.75 V < V_{DD} < 5.25 V.
25. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
26. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

Figure 10. PLL Lock Timing Diagram

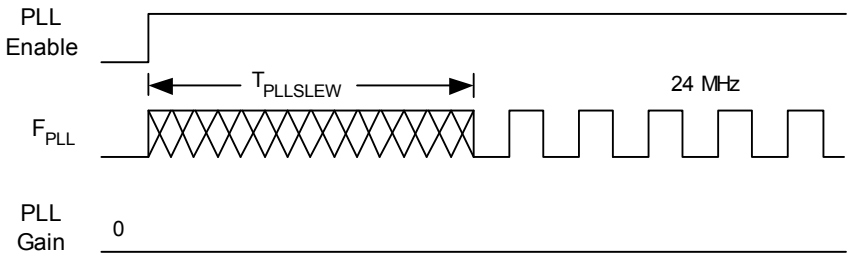


Figure 11. PLL Lock for Low Gain Setting Timing Diagram

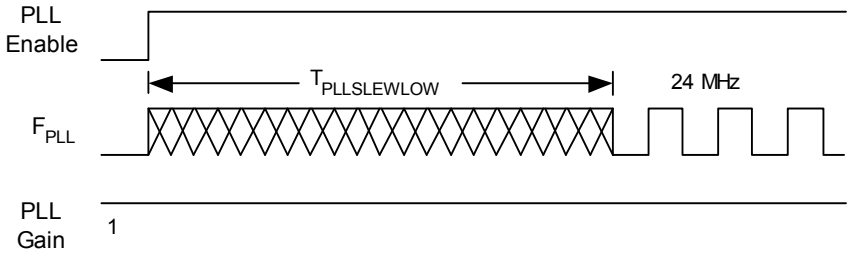
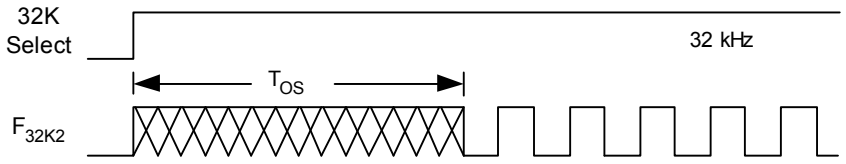


Figure 12. External Crystal Oscillator Startup Timing Diagram



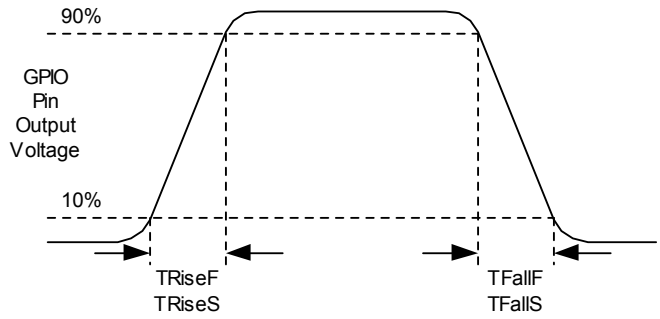
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 44. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
t_{RiseF}	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% – 90%
t_{FallF}	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% – 90%
t_{RiseS}	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% – 90%
t_{FallS}	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% – 90%

Figure 13. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp bias = High is not supported at 3.3 V.

Table 45. 5 V AC Operational Amplifier Specifications

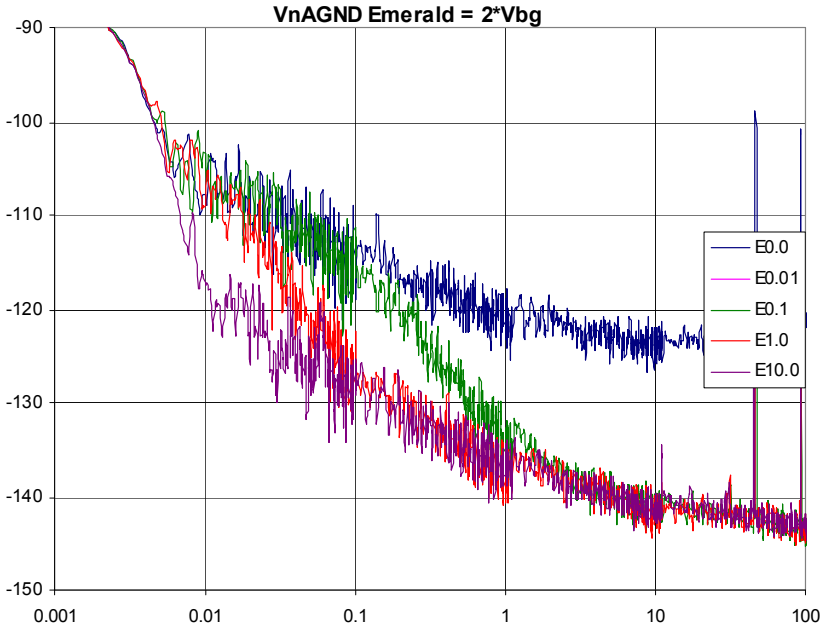
Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	
t_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	
SR_{FOA}	Falling Slew Rate (80% to 20%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	
E_{NOA}	Noise at 1 kHz Power = Medium, Opamp bias = High	–	100	–	nV/rt-Hz	

Table 46. 3.3 V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High	 – –	 – –	 3.92 0.72	 µs µs	
t_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 – –	 – –	 5.41 0.72	 µs µs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 0.31 2.7	 – –	 – –	 V/µs V/µs	
SR_{FOA}	Falling Slew Rate (80% to 20%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 0.24 1.8	 – –	 – –	 V/µs V/µs	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 0.67 2.8	 – –	 – –	 MHz MHz	
E_{NOA}	Noise at 1 kHz Power = Medium, Opamp bias = High	 –	 100	 –	 nV/rt-Hz	

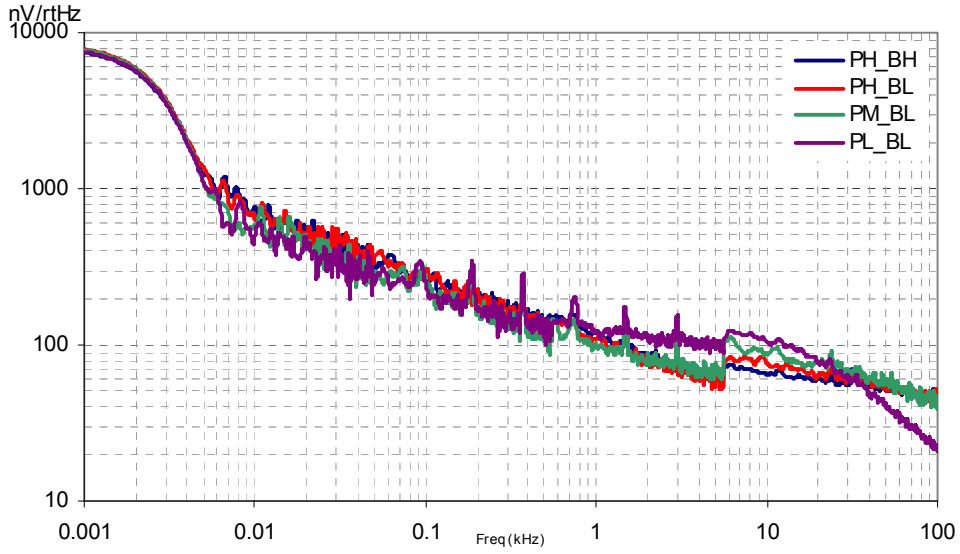
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 14. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 15. Typical Opamp Noise



AC Type-E Operational Amplifier Specifications

Table 47 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of the Limited Type E Analog PSoC blocks.

Table 47. AC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator Mode Response Time	–	75	100	ns	50 mV overdrive.

AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 48. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC Response Time	–	–	50	µs	≥ 50 mV overdrive.

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 49. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block Input Clock Frequency					
	V_{DD} ≥ 4.75 V	–	–	49	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	
Timer	Input Clock Frequency					
	No Capture, V_{DD} ≥ 4.75 V	–	–	49	MHz	
	No Capture, V_{DD} < 4.75 V	–	–	25	MHz	
	With Capture	–	–	25	MHz	
	Capture Pulse Width	50[27]	–	–	ns	
Counter	Input Clock Frequency					
	No Enable Input, V_{DD} ≥ 4.75 V	–	–	49	MHz	
	No Enable Input, V_{DD} < 4.75 V	–	–	25	MHz	
	With Enable Input	–	–	25	MHz	
	Enable Input Pulse Width	50[27]	–	–	ns	
Dead Band	Kill Pulse Width					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[27]	–	–	ns	
	Disable Mode	50[27]	–	–	ns	
	Input Clock Frequency					
	V_{DD} ≥ 4.75 V	–	–	49	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	
CRCPRS (PRS Mode)	Input Clock Frequency					
	V_{DD} ≥ 4.75 V	–	–	49	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	
CRCPRS (CRC Mode)	Input Clock Frequency	–	–	25	MHz	
SPIM	Input Clock Frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated Between Transmissions	50[13]	–	–	ns	
Tranmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 Stop Bits	–	–	49	MHz	
	V_{DD} ≥ 4.75 V, 1 Stop Bit	–	–	25	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 Stop Bits	–	–	49	MHz	
	V_{DD} ≥ 4.75 V, 1 Stop Bit	–	–	25	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	

Note
27. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 50. 5 V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	2.5	µs	
	Power = High	–	–	2.9	µs	
t_{SOB}	Falling Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	2.3	µs	
	Power = High	–	–	2.3	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1 V Step, 100 pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1 V Step, 100 pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	0.8	–	–	MHz	
	Power = High	0.8	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1 V$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	300	–	–	kHz	
	Power = High	300	–	–	kHz	

Table 51. 3.3 V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	3.8	µs	
	Power = High	–	–	3.8	µs	
t_{SOB}	Falling Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	3.2	µs	
	Power = High	–	–	2.9	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1 V Step, 100 pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1 V Step, 100 pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	0.64	–	–	MHz	
	Power = High	0.64	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1 V$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	200	–	–	kHz	
	Power = High	200	–	–	kHz	

AC SAR10 ADC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 52. AC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{INSAR10}$	Input clock frequency for SAR10 ADC	–	–	2.0	MHz	
F_{SSAR10}	Sample rate for SAR10 ADC SAR10 ADC Resolution = 10 bits	–	–	142.9	ksps	For 10-bit resolution, the sample rate is the ADC's input clock divided by 14.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 53. 5 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power-up IMO to Switch	150	–	–	µs	

Table 54. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1[28]	0.093	–	12.3	MHz	
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[29]	0.186	–	24.6	MHz	
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to Switch	150	–	–	µs	

Notes
28. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
29. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 55. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
t_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
t_{WRITE}	Flash Block Write Time	–	40	–	ms	
t_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	55	ns	$V_{DD} > 3.6$
t_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	75	ns	$3.0 \le V_{DD} \le 3.6$
$t_{ERASEALL}$	Flash Erase Time (Bulk)	–	40	–	ms	Erase all blocks and protection fields at once.
$t_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100[30]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200[30]	ms	–40 °C ≤ Tj ≤ 0 °C

Note
30. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note, AN2015 at http://ww.cypress.com under Application Notes for more information.

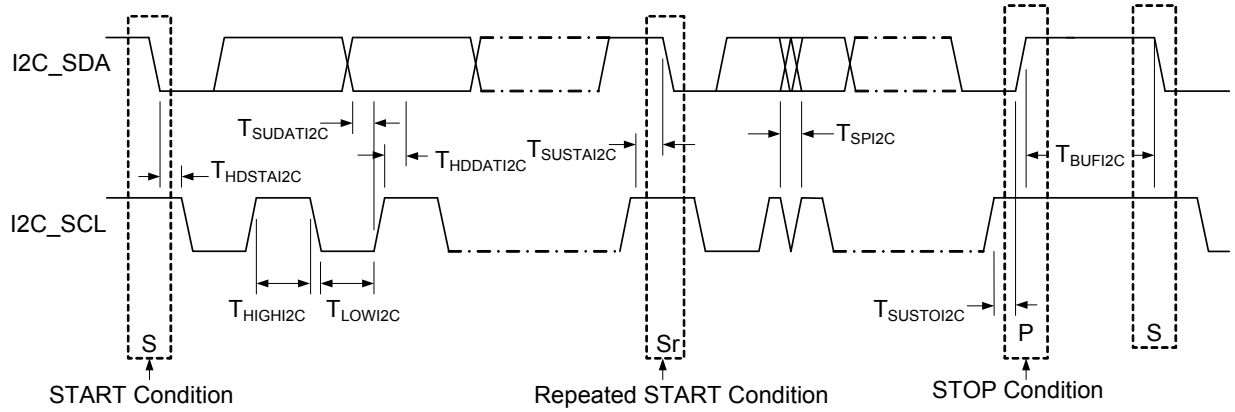
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 56. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$t_{SUDATI2C}$	Data setup time	250	–	100[31]	–	ns	
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 16. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

31. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

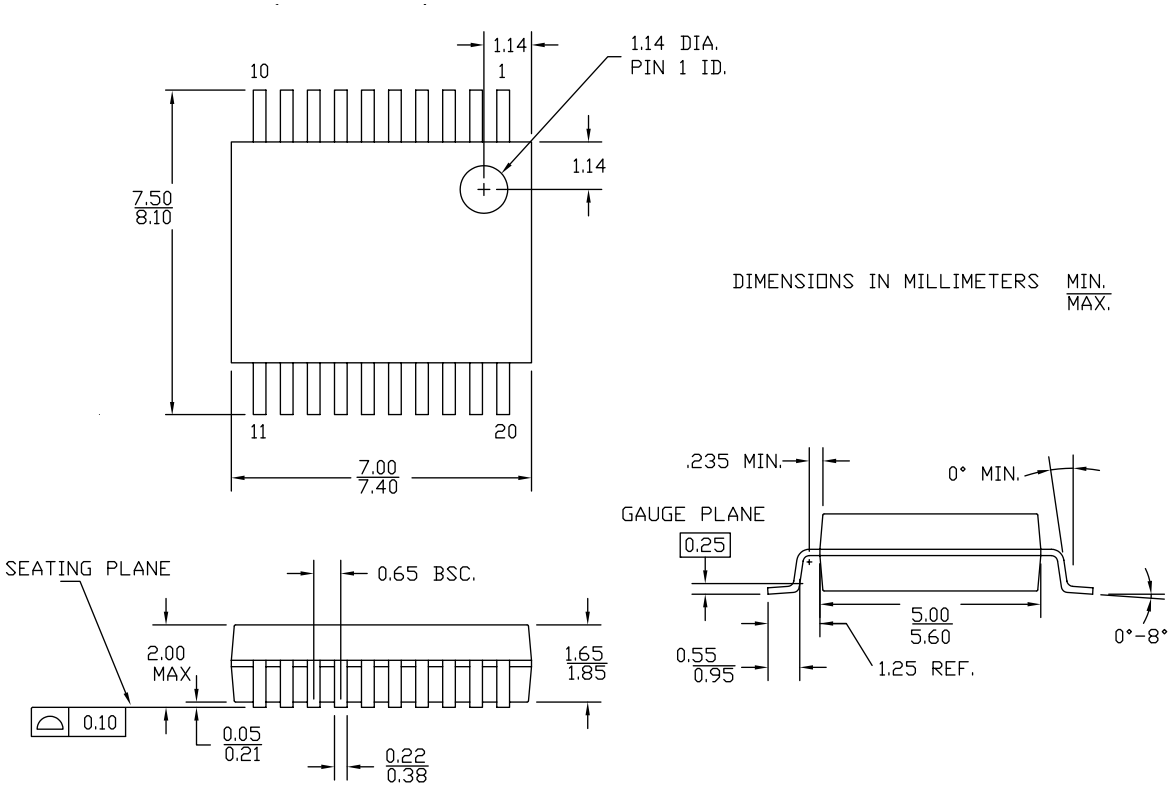
Packaging Information

This section illustrates the packaging specifications for the CY8C28xxx PSoC devices, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the Emulator Pod Dimension drawings at http://www.cypress.com.

Packaging Dimensions

Figure 17. 20-pin SSOP (210 Mils) Package Outline O20.21, 51-85077



51-85077 *F

Figure 18. 28-pin SSOP (210 Mils) O28.21 Package Outline, 51-85079

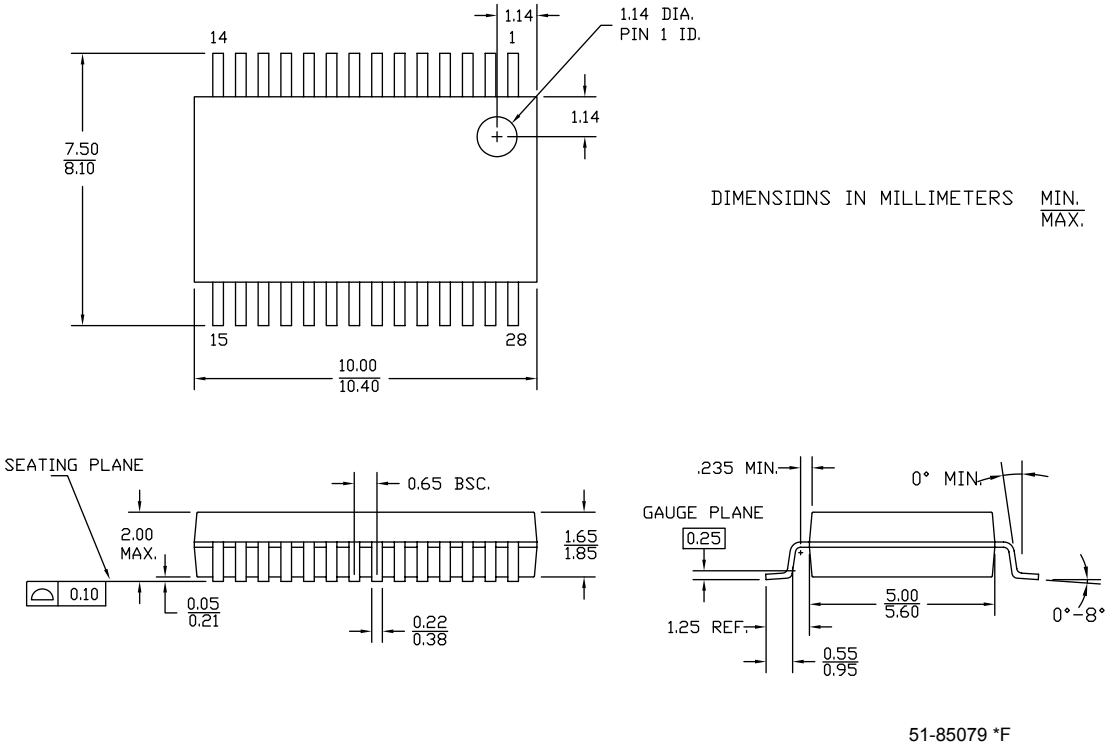


Figure 19. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064

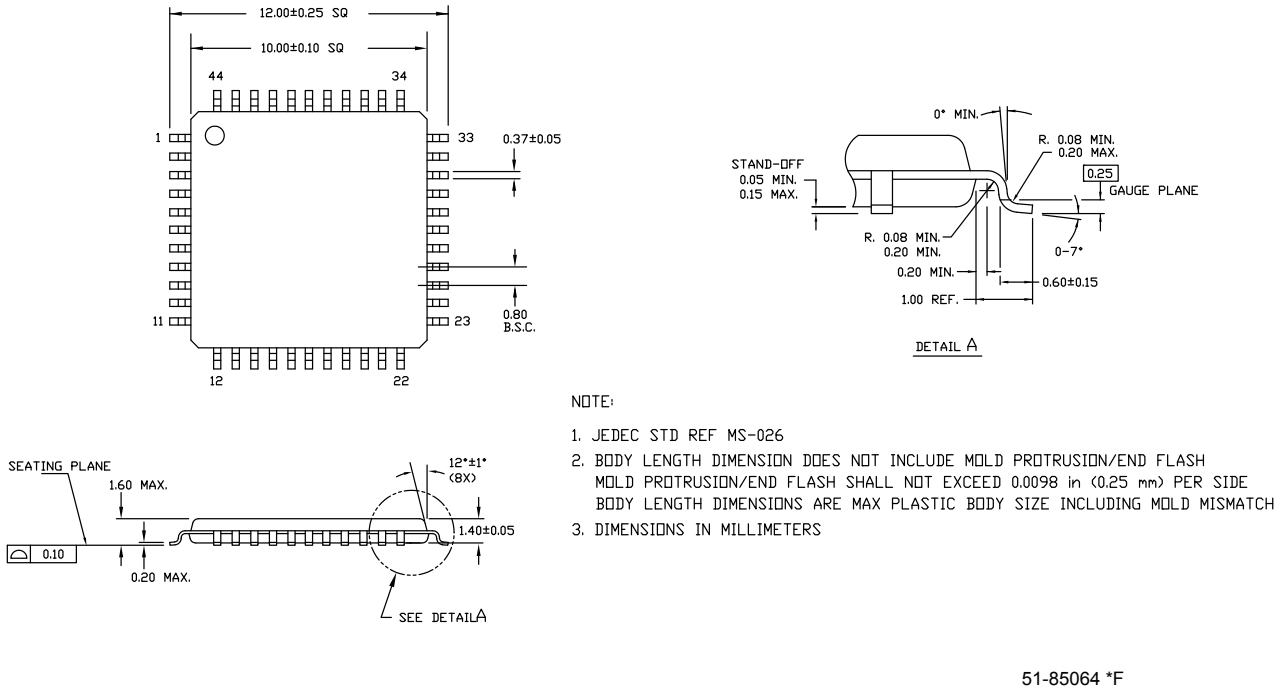
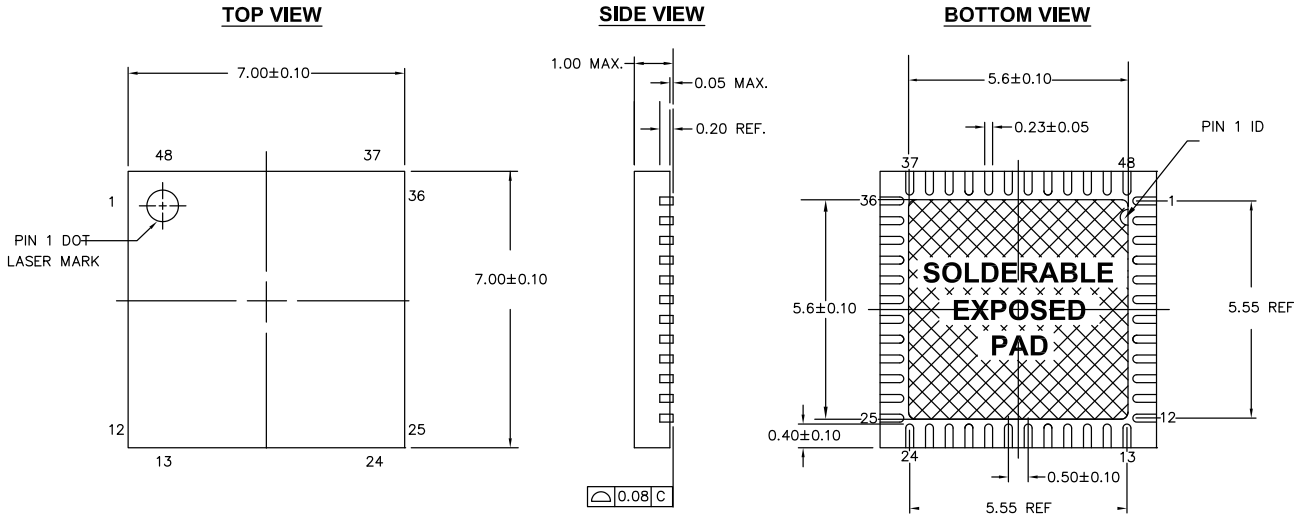


Figure 20. 48-pin QFN (7 × 7 × 1.0 mm) LT48D 5.6 × 5.6 E-Pad (Sawn Type) Package Outline, 001-45616



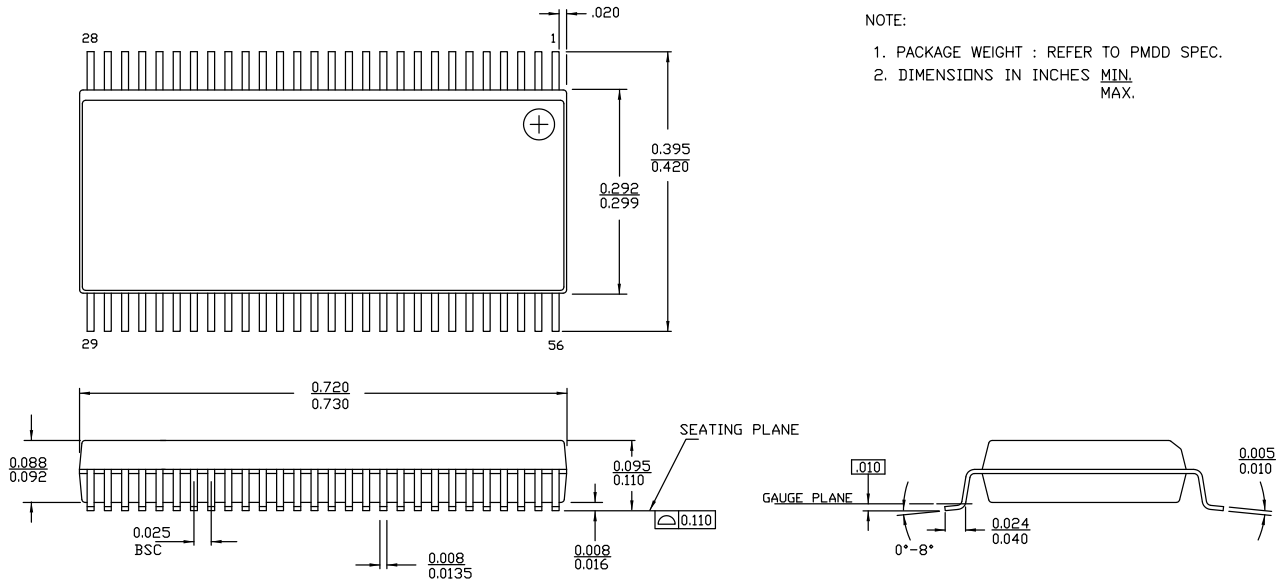
NOTES:
1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001-45616 *E

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Figure 21. 56-pin SSOP (300 Mils) O563 Package Outline, 51-85062



51-85062 *F

Thermal Impedances

Table 57. Thermal Impedances per Package

Package	Typical θ_{JA} [32]
20-pin SSOP	80.8 °C/W
28-pin SSOP	45.4 °C/W
44-pin TQFP	24.0 °C/W
48-pin QFN[33]	16.7 °C/W
56-pin SSOP	67.5 °C/W

Capacitance on Crystal Pins

Table 58. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
20-pin SSOP	Pin9 = 0.0056 pF Pin11 = 0.006048 pF
28-pin SSOP	Pin13 = 0.006796 pF Pin15 = 0.006755 pF
44-pin TQFP	Pin16 = 0.009428 pF Pin18 = 0.008635 pF
48-pin QFN	Pin17 = 0.008493 pF Pin19 = 0.008742 pF
56-pin SSOP	Pin27 = 0.007916 pF Pin31 = 0.007132 pF

Solder Reflow Specifications

Table 59 shows the solder reflow temperature limits that must not be exceeded.

Table 59. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
20-pin SSOP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
56-pin SSOP	260 °C	30 seconds

Notes
32. $T_J = T_A + POWER \times \theta_{JA}$
33. To achieve the thermal impedance specified for the QFN package, refer to *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com for PCB requirements.
34. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C28xxx family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at http://www.cypress.com.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the content of specific memory locations. Advanced emulation features are supported in PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- Pod kit for CY8C29x66 PSoC Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note The CY3207ISSP programmer needs the PSoC ISSP software. It is not compatible with the PSoC Programmer software. The latest PSoC ISSP software for this kit can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 60. Emulation and Programming Accessories

Part #	Pin Package	Pod Kit[35]	Foot Kit[36]	Adapter[37]
CY8C28243-24PVXI	20-SSOP	CY3250-28XXX	CY3250-20SSOP-FK	Adapters can be found at http://www.emulation.com.
CY8C28403-24PVXI CY8C28413-24PVXI CY8C28433-24PVXI CY8C28445-24PVXI CY8C28452-24PVXI	28-SSOP	CY3250-28XXX	CY3250-28SSOP-FK	
CY8C28513-24AXI CY8C28545-24AXI	44-TQFP	CY3250-28XXX	CY3250-44TQFP-FK	
CY8C28623-24LTXI CY8C28643-24LTXI CY8C28645-24LTXI	48-QFN	CY3250-28XXXQFN	CY3250-48QFN-FK	

Notes
35. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
36. Foot kit includes surface mount feet that can be soldered to the target PCB.
37. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

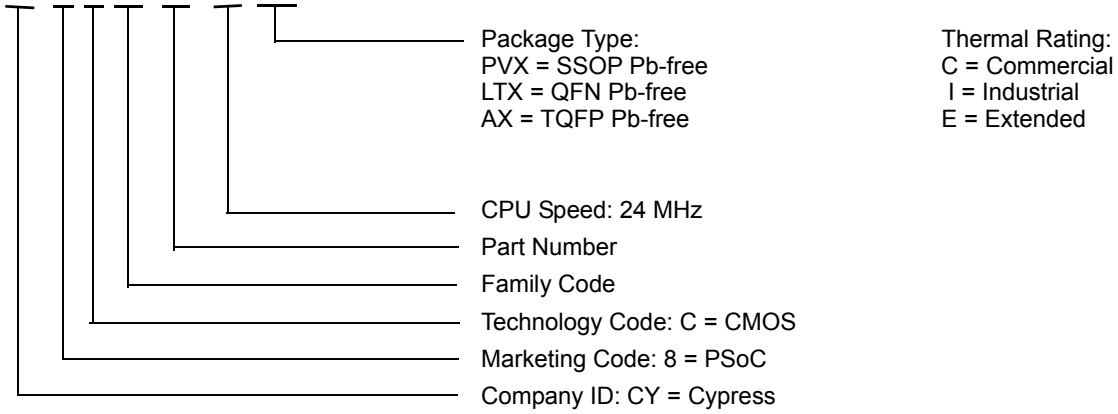
The following table lists the CY8C28xxx PSoC devices key package features and ordering codes.

Package	Ordering Code	Temperature Range	CapSense	Digital Blocks	Regular Analog Blocks	Limited Analog Blocks	HW I^2C	Decimators	10-bit SAR ADC	Digital I/O Pins	Analog Inputs	Analog Outputs	Flash (KBytes)	RAM (KBytes)	XRES Pin
28-Pin (210-Mil) SSOP	CY8C28403-24PVXI	–40 °C to 85 °C	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28403-24PVXIT	–40 °C to 85 °C	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28413-24PVXI	–40 °C to 85 °C	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28413-24PVXIT	–40 °C to 85 °C	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
44-Pin TQFP	CY8C28513-24AXI	–40 °C to 85 °C	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28513-24AXIT	–40 °C to 85 °C	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
48-Pin Sawn QFN	CY8C28623-24LTXI	–40 °C to 85 °C	N	12	6	0	2	2	N	44	10	2	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28623-24LTXIT	–40 °C to 85 °C	N	12	6	0	2	2	N	44	10	2	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28433-24PVXI	–40 °C to 85 °C	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28433-24PVXIT	–40 °C to 85 °C	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
20-Pin (210-Mil) SSOP	CY8C28243-24PVXI	–40 °C to 85 °C	N	12	12	0	2	4	Y	16	16	4	16	1	Y
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28243-24PVXIT	–40 °C to 85 °C	N	12	12	0	2	4	Y	16	16	4	16	1	Y
48-Pin Sawn QFN	CY8C28643-24LTXI	–40 °C to 85 °C	N	12	12	0	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28643-24LTXIT	–40 °C to 85 °C	N	12	12	0	2	4	Y	44	44	4	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28445-24PVXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28445-24PVXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
44-Pin TQFP	CY8C28545-24AXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28545-24AXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
48-Pin Sawn QFN	CY8C28645-24LTXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28645-24LTXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28452-24PVXI	–40 °C to 85 °C	Y	8	12	4	1	4	N	24	24	4	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28452-24PVXIT	–40 °C to 85 °C	Y	8	12	4	1	4	N	24	24	4	16	1	Y
56-Pin SSOP OCD	CY8C28000-24PVXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

CY 8 C 28 xxx - SP xxxx



Acronyms

Acronyms Used

Table 61 lists the acronyms that are used in this document.

Table 61. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC®	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SLIMO	slow IMO
IMO	internal main oscillator	SMP	switch mode pump
I/O	input/output	SOIC	small-outline integrated circuit
IrDA	infrared data association	SPI™	serial peripheral interface
ISSP	in-system serial programming	SRAM	static random access memory
LCD	liquid crystal display	SROM	supervisory read only memory
LED	light-emitting diode	SSOP	shrink small-outline package
LPC	low power comparator	UART	universal asynchronous receiver / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 available at http://www.cypress.com.

Document Conventions

Units of Measure

Table 62 lists the unit sof measures.

Table 62. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	µs	microsecond
dB	decibels	ms	millisecond
°C	degree Celsius	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	µV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohm	V	volts
Ω	ohm	µW	microwatts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
mH	millihenry		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	5. A logic signal having its asserted state as the logic 1 state. 6. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary *(continued)*

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary *(continued)*

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Glossary *(continued)*

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

Glossary *(continued)*

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Errata

This section describes the errata for CY8C28243, CY8C28403, CY8C28413, CY8C28433, CY8C28445, CY8C28452, CY8C28513, CY8C28545, CY8C28623, CY8C28643, CY8C28645 PSoC devices. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Please contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY8C28403	All Variants
CY8C28243	All Variants
CY8C28413	All Variants
CY8C28433	All Variants
CY8C28445	All Variants
CY8C28513	All Variants
CY8C28545	All Variants
CY8C28643	All Variants
CY8C28645	All Variants
CY8C28452	All Variants
CY8C28623	All Variants

Qualification Status

Engineering Samples

Errata Summary

The following table defines the errata applicability to CY8C28xxx devices.

Note Each erratum in the table below is hyperlinked. Click on the item entry to jump to its description.

Items	MPN	Silicon Revision	Fix Status
10-bit SAR ADC does not meet DNL/INL specification	CY8C28403 CY8C28413 CY8C28513 CY8C28433 CY8C28243 CY8C28643 CY8C28445 CY8C28545 CY8C28645	*A	Silicon fix is not planned. The workaround mentioned above should be used.
Wrong data read from IDAC_CRx and DACx_D registers	CY8C28413 CY8C28513 CY8C28433 CY8C28445 CY8C28545 CY8C28645 CY8C28452	*A	Silicon fix is not planned. The workaround mentioned above should be used.

1. 10-bit SAR ADC does not meet DNL/INL specification.

■ **Problem Definition**

The 10-bit hardware SAR ADC does not meet datasheet accuracy specifications for DNL and INL under some conditions.

■ **Parameters Affected**

INLSAR10: Integral nonlinearity

DNLSAR10: Differential nonlinearity

■ **Trigger Condition(S)**

The SAR ADC DNL has been measured greater than 2 LSB over temperature in all cases, as compared to the datasheet specification of 1.5 LSB.

When using the VPWR (Vdd) reference configuration, the SAR ADC DNL has been measured over temperature at 2 LSB for a supply voltage of 3.3 V. With a supply voltage of 5.5 V, the DNL has been measured greater than 3.5 LSB.

■ **Scope of Impact**

Inaccurate converted data.

■ **Workaround**

- Use an alternate ADC implementation (DelSig, ADCINC) available in CY8C28xxx devices.
- Avoid CPU operations that change the address and data buses while A-D conversion is running with internal Vpwr (Vdd) as Vref.
- Use un-buffered RefHi as ADC Vref. This may have a negative effect on the analog blocks in the analog array due to the noise introduced on RefHi reference.

■ **Fix Status**

Silicon fix is not planned. The workaround mentioned above should be used.

2. Wrong data read from IDAC_CRx and DACx_D registers.

■ **Problem Definition**

The CPU may read an incorrect value of bits 0, 3, 5, or 7 from the following registers:

- IDAC_CR0
- IDAC_CR1
- DAC0_D
- DAC1_D

■ **Parameters Affected**

F_{CPU1} and F_{CPU2} from the device data sheet.

■ **Trigger Condition(S)**

When CPU Clock is set at its highest frequency setting (24 MHz nominal).

■ **Scope of Impact**

Incorrect data read from affected registers.

■ **Workaround**

Temporarily slow down CPU Clock frequency to 12 MHz nominal (or lower) when affected registers are read.

Document History Page

Document Title: CY8C28243/CY8C28403/CY8C28413/CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/ CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™ Document Number: 001-48111				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
**	2593460	BTK / PYRS	10/20/08	New document (Revision **).
*A	2652217	BTK / PYRS	02/02/09	Extensive updates to content. Added registers maps. Updated Getting Started section Updated Development Tools section Added some SAR10 ADC specifications. Added more analog system figures
*B	2675937	BTK	03/18/09	Updated DC Analog Reference Specifications tables Minor content updates
*C	2679015	HMI	03/26/2009	Post to external web.
*D	2750217	TDU	08/10/09	Updates to Electrical Specifications section Minor content updates
*E	2768143	TDU	09/23/09	Updated DC Operational Amplifier, DC Analog Reference, DC SAR10ADC, and DC POR specifications; Added Figure 15 and Figure 16; Updated AC TypeE-Operational and AC SAR10ADC specifications
*F	2805324	ALH	11/11/09	Added Contents page. Updated Electrical Specifications.
*G	2902396	NJF	03/30/2010	Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Updated DC SAR10 ADC Specifications. Modified Note 23. Removed AC Analog Mux Bus Specifications, Third Party Tools and Build a PSoC Emulator into your Board. Updated Packaging Information and Ordering Code Definitions. Updated links in Sales, Solutions, and Legal Information.
*H	3063584	NJF	10/20/10	Added PSoC Device Characteristics table. Added DC I2C Specifications table. Added F32K_U max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update.
*I	3148779	NJF	01/20/11	Added Footnote # 34 to Thermal Impedances section. Table 7. 56-Pin Part Pinout (SSOP) (page 15) - Pin#28 - Pin Name changed to “V_{SS}”. Table 5. 44-Pin Part Pinout (TQFP) (page 13) - Pin#17 - Pin Type changed to “Power”. Under DC SAR10 ADC Specifications table, for parameter $V_{VREFSAR10}$, Max value changed from 4.95 V to V_{DD} – 0.3 V. Updated Table 59, “Solder Reflow Specifications,” on page 72 as per spec 25-00090.
*J	3598237	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*K	3758002	GULA	10/01/2012	Updated Packaging Information (spec 001-45616 (Changed revision from *B to *D), spec 51-85062 (Changed revision from *D to *F)).

Document History Page *(continued)*

Document Title: CY8C28243/CY8C28403/CY8C28413/CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/ CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™
Document Number: 001-48111

Revision	ECN	Origin of Change	Submission Date	Description of Change
*L	3993399	GVH	05/08/2013	Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata.
*M	4138595	GVH	09/27/2013	Updated to new template. Completing Sunset Review.
*N	4476160	ASRI / SEG	09/04/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added More Information. Added PSoC Designer. Updated PSoC Functional Overview: Updated PSoC Device Characteristics: Updated Table 2: Added a column “Analog Mux Buses” at the end. Removed “Getting Started”. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC I2C Specifications: Updated Table 42: Added V_{OLI2C} parameter and its details. Updated Packaging Information: spec 51-85064 – Changed revision from *E to *F. Completing Sunset Review.
*O	4914758	ASRI	09/10/2015	Updated Document Title to read as “CY8C28243/CY8C28403/CY8C28413/ CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/ CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™”. Removed CY8C28533 related information in all instances across the document. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC SAR10 ADC Specifications: Updated Table 38: Updated details in “Description” column of DNL_{SAR10} parameter. Updated Packaging Information: Updated Packaging Dimensions: spec 51-85077 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. spec 001-45616 – Changed revision from *D to *E. Updated Development Tool Selection: Updated Accessories (Emulation and Programming): Updated Table 60: Updated details in “Part #” column corresponding to 44-pin TQFP package. Updated Ordering Information: Updated part numbers. Updated Errata: Updated Part Numbers Affected: Updated table. Updated Errata Summary: Updated table and also details below the table. Updated to new template. Completing Sunset Review.

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