



PIC16(L)F153XX

Cost-Effective 8 to 48 Pins Microcontroller Product Brief

Description

PIC16(L)F153XX microcontrollers feature Intelligent Analog, Core Independent Peripherals (CIPs) and communication peripherals combined with eXtreme Low-Power (XLP) for a wide range of general purpose and low-power applications. The family features PWMs, multiple communication, temperature sensor and memory features like Memory Access Partition (MAP) and Device Information Area (DIA). The products are offered in a broad range of pin counts from 8 to 48 pins, to support customers in various applications.

Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
 - DC – 32 MHz clock input
 - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
 - 8-bit (TMR2) with Hardware Limit Timer (HLT) Extension
 - 16-bit (TMR0/1)
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
 - Variable prescaler selection
 - Variable window size selection
 - All sources configurable in hardware or software
- Programmable Code Protection

Memory

- Up to 28 KB Flash Program Memory
- Up to 2 KB Data SRAM Memory
- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
 - Write protect
 - Customizable Partition
- Device Information Area (DIA)

Operating Characteristics

- Operating Voltage Range:
 - 1.8V to 3.6V (PIC16LF153XX)
 - 2.3V to 5.5V (PIC16F153XX)
- Temperature Range:
 - Industrial: -40°C to 85°C
 - Extended: -40°C to 125°C

Power-Saving Functionality

- Doze mode:
 - Ability to run CPU core slower than the system clock
- Idle mode:
 - Ability to halt CPU core while internal peripherals continue operating
- Sleep mode:
 - Lowest power consumption
- Peripheral Module Disable (PMD):
 - Ability to disable hardware module to minimize power consumption of unused peripherals

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
 - 8 μ A @ 32 kHz, 1.8V, typical
 - 32 μ A/MHz @ 1.8V, typical

Digital Peripherals

- Four Configurable Logic Cells (CLCs):
 - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
 - Rising and Falling edge dead-band control
 - Full-bridge, half-bridge, 1-channel drive
 - Multiple signal sources
- Two Capture/Compare/PWM (CCP) modules
- Four 10-bit PWMs
- Numerically Controlled Oscillator (NCO):
 - Generates true linear frequency control and increased frequency resolution
 - Input Clock: 0 Hz < f_{NCO} < 32 MHz
 - Resolution: f_{NCO}/220
- Peripheral Pin Select (PPS):
 - Enables pin mapping of digital I/O

PIC16(L)F153XX

- Communication:
 - Up to two EUSART, RS-232, RS-485, LIN compatible
 - Up to two SPI
 - Two I²C, SMBus, PMBus™ compatible
- Up to 44 I/O Pins
 - Individually programmable pull-ups slew rate control Interrupt-on-Change with edge-select

Analog Peripherals

- Analog-to-Digital Converter (ADC):
 - 10-bit with up to 43 external channels
 - Conversion available during Sleep
- Two Comparator:
 - Low-Power/High-Speed mode
 - Fixed Voltage Reference at (non)inverting input(s)
 - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
 - 5-bit resolution, rail-to-rail
 - Positive Reference Selection
 - Unbuffered I/O pin output
 - Internal connections to ADCs and comparators
- Voltage Reference:
 - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output level

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
 - Selectable frequency range up to 32 MHz
 - ±1% at calibration (nominal)
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOCS)
- External Oscillator Block with:
 - Three crystal/resonator modes up to 20 MHz
 - Three external clock modes up to 20 MHz
 - Fail-Safe Clock Monitor
 - Allows for safe shutdown if peripherals clock stops
 - Oscillator Start-up Timer (OST)
 - Ensures stability of crystal oscillator sources

PIC16(L)F153XX

TABLE 1: PIC16(L)F153XX FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (KW)	Program Flash Memory (KB)	Storage Area Flash (B)	Data SRAM (bytes)	I/O Pins	10-Bit ADC	5-Bit DAC	Comparator	8-Bit/ (with HLT) Timer	16-Bit Timer	Window Watchdog Timer	CCP/10-Bit PWM	CWG	NCO	CLC	Zero Cross Detect	Temperature Sensor	Memory Access Partition	Device Information Area	EUSART/I ² C/SPI	Peripheral Pin Select	Peripheral Module Disable	Debug ⁽¹⁾
PIC16F15313	(C)	2	3.5	224	256	6	5	1	1	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	1/1	Y	Y	I
PIC16F15323	(C)	2	3.5	224	256	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	1/1	Y	Y	I
PIC16F15324	(D)	4	7	224	512	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16F15325	(B)	8	14	224	1024	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16F15344	(D)	4	7	224	512	18	17	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16F15345	(B)	8	14	224	1024	18	17	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16F15354	(A)	4	7	224	512	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16F15355	(A)	8	14	224	1024	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16F15356	(E)	16	28	224	2048	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16F15375	(F)	8	14	224	1024	36	35	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16F15376	(E)	16	28	224	2048	36	35	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16F15385	(F)	8	14	224	1024	44	43	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16F15386	(E)	16	28	224	2048	44	43	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I

Note 1: I - Debugging integrated on chip.

Data Sheet Index:

- A:** Future Release [PIC16\(L\)F15354/5 Data Sheet, 28-Pin](#)
- B:** Future Release [PIC16\(L\)F15325/45 Data Sheet, 14/20-Pin](#)
- C:** Future Release [PIC16\(L\)F15313/23 Data Sheet, 8/14-Pin](#)
- D:** Future Release [PIC16\(L\)F15324/44 Data Sheet, 14/20-Pin](#)
- E:** Future Release [PIC16\(L\)F15356/76/86 Data Sheet, 28/40/48-Pin](#)
- F:** Future Release [PIC16\(L\)F15375/85 Data Sheet, 40/48-Pin](#)

Note: For other small form-factor package availability and marking information, visit www.microchip.com/packaging or contact your local sales office.

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TABLE 2: PACKAGES

Device	(S)PDIP	SOIC	SSOP	TSSOP	(U)DFN (3x3)	QFN (4x4)	QFN (6x6)	UQFN (4x4)	TQFP	QFN (8x8)	UQFN (5x5)	UQFN (6x6)
PIC16(L)F15313	X	X	—	—	X	—	—	—	—	—	—	—
PIC16(L)F15323	X	X	—	X	—	X	—	X	—	—	—	—
PIC16(L)F15324	X	X	—	X	—	X	—	X	—	—	—	—
PIC16(L)F15325	X	X	—	X	—	X	—	X	—	—	—	—
PIC16(L)F15344	X	X	X	—	—	X	—	X	—	—	—	—
PIC16(L)F15345	X	X	X	—	—	X	—	X	—	—	—	—
PIC16(L)F15354	X	X	X	—	—	—	X	X	—	—	—	—
PIC16(L)F15355	X	X	X	—	—	—	X	X	—	—	—	—
PIC16(L)F15356	X	X	X	—	—	—	X	X	—	—	—	—
PIC16(L)F15375	X	—	—	—	—	—	—	—	X	X	X	—
PIC16(L)F15376	X	—	—	—	—	—	—	—	X	X	X	—
PIC16(L)F15385	—	—	—	—	—	—	—	—	X	—	—	X
PIC16(L)F15386	—	—	—	—	—	—	—	—	X	—	—	X

Note: Pin details are subject to change.

PIN DIAGRAMS

FIGURE 1: 8-PIN PDIP, SOIC, MSOP, FOR PIC16(L)F15313

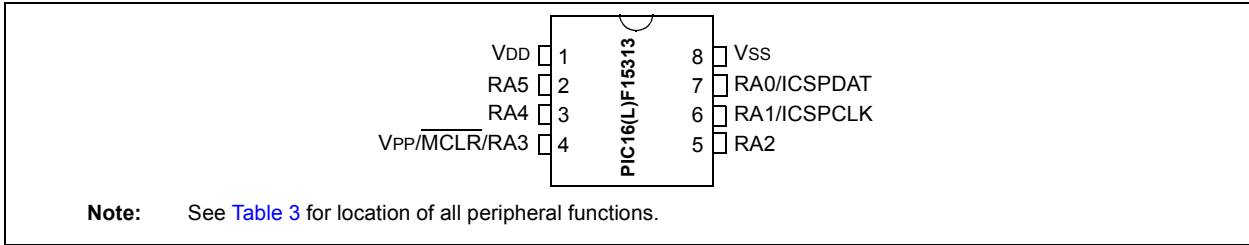


FIGURE 2: 14-PIN PDIP, SOIC, TSSOP FOR PIC16(L)F15323

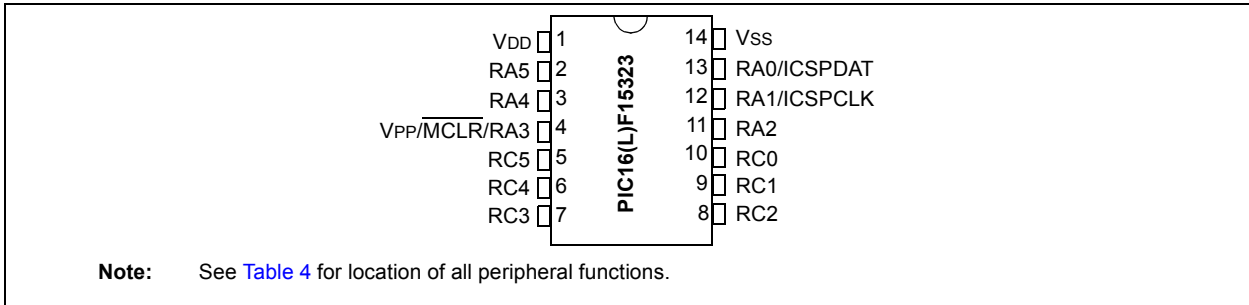


FIGURE 3: 14-PIN PDIP, TSSOP FOR PIC16(L)F15324 AND PIC16(L)F15325

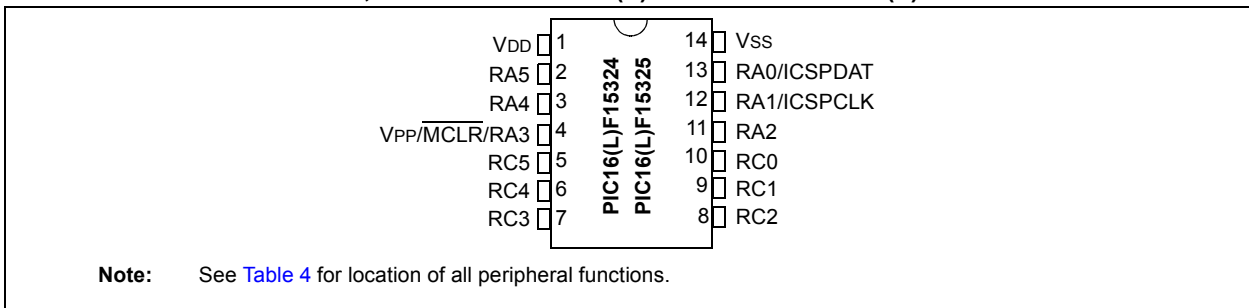
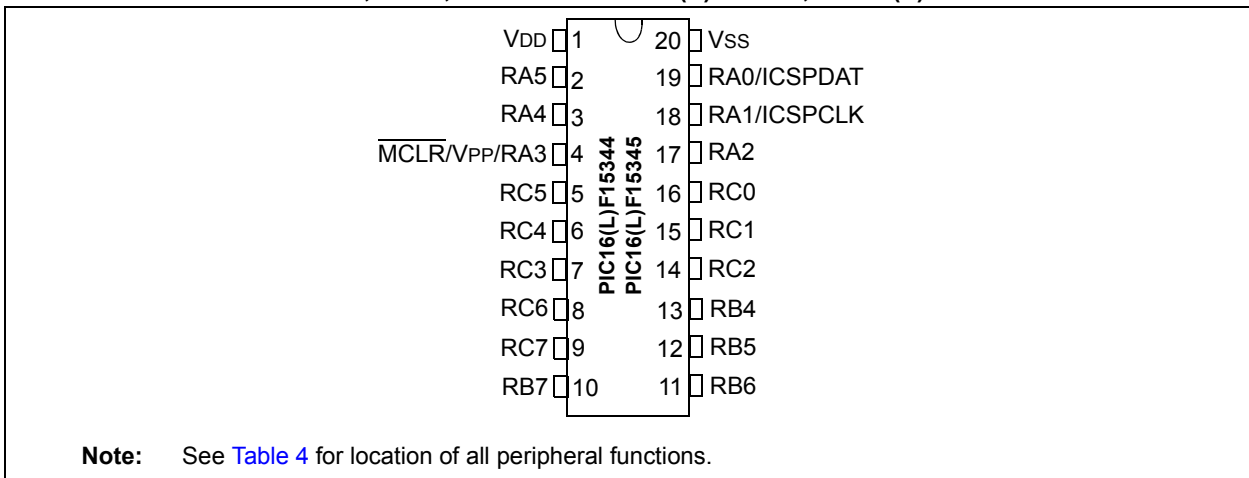


FIGURE 4: 20-PIN PDIP, SOIC, SSOP FOR PIC16(L)F15344, PIC16(L)F15345



PIC16(L)F153XX

FIGURE 5: 28-PIN PDIP, SOIC, SSOP FOR PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356

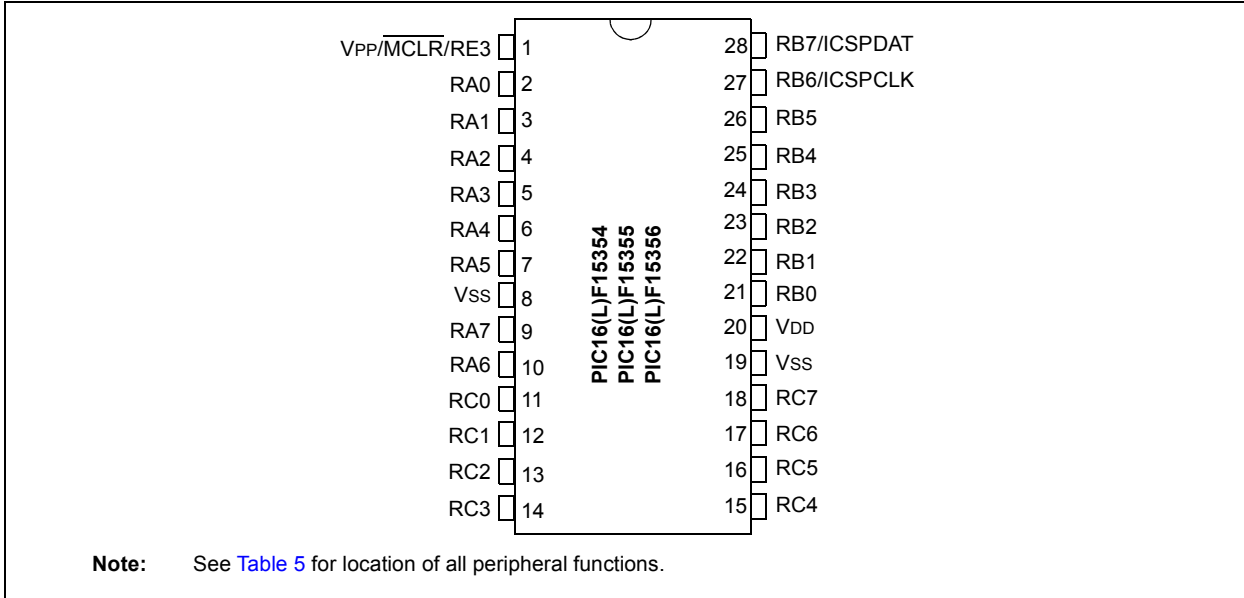


FIGURE 6: 40-PIN PDIP FOR PIC16(L)F15375, PIC16(L)F15376

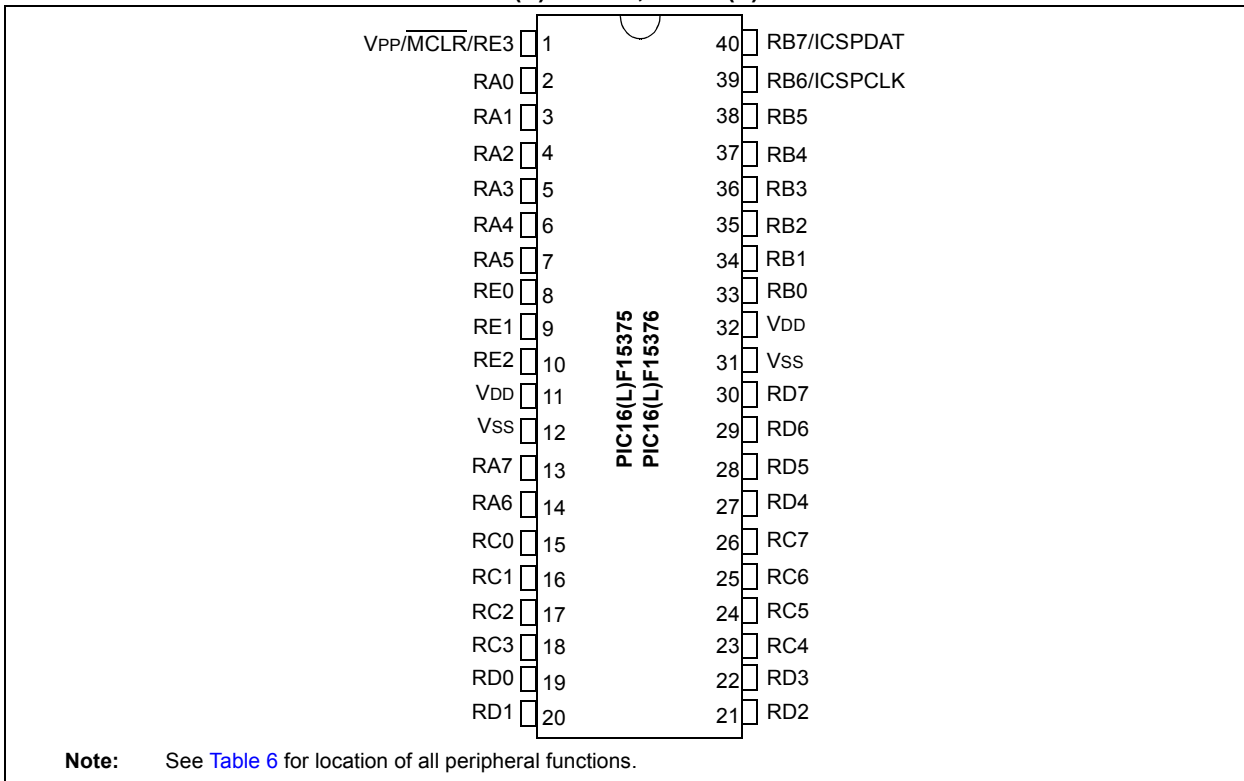


FIGURE 7: 16-PIN QFN/UQFN (4X4) FOR PIC16(L)F15323, PIC16(L)F15324, PIC16(L)F15325

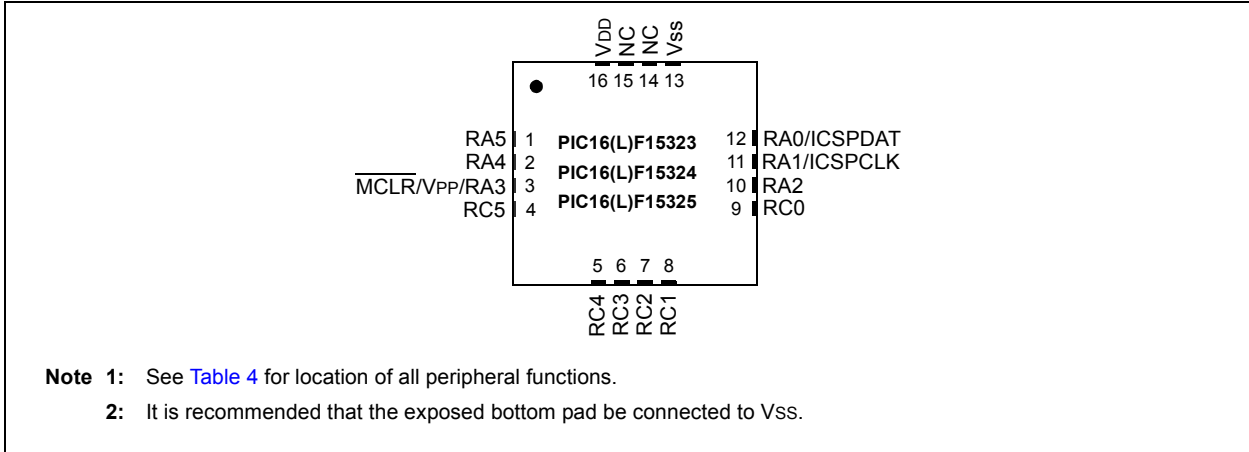
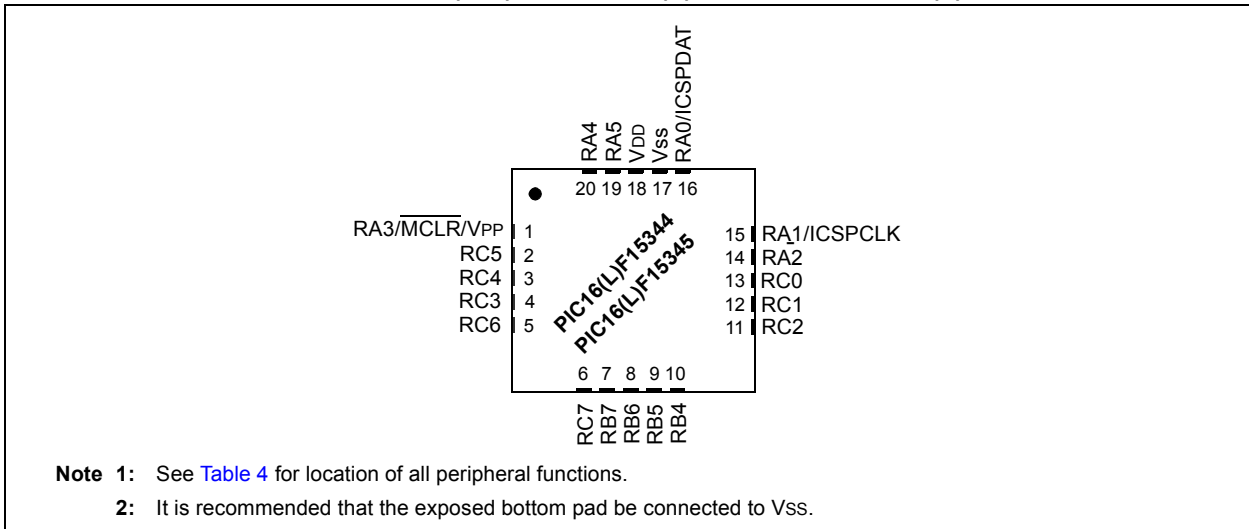


FIGURE 8: 20-PIN QFN/UQFN (4x4) FOR PIC16(L)F15344 AND PIC16(L)F15345



PIC16(L)F153XX

FIGURE 9: 28-PIN UQFN (4X4) FOR PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356

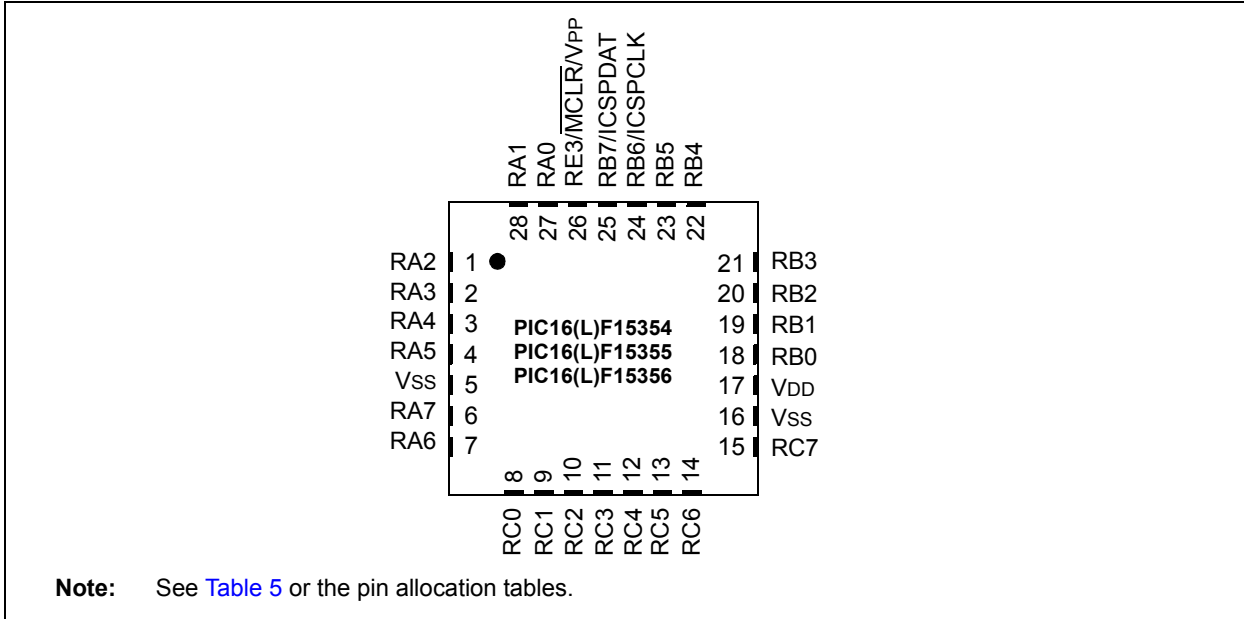


FIGURE 10: 28-PIN QFN (6X6) FOR PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356

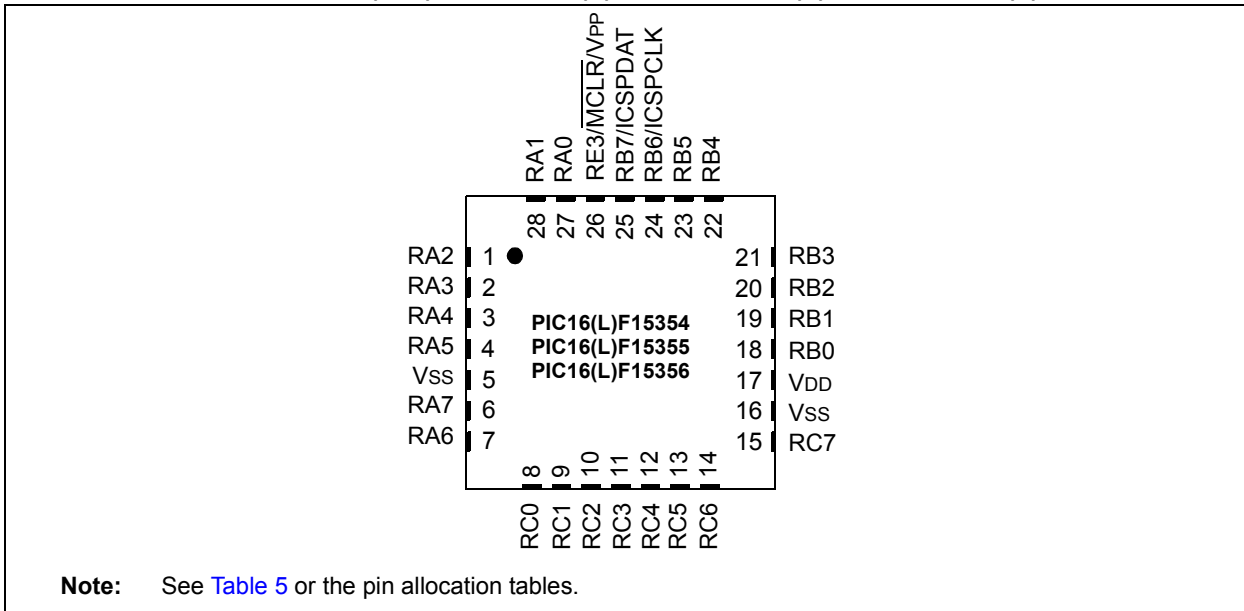


FIGURE 11: 40-PIN UQFN (5X5) FOR PIC16(L)F15375, PIC16(L)F15376

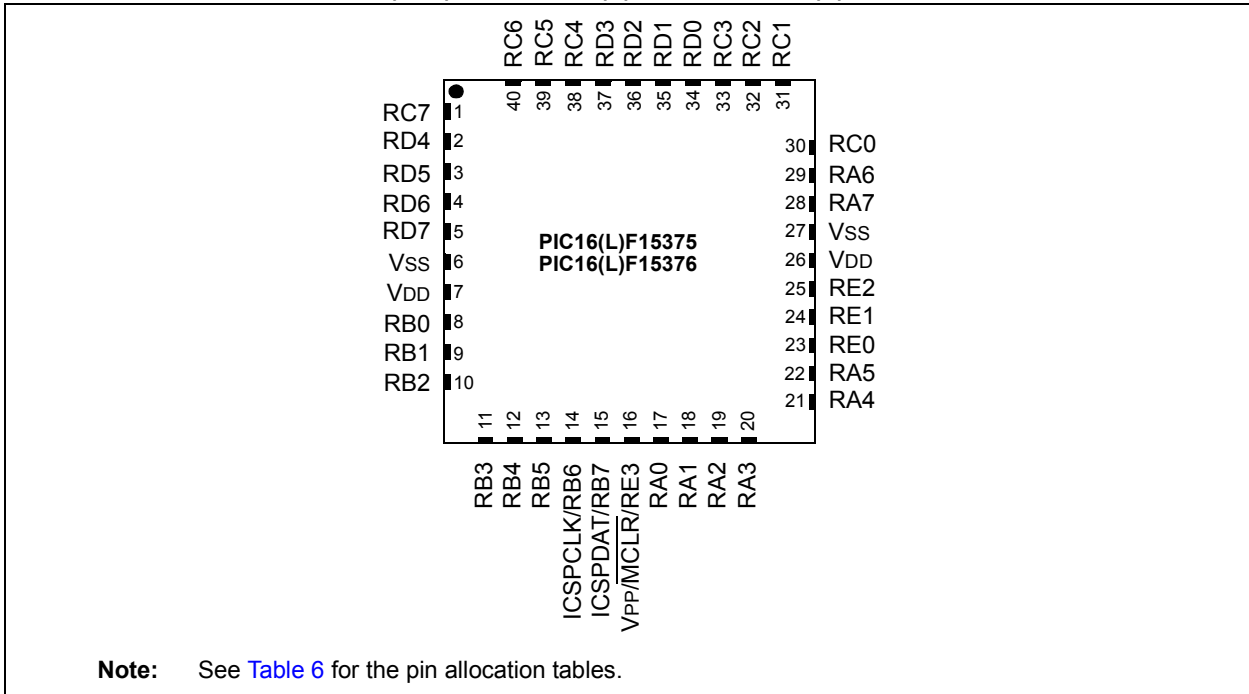
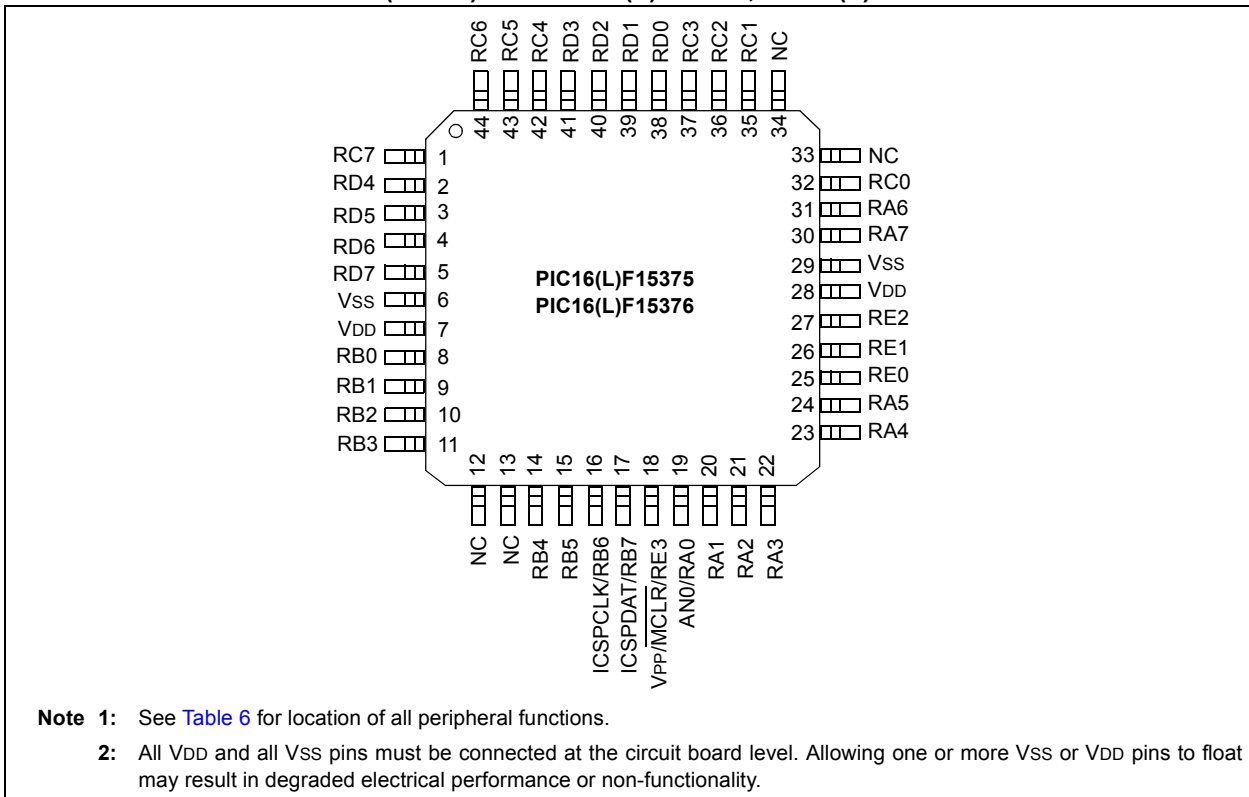


FIGURE 12: 44-PIN TQFP (10X10) FOR PIC16(L)F15375, PIC16(L)F15376



PIC16(L)F153XX

FIGURE 13: 44-PIN QFN (8X8X0.9) FOR PIC16(L)F15375, PIC16(L)F15376

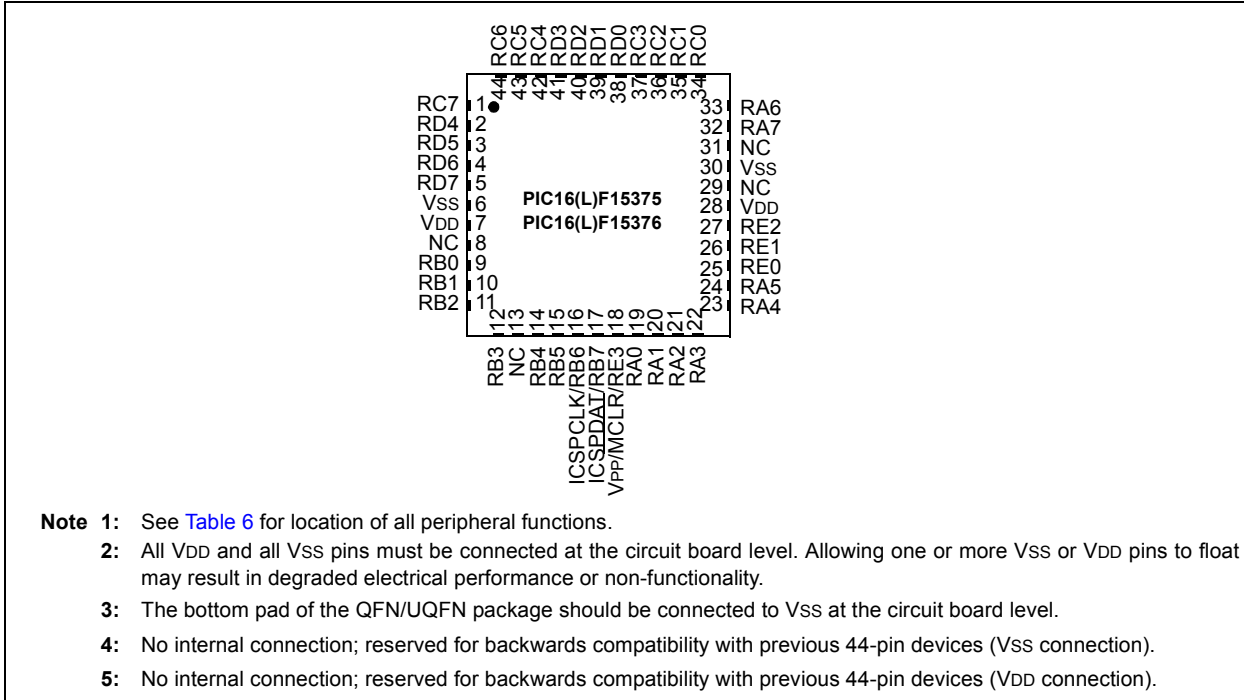


FIGURE 14: 48-PIN UQFN (6X6) FOR PIC16(L)F15385, PIC16(L)F15386

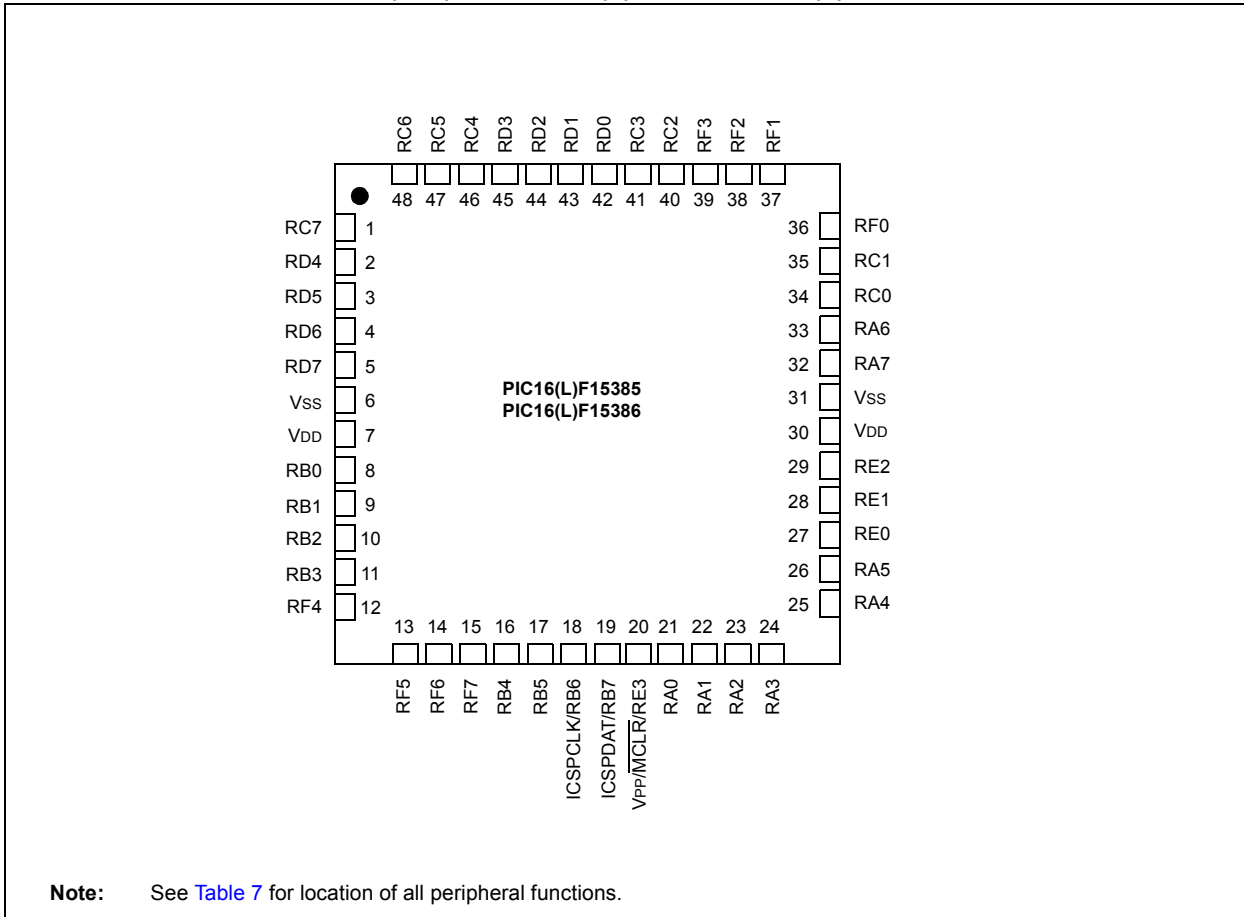
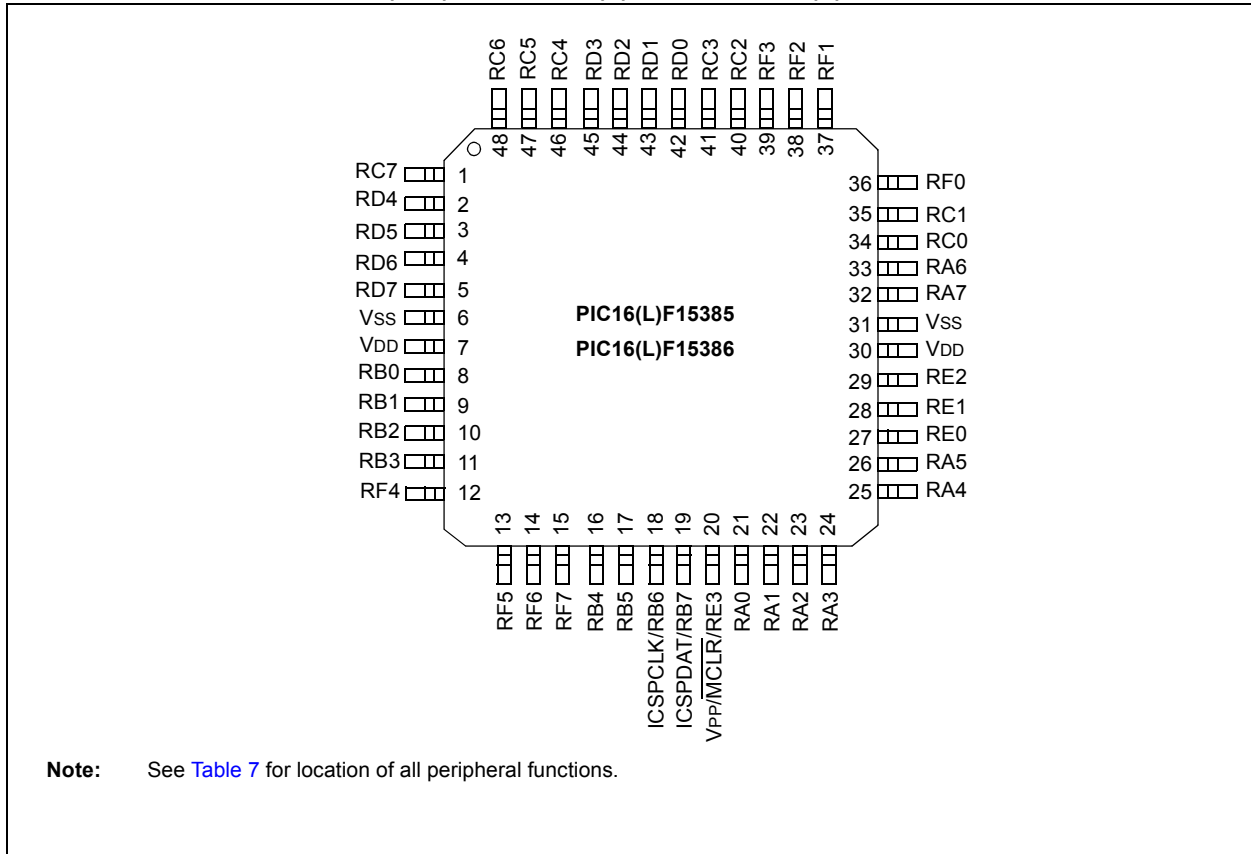


FIGURE 15: 48-PIN TQFP (7X7) FOR PIC16(L)F15385, PIC16(L)F15386



PIN ALLOCATION TABLES

TABLE 3: 8-PIN ALLOCATION TABLE (PIC16(L)F15313)

I/O ⁽²⁾	8-Pin PDIP/SOIC/MSOP	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC
RA0	7	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	TX/CK ⁽¹⁾	CLCIN3 ⁽¹⁾
RA1	6	ANA1	V _{REF+}	C1IN0-	—	DA1 _{REF+}	T0CKI ⁽¹⁾	—	—	—	SSP1CLK ^{(1),(4)} SSP1DAT ^{(1),(4)}	—	RX/DT ⁽¹⁾	CLCIN2 ⁽¹⁾
RA2	5	ANA2	V _{REF-}	—	—	DAC1 _{REF-}	—	—	—	CWG1 ⁽¹⁾	SSP1CLK ^{(1),(4)} SSP1DAT ^{(1),(4)}	ZCD1	—	—
RA3	4	—	—	—	—	—	—	—	—	—	SSP1SS ⁽¹⁾	—	—	CLCIN0 ⁽¹⁾
RA4	3	ANA4	—	C1IN1-	—	—	T1G ⁽¹⁾ SOSCO	—	—	—	—	—	—	—
RA5	2	ANA5 ADACT ⁽¹⁾	—	—	—	—	T1CKI ⁽¹⁾ T2IN ⁽¹⁾ SOSCIN SOSCI	CCP1 ⁽¹⁾ CCP2 ⁽¹⁾	—	—	—	—	—	CLCIN1 ⁽¹⁾
V _{DD}	1	—	—	—	—	—	—	—	—	—	—	—	—	—
V _{SS}	8	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT ⁽²⁾	—	—	—	C1OUT	NCO1OUT	—	TMR0	CCP1	PWM3	CWG1A	SDO1	—	DT1 ⁽³⁾	CLC1OUT
	—	—	—	C2OUT	—	—	—	CCP2	PWM4	CWG1B	SCK1	—	CK1	CLC2OUT
	—	—	—	—	—	—	—	—	PWM5	CWG1C	SCL1 ^{(3),(4)}	—	TX1	CLC3OUT
	—	—	—	—	—	—	—	—	PWM6	CWG1D	SDA1 ^{(3),(4)}	—	—	CLC4OUT

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
 - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLV specific or SMBUS input buffer thresholds.

TABLE 4: 14/16/20-PIN ALLOCATION TABLE (PIC16(L)F15323, PIC16(L)F15324, PIC16(L)F15325, PIC16(L)F15344)

I/O ⁽²⁾	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC
RA0	13	12	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—
RA1	12	11	18	15	ANA1	V _{REF+}	C1IN0-	—	DA1 _{REF+}	T0CKI ⁽¹⁾	—	—	—	—	—	—	—
RA2	11	10	17	14	ANA2	V _{REF-}	—	—	DAC1 _{REF-}	—	—	—	CWG1 ⁽¹⁾	—	ZCD1	—	CLCIN0 ⁽⁵⁾
RA3	4	3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—
RA4	3	2	3	20	ANA4	—	C1IN1-	—	—	T1G ⁽¹⁾ SOSCO	—	—	—	—	—	—	—
RA5	2	1	2	19	ANA5	—	—	—	—	T1CKI ⁽¹⁾ T2IN SOSCIN SOSCI	—	—	—	—	—	—	CLCIN3 ⁽⁵⁾
RC0	10	9	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	SSP1CLK ^{(1),(5)} SSP1DAT ^{(1),(5)}	—	—	—
RC1	9	8	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	SSP1CLK ^{(1),(5)} SSP1DAT ^{(1),(5)}	—	—	CLCIN2 ⁽⁵⁾
RC2	8	7	14	11	ANC2	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—
RC3	7	6	7	4	ANC3	—	C1IN3- C2IN3-	—	—	—	CCP2	—	—	SSP1SS ⁽⁵⁾	—	—	CLCIN1 ⁽⁵⁾ CLCIN0 ⁽⁵⁾
RC4	6	5	6	3	ANC4	—	—	—	—	—	—	—	—	SSP2CLK ^{(1),(5)} SSP2DAT ^{(1),(5)}	—	TX1/CK1 ⁽⁵⁾	CLCIN1 ⁽⁵⁾
RC5	5	4	5	2	ANC5	—	—	—	—	—	CCP1	—	—	SSP1CLK ^{(1),(5)} SSP1DAT ^{(1),(5)}	—	RX1/DT1 ⁽⁵⁾	—
RC6	—	—	8	5	ANC6	—	—	—	—	—	—	—	—	SSP1SS1 ⁽⁶⁾	—	—	—
RC7	—	—	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—
RB4	—	—	13	10	ANB4 ADACT ⁽¹⁾	—	—	—	—	—	—	—	—	SSP1CLK ^{(1),(6)} SSP1DAT ^{(1),(6)}	—	—	CLCIN2 ⁽⁵⁾
RB5	—	—	12	9	ANB5	—	—	—	—	—	—	—	—	SSP2CLK ^{(1),(6)} SSP2DAT ^{(1),(6)}	—	RX1/DT1 ⁽⁶⁾	CLCIN3 ⁽⁵⁾

TABLE 4: 14/16/20-PIN ALLOCATION TABLE (PIC16(L)F15323, PIC16(L)F15324, PIC16(L)F15325, PIC16(L)F15344)

I/O ⁽²⁾	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC
RB6	—	—	11	8	ANB6	—	—	—	—	—	—	—	—	SSP1CLK ^{(1),(6)} SSP1DAT ^{(1),(6)}	—	—	—
RB7	—	—	10	7	ANB7	—	—	—	—	—	—	—	—	SSP2CLK ^{(1),(6)} SSP2DAT ^{(1),(6)}	—	TX1/CK1 ⁽⁶⁾	—
V _{DD}	1	16	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—
V _{SS}	14	13	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT ⁽²⁾	—	—	—	—	—	—	C1OUT	NCO1OUT	—	TMR0	CCP1	PWM3	CWG1A	SDO1 SDO2	—	DT1 ⁽³⁾	CLC1OU
	—	—	—	—	—	—	C2OUT	—	—	—	CCP2	PWM4	CWG1B	SCK1 SCK2	—	CK1	CLC2OU
	—	—	—	—	—	—	—	—	—	—	—	PWM5	CWG1C	SCL1 ^{(3),(4)} SCL2 ^{(3),(4)}	—	TX1	CLC3OU
	—	—	—	—	—	—	—	—	—	—	—	PWM6	CWG1D	SDA1 ^{(3),(4)} SDA2 ^{(3),(4)}	—	—	CLC4OU

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
 - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLV SMBUS input buffer thresholds.
 - 5: For 14 and 16-pin package only.
 - 6: For 20-pin package only.

TABLE 5: 28-PIN ALLOCATION TABLE (PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356)

I/O ⁽²⁾	28-Pin PDIP/SOIC/SSOP	28-Pin (U)QFN	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLC
RA0	2	27	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	CLCIN0 ⁽¹⁾	—
RA1	3	28	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	CLCIN1 ⁽¹⁾	—
RA2	4	1	ANA2	—	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—	—
RA3	5	2	ANA3	VREF+	C1IN1+	—	DACREF+	—	—	—	—	—	—	—	—	—
RA4	6	3	ANA4	—	—	—	—	TOCKI	—	—	—	—	—	—	—	—
RA5	7	4	ANA5	—	—	—	—	T1G ⁽¹⁾	—	—	—	SSP1SS ⁽¹⁾	—	—	—	—
RA6	10	7	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—
RA7	9	6	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—
RB0	21	18	ANB0	—	C2IN1+	—	—	—	—	—	CWG1 ⁽¹⁾	SSP2SS ⁽¹⁾	ZCD1	—	—	—
RB1	22	19	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—	—
RB2	23	20	ANB2	—	—	—	—	—	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—	—
RB3	24	21	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—
RB4	25	22	ANB4 ADACT ⁽¹⁾	—	—	—	—	—	—	—	—	—	—	—	—	—
RB5	26	23	ANB5	—	—	—	—	—	—	—	—	—	—	—	—	—
RB6	27	24	ANB6	—	—	—	—	—	—	—	—	—	—	TX2 CK2 ⁽¹⁾	CLCIN2 ⁽¹⁾	—
RB7	28	25	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	—	RX2 DT2 ⁽¹⁾	CLCIN3 ⁽¹⁾	—
RC0	11	8	ANC0	—	—	—	—	SOSCO T1CKI	—	—	—	—	—	—	—	—
RC1	12	9	ANC1	—	—	—	—	SOSCI	CCP2 ⁽¹⁾	—	—	—	—	—	—	—
RC2	13	10	ANC2	—	—	—	—	—	CCP1 ⁽¹⁾	—	—	—	—	—	—	—
RC3	14	11	ANC3	—	—	—	—	T2IN ⁽¹⁾	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—	—
RC4	15	12	ANC4	—	—	—	—	—	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—	—

TABLE 5: 28-PIN ALLOCATION TABLE (PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356) (CONTINUED)

I/O ⁽²⁾	28-Pin PDIP/SOIC/SSOP	28-Pin (U)QFN	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKB
RC5	16	13	ANC5	—	—	—	—	—	—	—	—	—	—	—	—	—
RC6	17	14	ANC6	—	—	—	—	—	—	—	—	—	—	TX1 CK1 ⁽¹⁾	—	—
RC7	18	15	ANC7	—	—	—	—	—	—	—	—	—	—	RX1 DT1 ⁽¹⁾	—	—
RE3	1	26	ANE3	—	—	—	—	—	—	—	—	—	—	—	—	—
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	8	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	19	5	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSEL0	19	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT ⁽²⁾	—	—	—	—	C1OUT	NCO1OUT	—	TMR0	CCP1	PWM3	CWG1A CWG2A	SDO	—	DT ⁽³⁾	CLC1OUT	CLKB
	—	—	—	—	C2OUT	—	—	—	CCP2	PWM4	CWG1B CWG2B	SCK	—	CK	CLC2OUT	—
	—	—	—	—	—	—	—	—	—	PWM5	CWG1C CWG2C	SCL ^{(3),(4)}	—	TX	CLC3OUT	—
	—	—	—	—	—	—	—	—	—	PWM6	CWG1D CWG2D	SDA ^{(3),(4)}	—	—	CLC4OUT	—

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
 - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLV_{CFG} specific or SMBUS input buffer thresholds.

TABLE 6: 40/44-PIN ALLOCATION TABLE (PIC16(L)F15375, PIC16(L)F15376)

I/O ⁽²⁾	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC
RA0	2	17	19	19	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	CLCIN0 ⁽¹⁾
RA1	3	18	20	20	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	CLCIN1 ⁽¹⁾
RA2	4	19	21	21	ANA2	—	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—
RA3	5	20	22	22	ANA3	VREF+	C1IN1+	—	DACREF+	—	—	—	—	—	—	—	—
RA4	6	21	23	23	ANA4	—	—	—	—	TOCKI ⁽¹⁾	—	—	—	—	—	—	—
RA5	7	22	24	24	ANA5	—	—	—	—	T1G ⁽¹⁾	—	—	—	SSP1SS ⁽¹⁾	—	—	—
RA6	14	29	33	31	ANA6	—	—	—	—	—	—	—	—	—	—	—	—
RA7	13	28	32	30	ANA7	—	—	—	—	—	—	—	—	—	—	—	—
RB0	33	8	9	8	ANB0	—	C2IN1+	—	—	—	—	—	CWG1 ⁽¹⁾	SSP2SS ⁽¹⁾	ZCD1	—	—
RB1	34	9	10	9	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—
RB2	34	10	11	10	ANB2	—	—	—	—	—	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—
RB3	36	11	12	11	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—
RB4	37	12	14	14	ANB4 ADACT ⁽¹⁾	—	—	—	—	—	—	—	—	—	—	—	—
RB5	38	13	15	15	ANB5	—	—	—	—	—	—	—	—	—	—	—	—
RB6	39	14	16	16	ANB6	—	—	—	—	—	—	—	—	—	—	TX2 CK2 ⁽¹⁾	CLCIN2 ⁽¹⁾
RB7	40	15	17	17	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	—	RX2 DT2 ⁽¹⁾	CLCIN3 ⁽¹⁾
RC0	15	30	34	32	ANC0	—	—	—	—	SOSCO T1CKI ⁽¹⁾	—	—	—	—	—	—	—
RC1	16	31	35	35	ANC1	—	—	—	—	SOSCI	CCP2 ⁽¹⁾	—	—	—	—	—	—
RC2	17	32	36	36	ANC2	—	—	—	—	—	CCP1 ⁽¹⁾	—	—	—	—	—	—
RC3	18	33	37	37	ANC3	—	—	—	—	T2IN ⁽¹⁾	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—
RC4	23	38	42	42	ANC4	—	—	—	—	—	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—

TABLE 6: 40/44-PIN ALLOCATION TABLE (PIC16(L)F15375, PIC16(L)F15376) (CONTINUED)

I/O ⁽²⁾	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC
OUT ⁽²⁾	—	—	—	—	—	—	C1OUT	NCO1OUT	—	TMR0	CCP1	PWM3	CWG1A CWG2A	SDO1 SDO2	—	DT ⁽³⁾	CLC1OUT
	—	—	—	—	—	—	C2OUT	—	—	—	CCP2	PWM4	CWG1B CWG2B	SCK1 SCK2	—	CK1 CK2	CLC2OUT
	—	—	—	—	—	—	—	—	—	—	—	PWM5	CWG1C CWG2C	SCK1 ^{(3),(4)} SCL2 ^{(3),(4)}	—	TX1 TX2	CLC3OUT
	—	—	—	—	—	—	—	—	—	—	—	PWM6	CWG1D CWG2D	SDA1 ^{(3),(4)} SDA2 ^{(3),(4)}	—	—	CLC4OUT

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
 - 2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options.
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLV or SMBUS input buffer thresholds.

TABLE 7: 48-PIN ALLOCATION TABLE (PIC16(L)F15385, PIC16(L)F15386)

I/O ⁽²⁾	48-Pin UQFN/TQFP	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC
RA0	21	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	CLCIN0 ⁽¹⁾
RA1	22	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	CLCIN1 ⁽¹⁾
RA2	23	ANA2	—	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—
RA3	24	ANA3	VREF+	C1IN1+	—	DACREF+	—	—	—	—	—	—	—	—
RA4	25	ANA4	—	C1IN1-	—	—	T0CKI ⁽¹⁾	—	—	—	—	—	—	—
RA5	26	ANA5 ADACT	—	—	—	—	T1G ⁽¹⁾	—	—	—	SSP1SS ⁽¹⁾	—	—	—
RA6	33	ANA6	—	—	—	—	—	—	—	—	—	—	—	—
RA7	32	ANA7	—	—	—	—	—	—	—	—	—	—	—	—
RB0	8	ANB0	—	C2IN1+	—	—	—	—	—	CWG1 ⁽¹⁾	SSP2SS ⁽¹⁾	ZCD1	—	—
RB1	9	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—
RB2	10	ANB2	—	—	—	—	—	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—
RB3	11	ANB3	—	C1IN3- C2IN3-	—	—	—	—	—	—	—	—	—	—
RB4	16	ANB4 ADACT ⁽¹⁾	—	—	—	—	—	—	—	—	—	—	—	—
RB5	17	ANB5	—	—	—	—	—	—	—	—	—	—	—	—
RB6	18	ANB6	—	—	—	—	—	—	—	—	—	—	TX2 CK2 ⁽¹⁾	CLCIN2 ⁽¹⁾
RB7	19	ANB7	—	—	—	DAC1OUT2	—	—	—	—	—	—	RX2 DT2 ⁽¹⁾	CLCIN3 ⁽¹⁾
RC0	34	ANC0	—	—	—	—	SOSCO T1CKI ⁽¹⁾	—	—	—	—	—	—	—
RC1	35	ANC1	—	—	—	—	SOSCI	CCP2 ⁽¹⁾	—	—	—	—	—	—
RC2	40	ANC2	—	—	—	—	—	CCP1 ⁽¹⁾	—	—	—	—	—	—
RC3	41	ANC3	—	—	—	—	T2IN ⁽¹⁾	—	—	—	SSP1CLK ⁽¹⁾ SSP1DAT ⁽¹⁾	—	—	—

TABLE 7: 48-PIN ALLOCATION TABLE (PIC16(L)F15385, PIC16(L)F15386) (CONTINUED)

I/O ⁽²⁾	48-Pin UQFN/TQFP	ADC	Reference	Comparator	NCO	DAC	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC
V _{SS}	6	—	—	—	—	—	—	—	—	—	—	—	—	—
V _{SS}	31	—	—	—	—	—	—	—	—	—	—	—	—	—
VSELO	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT ⁽²⁾	—	—	—	C1OUT	NCO1OUT	—	TMR0	CCP1	PWM3	CWG1A CWG2A	SDO1 SDO2	—	DT ⁽³⁾	CLC1OUT
	—	—	—	C2OUT	—	—	—	CCP2	PWM4	CWG1B CWG2B	SCK1 SCK2	—	CK1 CK2	CLC2OUT
	—	—	—	—	—	—	—	—	PWM5	CWG1C CWG2C	SCK1 ^{(3),(4)} SCL2 ^{(3),(4)}	—	TX1 TX2	CLC3OUT
	—	—	—	—	—	—	—	—	PWM6	CWG1D CWG2D	SDA1 ^{(3),(4)} SDA2 ^{(3),(4)}	—	—	CLC4OUT

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
 - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLx registers. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLx specific or SMBUS input buffer thresholds.

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