AN11119

Medium power small-signal MOSFETs in DC-to-DC conversion

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Document information

Info	Content
Keywords	DC-to-DC converter, charge pump, buck converter, boost converter, small-signal MOSFET
Abstract	This application note explores different methods of DC-to-DC conversion. It includes some examples of DC-to-DC down-converters using small-signal MOSFETs.

Revision history

Rev	Date	Description
3	20130507	Corrected typo on page 13 (changed 0.68 μH to 6.8 μH)
2	20120705	Figure 24: changed
1	20120504	Initial revision

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1. Introduction

In modern electronic designs various supply voltages need to be generated. In most cases power supply provides one or a few different DC voltages. These voltages need to be converted to another voltage for several functional units in the application. Voltage conversion can work in both directions: it can be step up or step down. This application note presents different methods of DC-to-DC conversion.

Using linear voltage regulators for voltage conversion was common, even if a voltage had to be reduced significantly or if the load currents were high. Because linear voltage regulator works as a controlled series resistor, a lot of energy is dissipated thermally.

Due to the environmental requirement to improve energy efficiency of electronic equipment, Switch mode power supplies are replacing linear voltage regulators. In Switch mode power supplies, energy is stored in the magnetic field of inductors or as a charge in capacitors. Ohmic loss of energy has to be avoided as much as possible.

Newly developed electronic components for implementation of switches, such as modern MOSFETs, support design of highly efficient power supplies. Small-signal MOSFETs with low drain-source on-state resistance R_{DSon} values and good switching performance open a new application area for medium power Switch mode DC-to-DC conversion. Although fully integrated solutions are available, applications with external switching stages are widely used due to flexibility and cost reasons.

2. DC-to-DC conversion methods

2.1 Linear voltage regulation

Although Switch mode power supplies are replacing linear voltage regulators, there are many application areas where this approach is still used. Linear voltage regulators are found where the output voltage needs to be free from switching ripple and overlaid distortion. Supply for analog-to-digital converters (ADC) and digital-to-analog converters (DAC) and analog circuit parts with high signal-to-noise requirements are good examples. Often such stabilizers are put behind Switch mode voltage converter to achieve a very clean output voltage for the circuit block behind.

Figure 1 presents simple circuit diagram for voltage stabilizer. The output voltage is:

$$V_{OUT} = V_Z - V_{BE} \tag{1}$$

where V_Z is Zener voltage and V_{BE} is base-emitter voltage of transistor T1.

The transistor has total power dissipation:

$$P_{tot} = (V_{IN} - V_{OUT}) \times I_{load} + V_{BE} \times I_B \tag{2}$$

The first part of the addition contains dominating part of the losses. It increases with voltage difference from the input to the output and the load current. In this circuit example, an NXP Semiconductors low collector-emitter saturation voltage V_{CEsat} transistor is applied. It offers high and constant gain amplification. This means low dependency on DC current gain h_{FE} versus collector current and the advantage of low V_{CEsat}.

This design is beneficial because it keeps voltage drop across the regulator as small as possible. Linear voltage regulators that need low voltage on top of the output voltage for proper stabilization are called low dropout regulators (LDO).

Along with minimum dropout voltage, the quiescent current I_q is an important parameter with respect to the energy efficiency. This parameter defines the current that flows into the circuit when no load is present.

$$I_q = (V_{IN} - V_Z)/R1 \tag{3}$$

A circuit example:

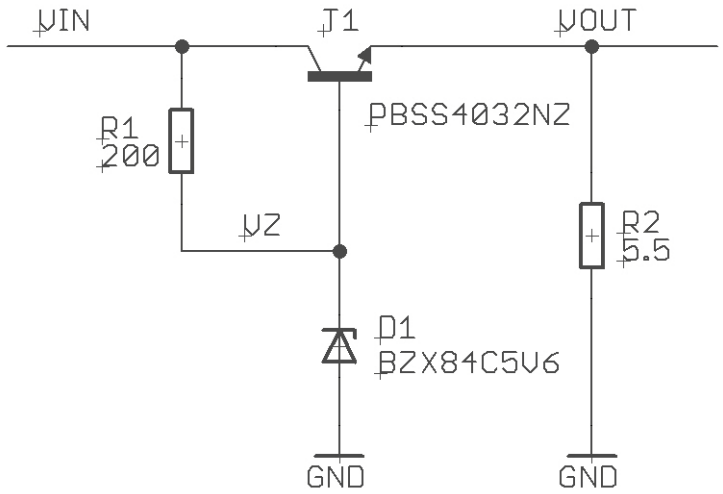


Fig 1. Simple linear voltage regulator with Zener diode and BISS transistor in the load path.

If requirements for quality of the line and load regulation are high, more sophisticated circuits need to be used. These contain voltage reference with high temperature stability and more precise feedback control with an error amplifier.

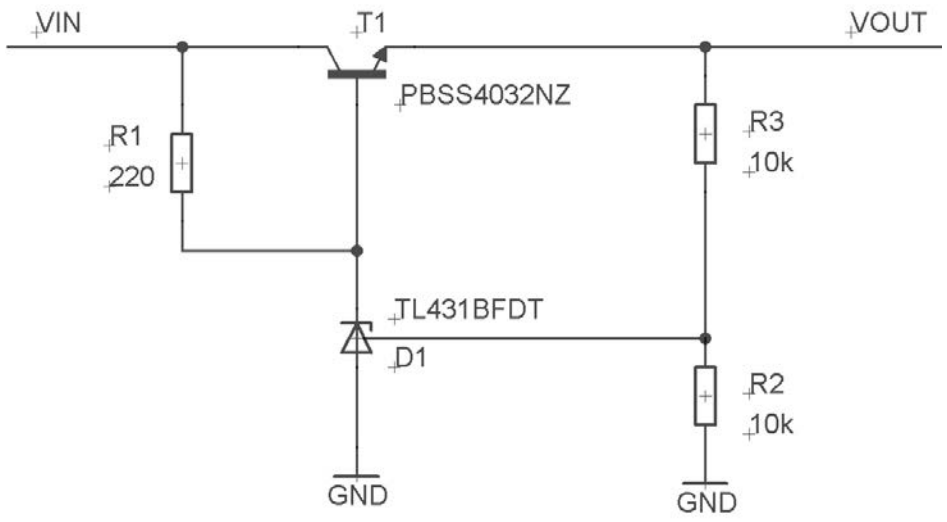


Fig 2. Linear voltage regulator with a TL431BFDT as an error amplifier

Figure 2 shows an example using TL431BFDT shunt regulator as an error amplifier with an external series load regulation transistor.

For additional features such as protection against thermal damage and current limitation, typical choice is an integrated regulator. An example of such a device is NX1117. Maximum nominal output current is 1 A. Dropout voltage is the difference between V_{IN} and V_{OUT}. Maximum dropout voltage of NX1117 is 1.2 V for 800 mA load current.

LDOs specifications contain additional key parameters. Line regulation parameter shows output voltage change in response to input voltage change. Output regulation states stability of the output voltage for different load currents, for example 0 mA versus 800 mA. Ripple rejection indicates reduction of a ripple after rectification achieved with Graetz bridge and a capacitor added at the output. Therefore this parameter is measured for 120 Hz sine wave overlaid onto input voltage. This is a scenario adapted to 60 Hz line supply system. An additional parameter is stability of the output voltage versus temperature and spread of nominal output voltage for an LDO at a nominal operating point.

Figure 3 shows a simple example with adjustable version of NX1117. V_{OUT} can be calculated as:

$$V_{OUT} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj} \cdot R1 \quad (4)$$

Adjust current I_{adj} is typically 50 μA for NX1117 and therefore the second term can be neglected. Reference voltage V_{ref} is 1.25 V for the adjustable NX1117. In addition to adjustable type many regulator types with fixed output voltages are available. In this case, the reference pin is connected to the ground and divider with R1 and R2 is integrated.

The dissipated power of fixed regulator is:

$$P_{tot} = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (5)$$

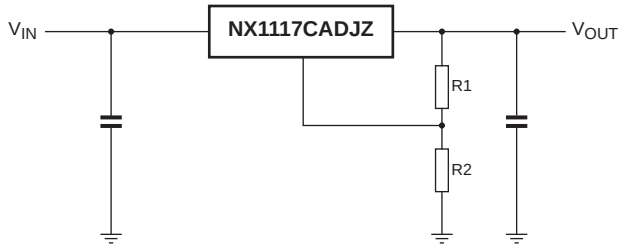


Fig 3. Adjustable linear voltage regulator NX1117CADJZ

2.2 Voltage conversion with a charge pump

In some applications, a simple voltage inversion or a doubling of voltage is required. Sometimes only a low current is needed. An example of such application is generation of negative voltage for operational amplifier or comparator or boosted voltage for high-side switch of a buck converter. The latter topology is discussed in more detail further in this document. Usage of charge pumps is a common method of DC-to-DC conversion without disadvantage of generating large losses. Charge pumps use capacitors for energy storage. The principle is that a capacitor is charged and then shifted up or down to obtain a higher voltage or to get an inverted voltage.

Figure 4 shows an example of such circuit on condition of ideal diodes without forward voltage loss. A generator is providing a square wave signal. It delivers a signal with low level of 0 V and high level of V_{IN}. If the generator outputs a high signal, C2 is charged. When the generator output switches to the ground, the positive pole of the capacitor is connected to the ground. Due to the charged capacitor, the node where C2 is connected to the cathode of D4 and the anode of D2 has a voltage level of V_{IN}. The diode D4 becomes conductive and C4 is charged to negative voltage. V_{OUT2} becomes inverted V_{IN} after a few cycles.

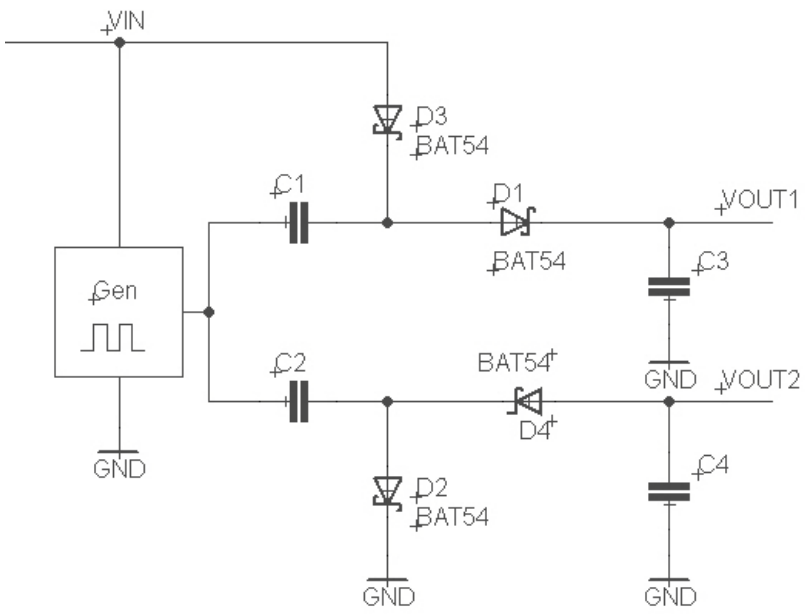
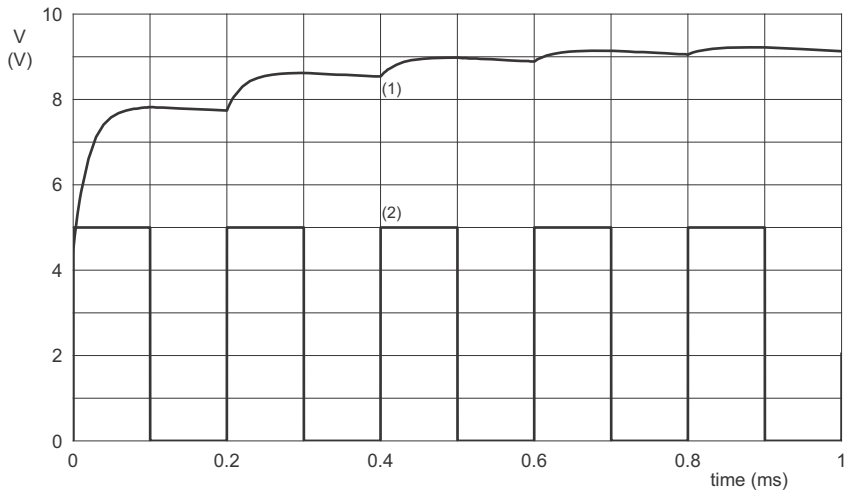


Fig 4. Charge pump diagram with inverted and doubled output voltage

When the output of the generator is at low level, C1 is charged to V_{IN} via D3 through the upper signal path. Also C3 gets charged to V_{IN} via D3 and D1. When the output changes to the high state, the negative pole of the charged capacitor is shifted up to V_{IN}. Capacitor C3 is charged to double V_{IN} in the ideal case after a few switching cycles.

In practice, forward voltage of diodes reduces output voltage. This means that output voltage of the discussed voltage doubling is decreased by twice V_F compared to lossless and ideal condition.



(1) V_{OUT}

(2) V_{IN}

Fig 5. Voltage doubling with a charge pump, BAT54 Schottky diodes

Figure 5 shows simulation result for the start-up of voltage doubling with charge pump and BAT54 Schottky diodes. The input voltage V_{IN} is 5 V, capacitor C1 is 22 μF and C3 is 10 μF. The load is 1 kΩ. The trace shows that theoretical output voltage of 10 V is not reached. If such a circuit has low supply voltage, forward voltage losses of diodes become a significant problem. In order to improve it, switches, which are usually implemented with MOSFETs, can replace diodes.

2.3 Topologies of voltage converters with inductances

Application areas of charge pumps described in previous chapter are usually limited to low current applications. For higher output power and highly energy-efficient voltage converters, the best solution is topology with inductors. With a small topology modification down-, up- and up-down converters can be implemented.

2.3.1 DC-to-DC down-converter

Figure 6 shows the circuit diagram of a simple DC-to-DC down-converter. In contrast to a linear regulator, this circuit would have 100 % efficiency in case of ideal components application. In practice, there are losses in switching transistor because the on-resistance is not equal to 0 Ω and also because transistor needs switching time, which introduces switching losses. Other components add losses too. Inductor has an ohmic resistance from the wire of the windings and magnetic core adds losses too. Magnetic core losses result from the change of the magnetic field which causes motion of small magnetic domains. The bigger the hysteresis of the core material, the bigger are these losses. Eddy currents cause further loss in the magnetic core of an inductor. Changing magnetic fields can induce circulating loops of current which heat up the ferromagnetic material. For high frequency switching, the current in the wire no longer uses the whole cross-section, instead it concentrates closer to the surface. This is a well-known skin effect which leads to higher ohmic losses.

Also the output capacitor has a residual resistance that leads to energy losses and a temperature increase. Finally, the diode introduces forward voltage losses and reverse current losses. These mechanisms and facts reduce the energy efficiency of DC-to-DC converters from 75 % to 98 % in real life conditions.

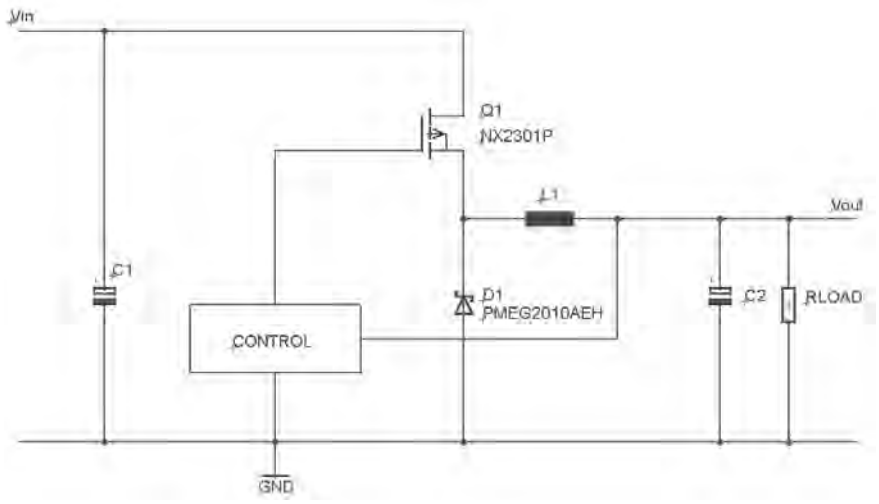


Fig 6. Simple DC-to-DC down-converter

The P-channel FET Q1 works as high-side switch. When the FET is switched on, the current in the inductor L1 increases with a linear curve $\Delta I_L = (t_{on}/L1) \times (V_{IN} \cdot V_{OUT})$, V_{OUT} is constant.

When the switch is opened, the current continuously flows via the path of the diode D1. The cathode of D1 is negative with the forward voltage V_F against ground. The current decreases linearly. C2 buffers the output voltage. The bigger it is, the smaller the ripple will be.

Figure 7 depicts a SPICE simulation. The high-side switch is implemented with NX2301P P-channel FET. It works at the voltage supply V1. The inductance of the inductor is chosen to 68 μH, the output voltage is filtered with 10 μF capacitor. PMEG2010AEH Schottky diode is selected as a free-wheeling diode. To control NX2301P, a N-channel driver FET is implemented, which is switched from a square wave generator with 3.3 V high level (V2). In this example, the switching frequency is 100 kHz. A load resistor of 10 Ω is connected to the output.

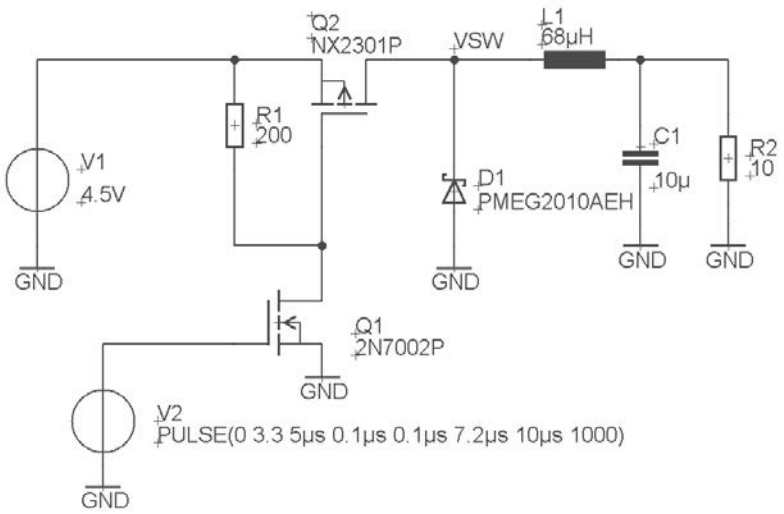


Fig 7. SPICE simulation diagram for a simple DC-to-DC down-converter using NX2301P as high-side switch and PMEG2010AEH as low-side Schottky diode.

Figure 8 shows simulation result. The current I_{L1} which flows through the inductor shows a linear increase while Q1 is switched on. The voltage at SW node V_{SW} nearly equals to the input voltage. When Q1 is switched off, the current through the inductor decreases. The signal SW changes to a negative voltage of about 300 mV, which is the forward voltage of the Schottky diode. The output current is the average of the triangle shaped waveform and is about 330 mA. The output voltage V_{OUT} is stable at roughly 3.25 V.

In the abovementioned example, the current flows through the inductance for the whole period of the switching cycle. This mode is called continuous mode of a DC-to-DC converter. Below is a calculation of output voltage. The voltage at an inductor is:

$$V_L = L \times (dIL/dt) \quad (6)$$

or

$$V_L = L \times (\Delta I_L/\Delta t) \quad (7)$$

so

$$\Delta I_L = V_L / L \times \Delta t \quad (8)$$

The stored energy in an inductor is:

$$E = L / 2 \times I^2 \quad (9)$$

For the Stationary mode while switch is closed, the energy increase in the inductor must be identical to the energy loss while switch is open.

Neglecting R_{DSon} losses in the switch and the forward voltage of the diode, we get the formula for ΔI_L:

$$\Delta I_L = (V_{IN} - V_{OUT}) \times t_{on} = V_{OUT} \times t_{off} \quad (10)$$

$$V_{OUT} / V_{IN} = t_{on} / (t_{on} + t_{off}) = t_{on} / T \quad (11)$$

where T is cycle time and the duty cycle D is:

$$D = t_{on} / T \quad (12)$$

$$V_{OUT} = V_{IN} \times D \quad (13)$$

In our example:

$$V_{OUT} = 4{,}5\ V \times (7{,}2 / 10) = 3{,}24\ V \quad (14)$$

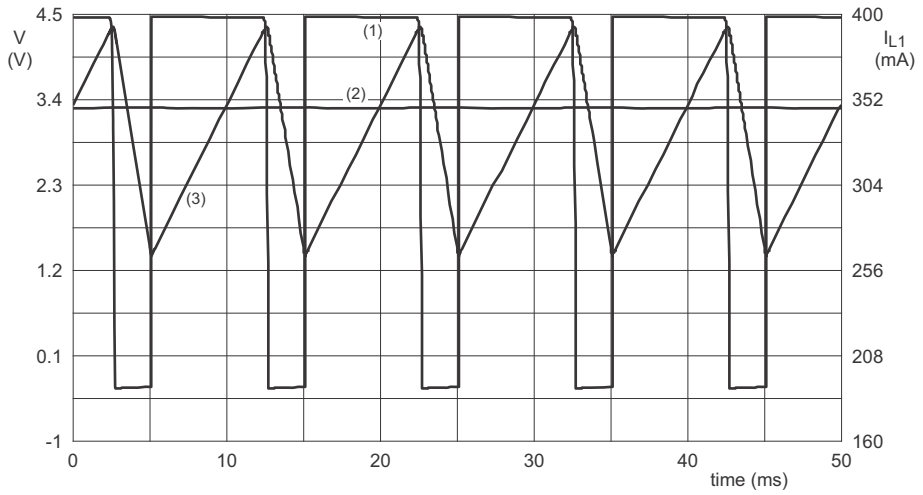
If the duty cycle is 1 as a corner case, the switch is always closed and the output voltage equals the input voltage. If the duty cycle is smaller than 1, the output voltage is reduced by factor D.

The ripple of the current is:

$$\Delta I_L = (V_{IN} - V_{OUT}) / L \times t_{on} \quad (15)$$

In our example:

$$\Delta I_L = (4{,}5\ V - 3{,}24\ V) / 68\ \mu H \times 7{,}2\ \mu s = 133\ mA \quad (16)$$



(1) V_{SW}

(2) V_{OUT}

(3) I_{L1}

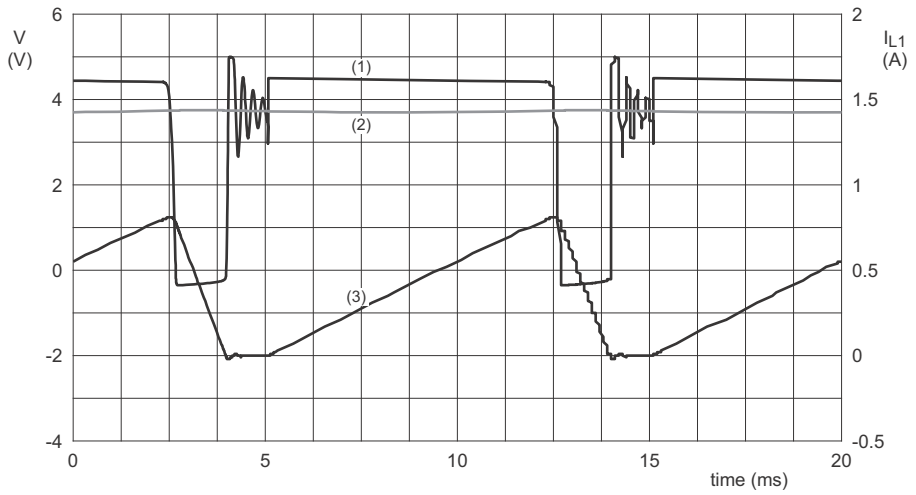
Fig 8. Curves of the current through L1, SW node voltage and output voltage

If the load current is increased in the continuous mode, the output voltage stays constant (ideal components) . This means that duty cycle for the switch does not need to be changed to a significant extent from a DC-to-DC controller IC as long as the converter runs in the continuous mode. There is a current limit where the continuous mode is left. A relevant equation is below:

$$\Delta I_L = 2 \times I_{L(average)} = 2 \times I_{load} \quad (17)$$

If curve 3 on Figure 8 moves down by decreasing the output current until the x-axis is touched, the limit of the continuous mode is reached. From this point onward the duty cycle has to be reduced in order to keep the same output voltage.

If non-continuous mode is reached, the voltage curve of SW node of the circuit changes significantly. Normally there is roughly a square wave between V_{IN} and $-V_F$. If the current through the inductance reaches 0 A, the voltage at the diode changes from forward direction to reverse. The diode blocks the output capacitor, which is charged to V_{OUT} from being discharged via L1 (Q1 is still closed). After the current through L1 went down to zero, SW node shows an oscillation supported by the resonance circuit of L1 and C_{OUT}. Figure 9 shows this typical behavior. Circuit on Figure 7 was modified by reducing the inductance of L1 to 6.8 μH for this experiment. This leads to a higher current ripple, and a non-continuous mode.



(1) V_{SW}

(2) V_{OUT}

(3) I_{L1}

Fig 9. Converter in a non-continuous condition, current curve of I_L reaches the x-axis at 0 A, curve of SW node jumps from $-V_F$ to an oscillation around V_{OUT}

Figure 10 shows a change in the down-converter topology to improve efficiency of the simple circuit. The Schottky diode generates forward voltage losses for the time period when high-side switch is opened. A MOSFET can replace a diode. The low-side switch needs to be turned on when the upper FET is switched off. The controller has to take care that there is never an overlap of the on-states of both transistors in this case the switching stage would create a short circuit with a significant current peak, high losses and risk to damage the FETs. Because every MOSFET contains a body-diode from the source to the drain, the circuit would in principle work even if Q2 is never switched on. In this case, the body-diode of Q2 would work like a Schottky diode in the simple topology on Figure 6. Therefore the turn-on time of Q2 is not very critical. If Q2 switches on after Q1 is closed, the body diode conducts the current from L1.

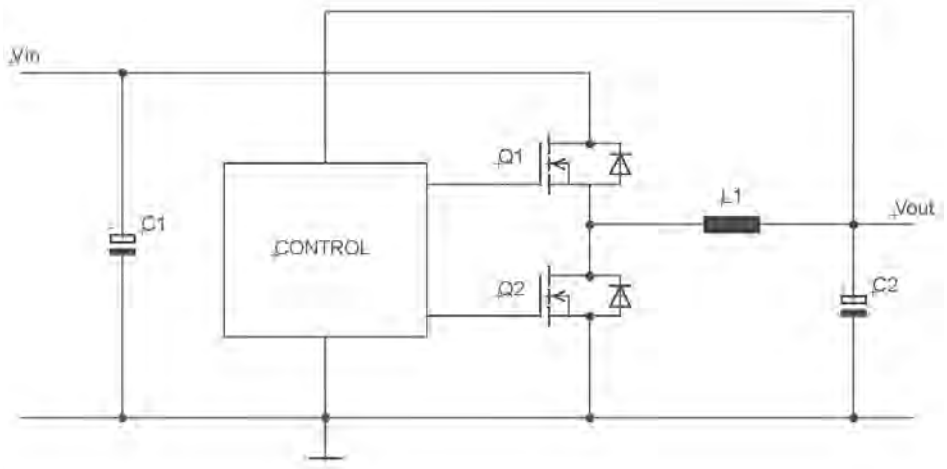


Fig 10. Synchronous DC-to-DC down-converter (FETs including body-diodes)

2.3.2 DC-to-DC up-converter

In the previous chapter, inductor-based DC-to-DC down conversion was discussed. With a small change in the topology, the down-converter can be changed into an up-converter. Figure 11 shows the topology of a simple DC-to-DC up-converter. If the low-side switch FET Q1 is closed, the current in the inductance increases:

$$\Delta I_L = V_{IN} \times t_{on} \tag{18}$$

The diode D1 is driven in reverse mode because the anode is connected to the ground and the cathode is connected to the positive voltage V_{OUT} at C2. If the switch is closed, the current I_L continues to flow through D1 into the output. If the converter runs in a stationary mode, we can calculate:

$$\Delta I_L = V_{IN}/L \times t_{on} = (V_{OUT} - V_{IN})/L \times t_{off} \tag{19}$$

$$V_{IN} \times t_{on} = (V_{OUT} - V_{IN}) \times t_{off} \tag{20}$$

$$V_{OUT} = V_{IN} \times (t_{on}/t_{off} + 1) \tag{21}$$

where the duty cycle is:

$$D = t_{on}/T \tag{22}$$

$$T = t_{on} + t_{off} \tag{23}$$

$$\begin{aligned} V_{OUT} &= V_{IN} \times (t_{on} + t_{off})/t_{off} = V_{IN} \times T/(T - t_{on}) \\ &= V_{IN} \times 1/(1 - t_{on}/T) \\ &= V_{IN} \times 1/(1 - D) \end{aligned} \tag{24}$$

The corner cases of the equation show that for D = 0, which means that the transistor is never switched on, $V_{OUT} = V_{IN}$. It makes sense to consider lossless components. Lossless means a diode with no forward voltage and an inductance without an ohmic resistance of the windings and the additional loss mechanisms discussed in the previous chapter. If D gets close to 1, the output voltage increases rapidly. This is critical for safe operation because high duty cycle can result in very high voltages at the FETs drain.

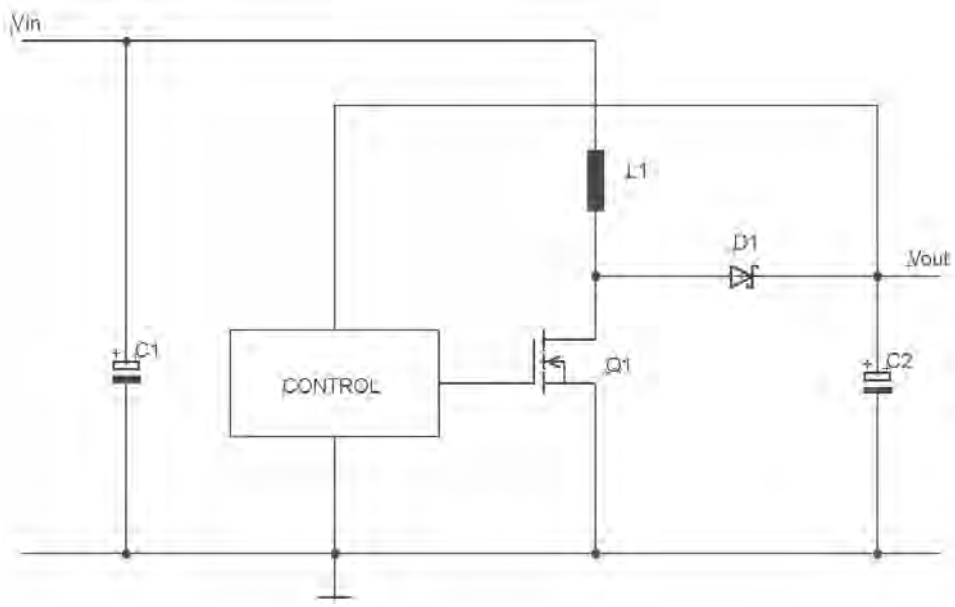


Fig 11. Simple DC-to-DC up-converter

Figure 12 shows SPICE simulation. The low-side switch is implemented with PMV20XN N-channel MOSFET in SOT23 package and PMEG2010AEH Schottky diode. The converter is switched with 100 kHz signal control signal with a duty cycle of 0.5.

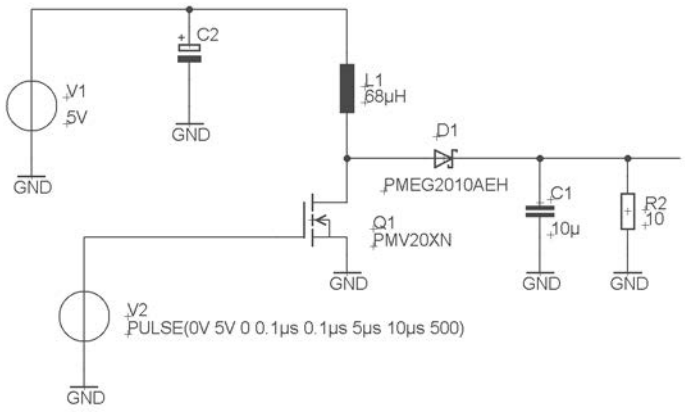
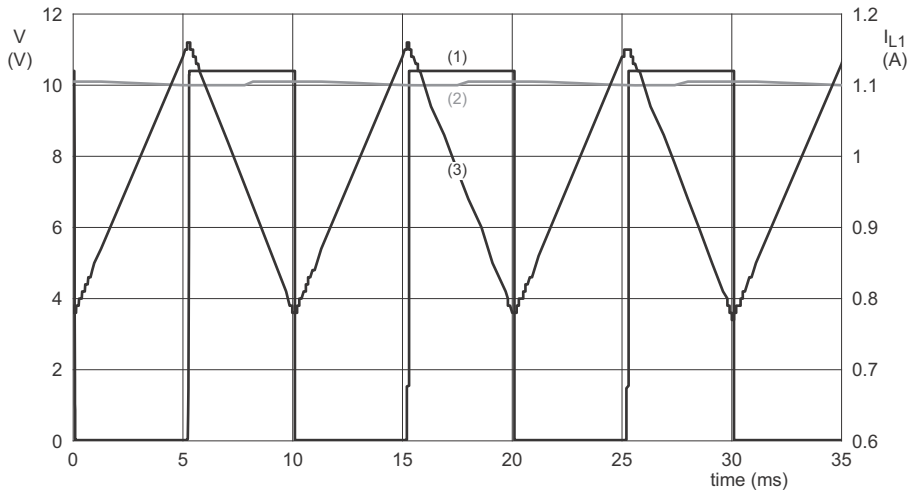


Fig 12. SPICE simulation diagram for a simple DC-to-DC up-converter with PMV20XN N-channel FET and PMEG2010AEH Schottky diode

Figure 13 shows simulation results. Curve 2 represents output voltage. For ideal components, the output voltage would be twice as high as the input due to the duty cycle of 0.5. In practice, the forward voltage of the diode reduces the output voltage. Curve 1 shows drain voltage V_D of the N-channel FET. It switches between ground level and $V_{D(max)}$ and equals:

$$V_{D(max)} = V_{IN} \times 1/(1 - D) + V_F \quad (25)$$

In the simulated case with the duty cycle D = 0.5, $V_{D(max)} = 2 \times V_{IN} + V_F$.



(1) V_D

(2) V_{OUT}

(3) I_{L1}

Fig 13. Simulation results, simple up-converter

Similar to DC-to-DC down-converter, energy efficiency of the up-converter also can be improved if the Schottky diode is replaced by a FET, which switches on for the correct phase in the switching cycle. Figure 14 shows the topology of synchronous DC-to-DC up-converter.

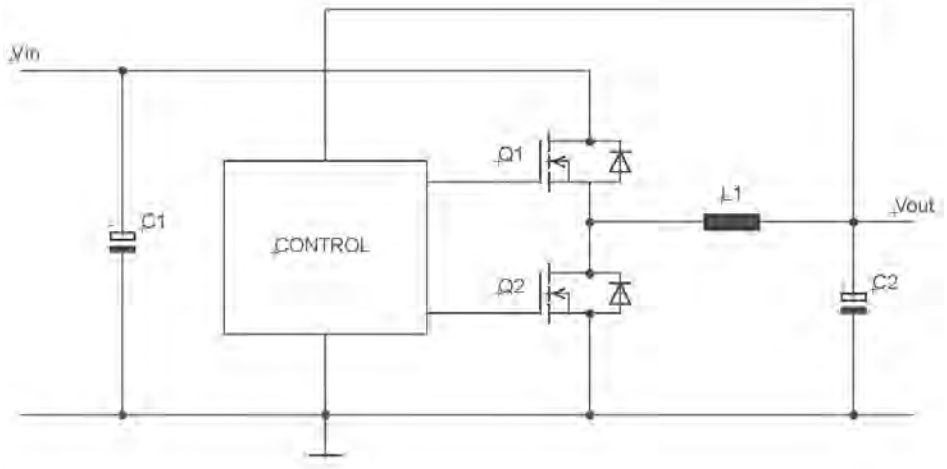


Fig 14. Synchronous DC-to-DC down-converter

2.3.3 DC-to-DC up- and down-converter

If two topologies of the DC-to-DC down-converter and up-converter are combined as shown on Figure 15, the output voltage can either be reduced or boosted in relation to the input voltage. The MOSFET switches need to be controlled in a proper way to allow the conversion in both directions. Q3 and Q4 can switch similarly to the DC-to-DC down-converter shown on Figure 10. In addition, Q2 must be switched on constantly to connect the inductor to the output capacitor. For the up-conversion mode, MOSFETs Q2 and Q1 work as the switching stage, as described for the synchronous up-converter on Figure 14. The MOSFET Q3 is constantly switched on to connect the inductor to the input supply voltage in this case.

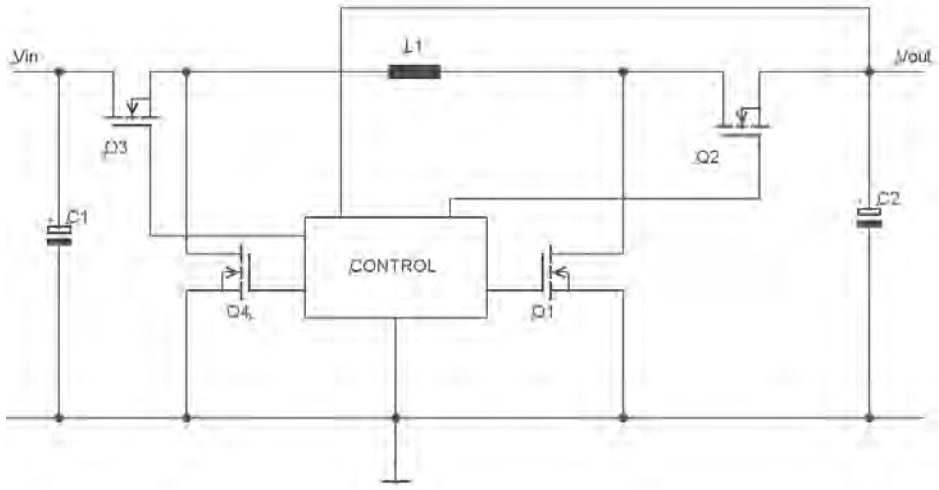


Fig 15. Up-down converter

3. Medium power DC-to-DC down-converter using small-signal MOSFETs

3.1 DC-to-DC down-converter application board

Figure 16 shows an application Printed-Circuit Board (PCB) with NXP Semiconductors small-signal MOSFETs implemented in a DC-to-DC step-down converter. NXP Semiconductors offers small-signal MOSFETs in small SMD packages such as SOT457, SOT23, SOT223 and DFN2020MD-6 (SOT1220). Many of these MOSFETs provide very low R_{DSon} together with a good switching performance.

The topology of the application board on Figure 16 is a synchronous down-converter same as in Section 2.3.1. The circuit contains a controller LTC3851 of Linear Technology Corporation. Two N-channel MOSFETs build switching stage. The high-side switch connects the node with the inductor to the input supply. Therefore, it is necessary to have a control voltage available that is higher than the input voltage itself. This extra voltage for the control of the gate of the upper MOSFET is generated with a charge pump. The capacitor C25 is connected to the SW node, the switched output and via Schottky diode to a stabilized voltage INTVCC (pin 12). INTVCC is provided by an internal 5 V LDO. The capacitor is charged via the diode when the low-side switch is turned on. In this case, one side of C25 is connected to ground. If Q2 is turned off and Q1 is switched on, the charged

capacitor gets connected to V_{IN}. At the pin BOOST (pin 14) a voltage of V_{IN} + INTVCC − V_F (forward voltage of the diode) can be measured. This boosted voltage can drive the high-side switch properly. Low current Schottky diodes are sufficient for the charge pump (for example, BAT54J, 1PS76SB40 or 1PS76SB21). These diodes are supplied in the SMD packages like SOD323F and SOD323.

The LTC3851 controller contains a 0.8 V precision reference voltage for the output voltage regulation. The output of the down-converter is fed back to the pin FB. A resistor divider formed by R41 + R39 and R38 adjusts the output voltage.The equation for the output voltage is:

$$V_{OUT} = 0{,}8\ V \times (1 + (R41 + R39)/R38) \tag{26}$$

The controller works with a constant frequency. As described in Section 2.3.1, the output voltage of DC-to-DC down-converter can be controlled rather easily for higher currents, but low current conditions are more ambitious for the control. The duty cycle needs to be changed significantly or the controller can change to a different control mode like burst operation. For the LTC3851 there are three options: forced continuous operation, burst mode operation and a pulse-skip mode.

Burst mode operation gives better efficiency, but more ripple and a higher ElectroMagnetic Interference (EMI) level. The best mode depends on the specification and requirements of the end application.

The switching frequency can be programmed in a range from 250 kHz to 750 kHz. The resistor R30 determines the frequency. Alternatively the controller can synchronize the internal oscillator to an external clock source (MODE/PLLIN, pin 1). In this mode an RC network needs to be connected to pin 2 (FREQ), which serves as PLL loop filter.

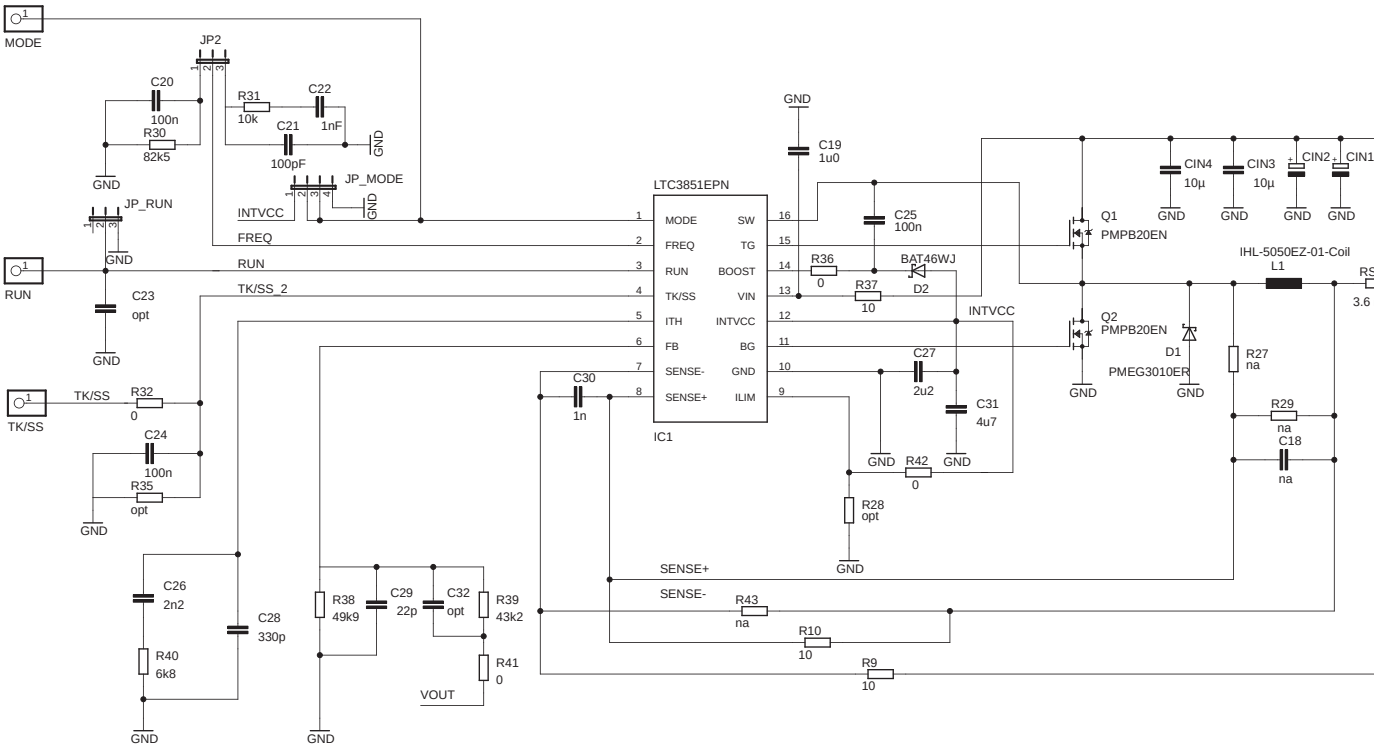


Fig 16. Circuit diagram for reference application of DC-to-DC down-converter with NXP Semiconductors small-signal M LTC3851 as controller

3.2 NXP Semiconductors small-signal MOSFETs suitable for DC-to-DC conversion

DC-to-DC converters can be found in many applications. Topology of step-down converter controller with an external FET stage are often implemented in computing and consumer applications. Modern concepts with latest generation SOC (System-on-Chip) solutions require many separate supply voltages. These can be processors on motherboards, in notebooks and tablet PCs, on core chips of LCD-TV or a set-top box.

The power requirements range from more than hundred watts down to a few watts. In desktop PCs, DC-to-DC converter can be found on the motherboard which provide a current capability of up to 100 A and an output power of up to 130 W. MOSFETs in switching stages are Loss-Free Package (LFPAK) types and to a growing extent Quad Flat-pack No-lead (QFN) 5 × 6 packages. For net- and notebooks the power requirements are smaller. The power consumption ranges from 18 W to 55 W. The switching MOSFETs are mainly SO-8 and QFN 3 × 3 types. In consumer applications such as LCD-TVs and set-top boxes as well as in low-power netbooks or tablet PCs, power requirements from 7 W to 15 W can be found.

For medium power range small-signal MOSFETs can replace SO-8 versions nowadays in smaller packages like QFN 3 × 3, but also in QFN 2 × 2 or SOT457.

3.3 Dimensioning aspects for the inductor and output capacitor

In order to reach a desired current ripple, choose carefully inductance of the inductor used in the down-converter. With a bigger current ripple, the output voltage shows a larger ripple. The ripple increases the smaller the inductance becomes and the higher the input voltage is. Furthermore it increases if the switching frequency is reduced.

ΔI_L can be calculated:

$$\Delta I_L = V_{IN}/L \times t_{on} = V_{OUT}/L \times t_{off} \quad (27)$$

with:

$$T = t_{on} + t_{off} = 1/f \quad (28)$$

we get:

$$\Delta I_L = (V_{OUT}/L) \times (1 - V_{OUT}/V_{IN}) \times 1/f \quad (29)$$

this means:

$$L = (V_{OUT}/\Delta I_L) \times (1 - V_{OUT}/V_{IN}) \times 1/f \quad (30)$$

For the corner case in which circuit runs at the limit of the continuous mode, current goes down exactly to zero before it increases again and we get simple relation:

$$\Delta I_L = 2 \times I_{average} \quad (31)$$

Putting equasion 32 into the formula for ΔI_L:

$$L = V_{OUT} \times (1 - V_{OUT}/V_{IN})/2 \times I_{average} \times f \quad (32)$$

In practice, the ripple current ΔI_L is about 30 % of the maximum current, as a rule of thumb.

The ripple of the output voltage does not depend on the chosen inductance and the ΔI_L only, but also on the capacitance of the output capacitor. The bigger the capacitor, the smaller the ripple is. Figure 17 shows the waveform of the current into the capacitor. For a lossless capacitor, there is basic equation:

$$Vc = \frac{1}{C} \times \int_{to}^{t2} Ic \times dt \quad (33)$$

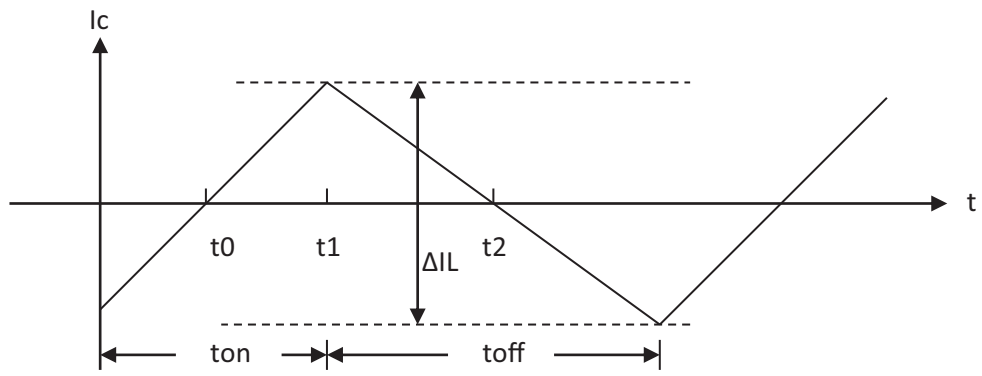


Fig 17. Capacitor current I_C versus time

For t0 to t1:

$$I_C = \Delta I_L / t_{on} \times t \quad (34)$$

and for t1 to t2

$$I_C = \Delta I_L / t_{off} \times t \quad (35)$$

the integral formula for the capacitor ripple voltage can be written as:

$$V_{Cpeak} = \frac{1}{C} \int_{0}^{\frac{ton}{2}} \left(\frac{\Delta I_L}{t_{on}} \cdot t \right) dt + \frac{1}{C} \int_{0}^{\frac{toff}{2}} \left(\frac{\Delta I_L}{t_{off}} \cdot t \right) dt \quad (36)$$

With:

$$T = t_{on} + t_{off} = 1/f \tag{37}$$

the result is:

$$V_{C\_ripple} = \Delta I_L/(C \times 8 \times f) \tag{38}$$

For real capacitors take into account an Equivalent Series Resistance (ESR). So we get an equation:

$$V_{C\_ripple} = \Delta I_L \times (ESR + 1/(8 \times f \times C_{out})) \tag{39}$$

3.4 MOSFET losses calculation

For MOSFETs used as switches consider two loss processes. One is the ohmic loss caused by the residual on-state resistor R_{DSon}. The second loss process happens at the switching transients. Because FETs are not ideal switches that can change from off- to on-state or reverse without a small turn-over time.

The R_{DSon} losses are also called I^2R-losses and they can be calculated:

$$P_{up\_side\_switch} = D \times (I_{OUT})^2 \times (1 + \delta) \times R_{DSon} = V_{OUT}/V_{IN} \times (I_{OUT})^2 \times (1 + \delta) \times R_{DSon} \tag{40}$$

with duty cycle:

$$D = t_{on}/T \tag{41}$$

The term 1+δ contains the temperature dependency of R_{DSon} of a MOSFET. δ has typically a value of:

$$\delta = (0,005/°C) \times (T_j - 25°C) \tag{42}$$

For the low side switch, there is a similar formula. Because synchronous FET is conducting while the high-side switch is closed, the I^2R looses can be calculated with the equation:

$$P_{low\_side\_switch} = (1 - D) \times (I_{OUT})^2 \times (1 + \delta) \times R_{DSon} = 1 - (V_{OUT}/V_{IN}) \times (I_{OUT})^2 \times (1 + \delta) \times R_{DSon} \tag{43}$$

Regarding the transition losses, only the high-side switch suffers from this mechanism. The reason is that the implemented free-wheeling diode (D1 on Figure 16) is getting conductive. It reduces the voltage over the synchronous FET to its small forward voltage V_F. If the circuit does not contain a free-wheeling diode, the situation is different: losses of the body diode need to be added to the R_{DSon} losses of the FET. In general, efficiency suffers from the higher V_F and reverse recovery time of the body diode if there is no free-wheeling Schottky diode implemented.

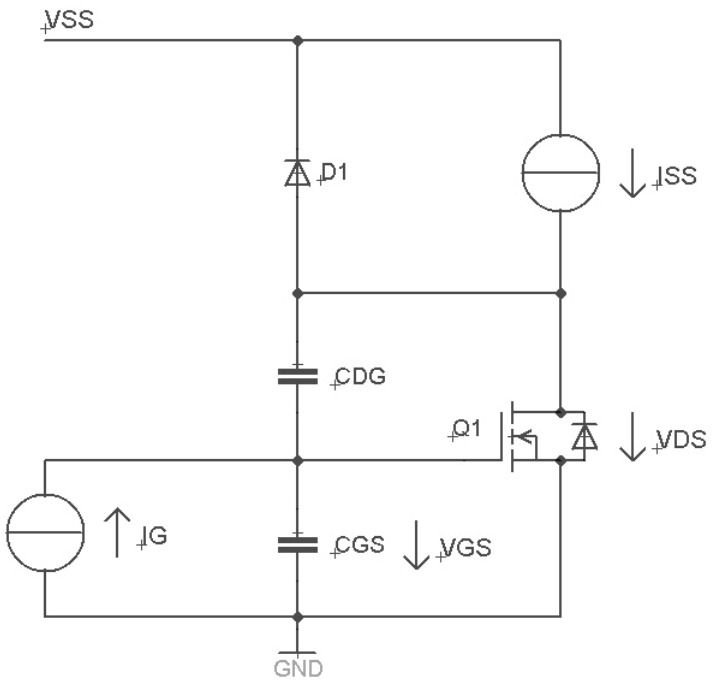


Fig 18. Diagram for switching behavior tests for MOSFET

Figure 18 shows a test circuit for the switching behavior of a MOSFET. The parasitic capacitors from the gate to the source C_{GS} and from the drain to the gate C_{DG} are depicted explicitly. Current source I_G controlls gate. At the drain another current source is connected towards V_{SS} with a free-wheeling diode in parallel. As long as the FET is closed, the current flows through this diode.

Figure 19 shows how the switching-on process looks like. If the current source I_G is switched on, voltage at C_{GS} rises with a linear curve until gate-source threshold voltage $V_{GS(th)}$ is reached. At this time a drain current starts to flow. This means that the FET remains in the off-state during the time period t0.

During t1 the drain current increases. Also the gate voltage increases until $V_{GS(pl)}$ is reached. $V_{GS(pl)}$ is commonly known as plateau voltage of a MOSFET. It is normally not explicitly mentioned in data sheets, but it can be derived from the diagram gate charge versus gate-source voltage which can be found in detailed data sheets. After the time period t0 and t1, the charge is $Q0 = V_{pl} \times (C_{GS} + C_{DS})$.

In the next time period t2, the drain voltage decreases and gate-source voltage V_{GS} stays constant at $V_{GS(pl)}$. C_{DS} gets charged in the reverse direction with the charge Q1 which is:

$$Q1 = V_{SS} \times C_{DS} \tag{44}$$

C_{DS} is similar to the Miller capacitance known from bipolar transistors and has a significant impact on the switching performance of a MOSFET.

During t3 the gate voltage increases again until the current source is stopped where the desired maximum gate voltage is reached. The R_{DSon} of the FET is reduced further. The gate driver provides an additional charge Q2, which is:

$$Q2 = (V_{GS(t4)} - V_{GS(pl)}) \times (C_{GS} + C_{DS}) \quad (45)$$

The total charge follows the equation: $Q_G = Q0 + Q1 + Q2$

This charge can easily exceed 100 nC for a power MOSFET. With the equation:

$$I_G = Q_G / t_s \quad (46)$$

the gate current can be calculated to achieve a switching time t_s. Therefore, if small transition times are desired, in order to keep the switching losses small, apply powerful drivers to controll MOSFETs.

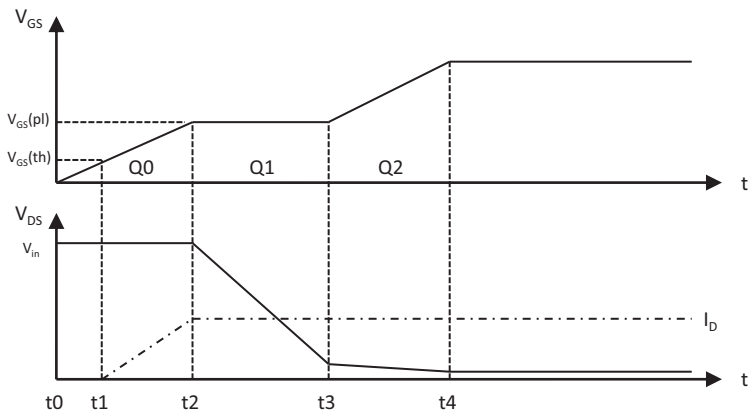


Fig 19. Turn-on process for MOSFET, V_{GS}, V_{DS} and I_D curves

During the time t1, there is the full input voltage at the FET while drain current I_D increases. In the next time section t2, I_D is constant while drain-source voltage V_{DS} decreases. The major switching losses occur during these two timw periods in the switching process. Rather small losses during t3 are neglected. During t3 R_{DSon} falls to the minimum value that is reached when the final V_{GS} voltage is reached.

Switching losses during turn-on occur in the time period t1 and t2. The most dominant time is t2 where the gate voltage of the MOSFET remains at the plateau voltage $V_{(pl)}$. The losses can be calculated as:

$$P_{SW(on)} = V_{IN} \times I/2 \times (t3 + t1) \times 1/T \quad (47)$$

with the switching frequency of converter: $f_{SW} = 1/T$

Turn-off behavior of a MOSFET is similar to the turn-on process. Total switching losses can be summarized as:

$$P_{SW} = V_{IN} \times 1/T \times (I_{min}/2 \times t_{on} + I_{max}/2 \times t_{off}) \quad (48)$$

Switching time depends on the current drive capabilities of the driver device and the gate resistance of the FET. If we assume an identical drive current for turn-on and turn-off event, switching time equals: $t_{SW} = Q_G / I_{drive}$

For the LTC3851 t_{SW} can be estimated roughly as follows. R_{drive} is about 2 Ω for the controller. The relevant voltage is driver voltage INTVCC – $V_{(th)}$, so we get:

$$t_{SW} = Q_G \times R_{drive} / (V_{drive} - V_{GS(th)}) \quad (49)$$

4. NXP Semiconductors high-performance small-signal MOSFETs in small packages

4.1 Low R_{DSon} N-channel small-signal MOSFETs

NXP Semiconductors offers several small-signal MOSFETs which are suitable for a medium power DC-to-DC conversion. PMN15UN reaches R_{DSon} of 15 mΩ for a gate-source voltage of 4.5 V. This is a very small resistance for a SOT457 device which outperforms comparable MOSFETs on the market. Due to the copper leadframe, a very good thermal performance can be achieved for this relatively small package.

Table 1. Comparison of low R_{DSon} small-signal MOSFETs in different packages

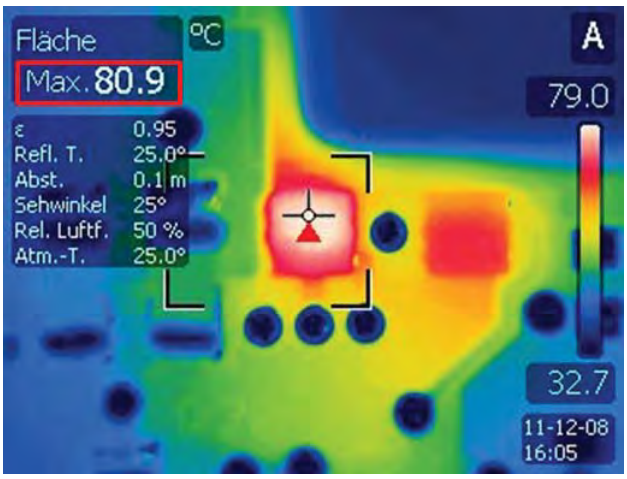
	PMT29EN	PMN15UN	PMPB20EN
Package	SOT223	SOT457	DFN2020MD-6 (SOT1220)
I_D(max)	6 A	6.3 A	5.8 A
V_{DS}	30 V	20 V	30 V
V_{GS}	20 V	8 V	20 V
$R_{DSon(typ)}$ (V_{GS} = 4.5 V)	29 mΩ	15 mΩ	20 mΩ
Q_G	24 nC	7.8 nC	7.2 nC
t_f (fall time)	40 ns	6 ns	4.9 ns
P_{tot} (t_{sp} = 25 °C)	8.3 W	1.75 W	8.33 W

For both small board space requirements and good thermal performance, 2 mm x 2 mm DFN2020MD-6 (SOT1220) package is a very good choice. For medium power requirements, MOSFETs of this type can replace power packages like DFN3030 or SO8 (SOT96) packages.

Table 2. N-channel MOSFETs in DFN2020MD-6 (SOT1220)

Type	$V_{DS(max)}$	$V_{GS(max)}$	ESD	$R_{DSon(typ)}$ (V_{GS} = 4.5 V)
PMPB12UN	20 V	+/– 8 V	-	12 mΩ
PMPB12UN	20 V	+/– 8 V	-	20 mΩ
PMPB10XNE	20 V	+/– 12 V	2 kV	10 mΩ
PMPB15XN	20 V	+/– 12 V	-	15 mΩ
PMPB23XNE	20 V	+/– 12 V	2 kV	23 mΩ
PMPB16XN	30 V	+/– 12 V	-	16 mΩ
PMPB13XNE	30 V	+/– 12 V	2 kV	13 mΩ
PMPB29XNE	30 V	+/– 12 V	2 kV	29 mΩ
PMPB33XN	30 V	+/– 12 V	-	33 mΩ
PMPB11EN	30 V	+/– 20 V	-	12 mΩ
PMPB20EN	30 V	+/– 20 V	-	20 mΩ
PMPB40SNA	60 V	+/– 16 V	-	40 mΩ

Thermal photograph on Figure 20 shows reference DC-to-DC converter PCB running with an output current of 6 A . It performs a voltage down conversion from 10 V to 1.5 V. Due to the small duty cycle of 0.15, low side-switch has to dissipate a higher amount of energy than high side switch. The temperature of this device is about 80 °C. Considering the rule of thumb that junction temperature T_j is 5 to 10 °C warmer than the surface of the package, T_j is below 90 °C in this test.



V_{IN} = 10 V
V_{OUT} = 1.5 V
I_{OUT} = 6 A
f_{SW} = 490 kHz

Fig 20. Thermal photograph of the DC-to-DC converter PCB with PMPB20EN

4.2 Measurements at the reference PCB with PMPB20EN switching stage

Figure 21 shows a scope curve of the falling edge measured for the SW signal, the output of the FET switching stage. The load current was adjusted to 3.5 A. The output voltage is 3.3 V. Figure 22 depicts measurement result of the rising edge.

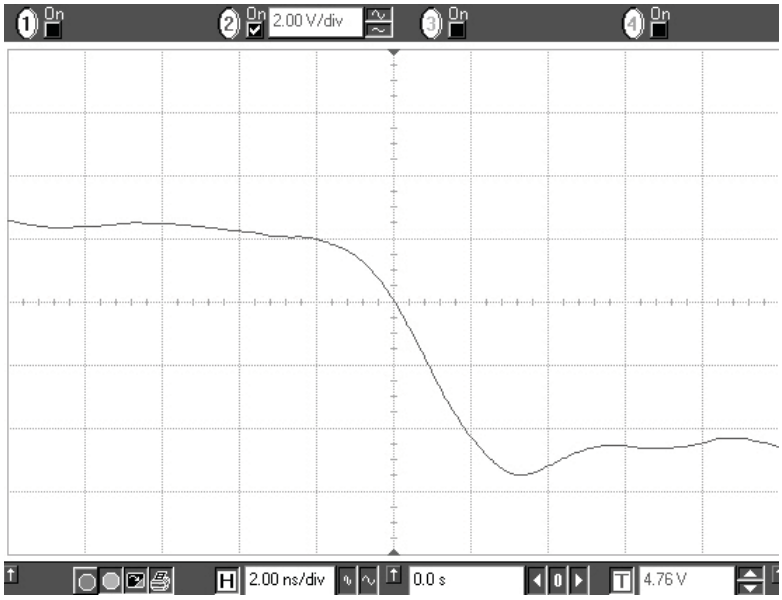


Fig 21. Falling edge measured at the output of the FET switching stage (Figure 16 SW node)

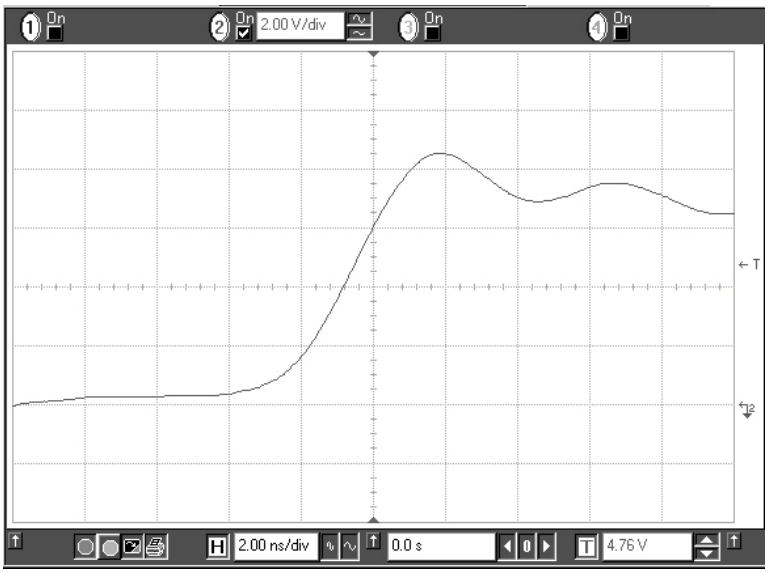


Fig 22. Rising edge measured at the output of FET switching stage (Figure 16 SW node)

Table 3. Stability of the output voltage versus load current, FET stage 2 × PMPB20EN in DFN2020MD-6 (SOT1220) package measured at power and sense contacts

Output load current	Output Voltage
0 A	3.296 V
0.1 A	3.296 V
0.5 A	3.295 V
1.0 A	3.295 V
2.0 A	3.294 V
3.0 A	3.294 V
4.0 A	3.293 V
6.0 A	3.292 V

5. Summary

Highly efficient medium power DC-to-DC converters can be designed with NXP Semiconductors small-signal MOSFETs. This can be a simple converter with a P-channel FET as high-side switch combined with a Schottky diode. For a Schottky diode NXP Semiconductors offers a wide selection of components with low forward voltages in compact flat power packages. For even better efficiency, synchronous DC-to-DC converters are recommended. Also for this topology NXP Semiconductors can offer suitable small-signal MOSFETs in various packages.

This document describes the way of working of different DC-to-DC conversion topologies. A reference design for synchronous DC-to-DC converter was presented with most important design aspects, such as power dissipation in the switching stage.

6. Appendix

Figure 22 and 23 show the component placement plans of the DC-to-DC converter reference board. The first figure shows component names whereas the second one indicates component values. This PCB is a 4 layer board with top layer containing solid copper areas which are connected to V_{IN}, V_{OUT} and ground. Layer 2 and the bottom layer are solid ground layers. Layer 3 contains signal connections.

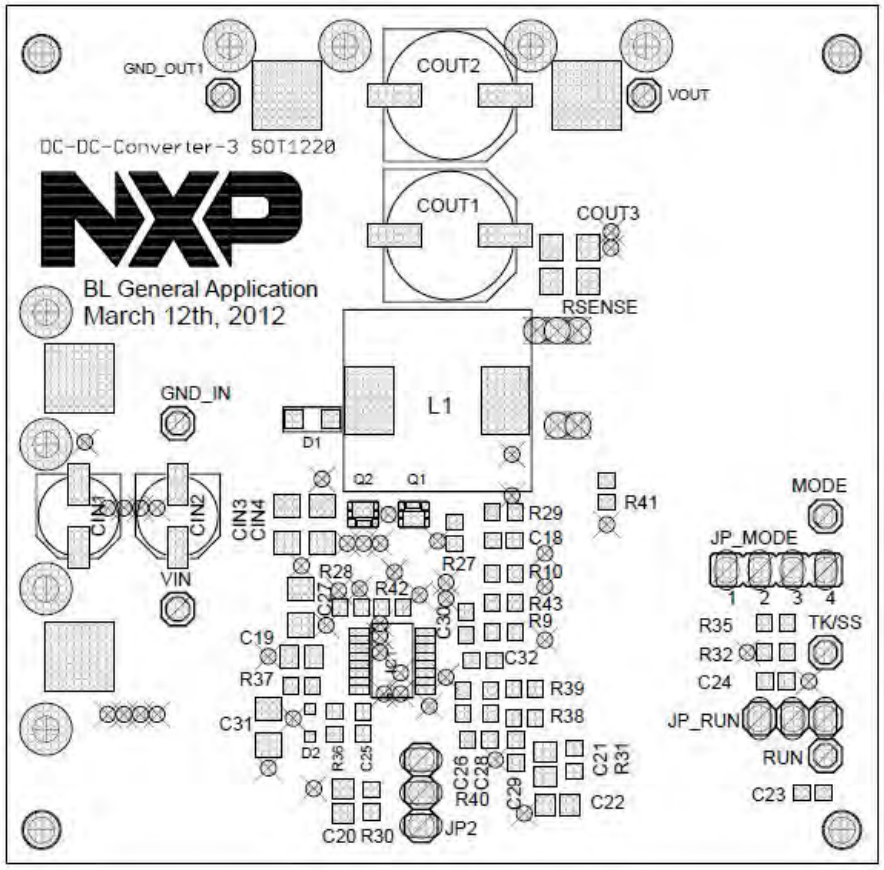


Fig 23. Component placement plan of the DC-to-DC converter reference board with component names

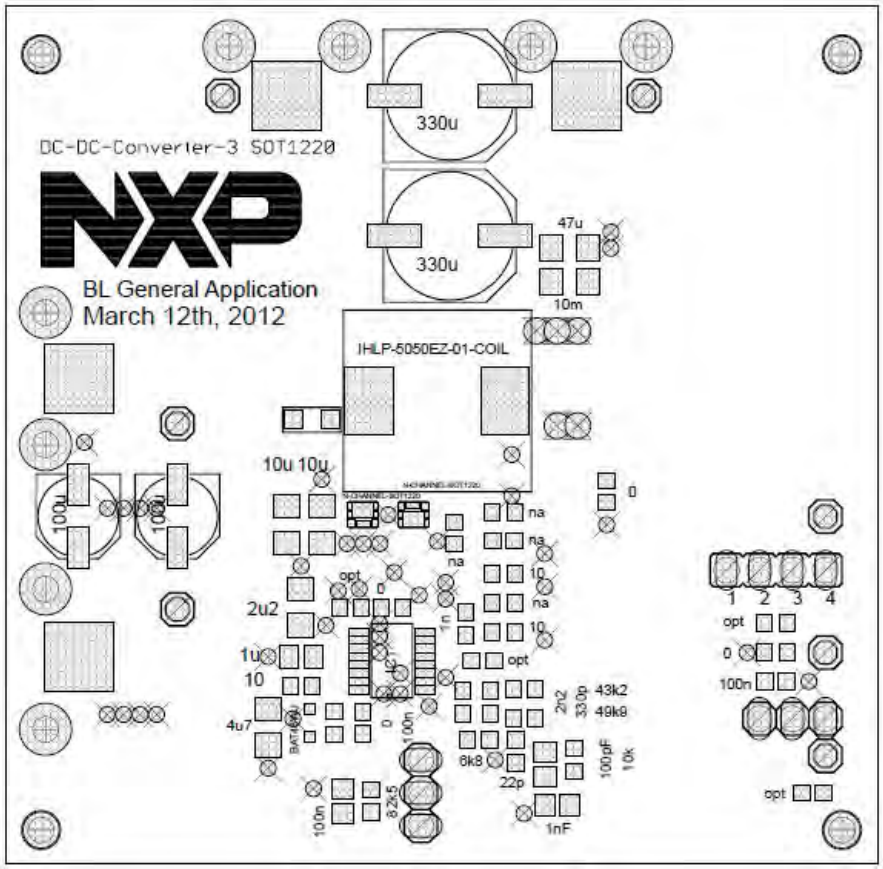


Fig 24. Component placement plan of the DC-to-DC converter reference board with component values

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