

# CBT3306

## Dual bus switch

Rev. 7 — 1 May 2012

Product data sheet

## 1. General description

The CBT3306 dual FET bus switch features independent line switches. Each switch is disabled when the associated output enable ( $\overline{\text{nOE}}$ ) input is HIGH.

The CBT3306 is characterized for operation from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

## 2. Features and benefits

- $5\ \Omega$  switch connection between two ports
- TTL-compatible input levels
- Multiple package options
- Latch-up protection exceeds 100 mA per JESD78B
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ CDM JESD22-C101D exceeds 1000 V

## 3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
CBT3306D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
CBT3306PW	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
CBT3306GT	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $1 \times 1.95 \times 0.5$ mm	SOT833-1
CBT3306GM	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body $1.6 \times 1.6 \times 0.5$ mm	SOT902-2

## 4. Marking

Table 2. Marking codes

Type number	Marking code
CBT3306D	CBT3306
CBT3306PW	3306
CBT3306GT	F06
CBT3306GM	F06

## 5. Functional diagram

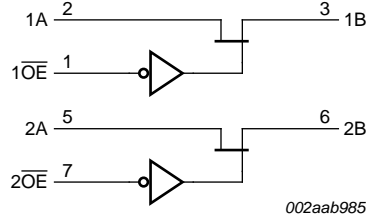


Fig 1. Logic diagram

## 6. Pinning information

### 6.1 Pinning

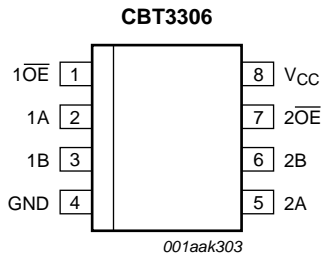


Fig 2. Pin configuration for SO8 (SOT96-1)

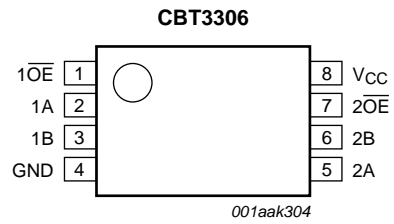


Fig 3. Pin configuration for TSSOP8 (SOT530-1)

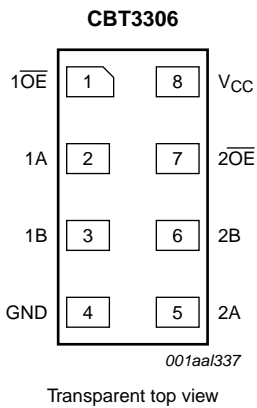


Fig 4. Pin configuration SOT833-1 (XSON8)

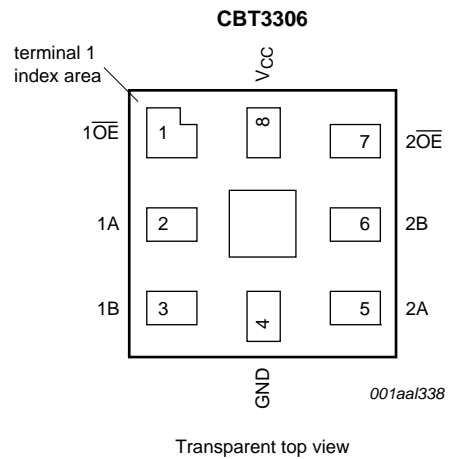


Fig 5. Pin configuration SOT902-2 (XQFN8)

## 6.2 Pin description

**Table 3.** Pin description

Symbol	Pin	Description
$1\overline{OE}, 2\overline{OE}$	1, 7	output enable input
1A, 2A	2, 5	data input/output (A port)
1B, 2B	3, 6	data input/output (B port)
GND	4	ground (0 V)
$V_{CC}$	8	positive supply voltage

## 7. Functional description

**Table 4.** Function selection<sup>[1]</sup>

Input	Input/output
$\overline{nOE}$	nA, nB
L	nA = nB
H	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

## 8. Limiting values

**Table 5.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1]</sup>

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		<sup>[2]</sup> -0.5	+7.0	V
$I_O$	output current		-	128	mA
$I_{IK}$	input clamping current	$V_{IO} = 0\text{ V}$	-50	-	mA
$T_{stg}$	storage temperature		-65	+150	$^{\circ}\text{C}$

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 9](#), is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## 9. Recommended operating conditions

**Table 6.** Operating conditions

All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$T_{amb}$	ambient temperature	operating in free air	-40	-	+85	$^{\circ}\text{C}$

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit	
			Min	Typ <sup>[1]</sup>	Max		
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_I = -18 \text{ mA}$	-	-	-1.2	V	
$I_I$	input leakage current	$V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } 5.5 \text{ V}$	-	-	$\pm 1$	$\mu\text{A}$	
$I_{CC}$	supply current	$V_{CC} = 5.5 \text{ V}; I_O = 0 \text{ mA};$ $V_I = V_{CC} \text{ or } \text{GND}$	-	-	3	$\mu\text{A}$	
$V_{pass}$	pass voltage	output HIGH; $V_I = V_{CC} = 5.0 \text{ V};$ $I_O = -100 \mu\text{A}$	3.6	3.9	4.2	V	
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 5.5 \text{ V};$ one input at 3.4 V, other inputs at $V_{CC}$ or GND	<sup>[2]</sup>	-	2.5	mA	
$C_I$	input capacitance	control pin; $V_I = 3 \text{ V or } 0 \text{ V}$	-	3.15	-	pF	
$C_{io(off)}$	off-state input/output capacitance	port off; $V_I = 3 \text{ V or } 0 \text{ V}; n\overline{OE} = V_{CC}$	-	6.45	-	pF	
$R_{ON}$	ON resistance	$V_{CC} = 4.5 \text{ V}; V_I = 0 \text{ V}; I_I = 64 \text{ mA}$	<sup>[3]</sup>	-	3.4	5	$\Omega$
		$V_{CC} = 4.5 \text{ V}; V_I = 0 \text{ V}; I_I = 30 \text{ mA}$	<sup>[3]</sup>	-	3.4	5	$\Omega$
		$V_{CC} = 4.5 \text{ V}; V_I = 2.4 \text{ V}; I_I = 15 \text{ mA}$	<sup>[3]</sup>	-	6.8	15	$\Omega$

[1] All typical values are at  $V_{CC} = 5 \text{ V}, T_{amb} = 25 \text{ }^\circ\text{C}$ .

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

[3] Measured by the voltage drop between the nA and the nB terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nA, nB) terminals.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

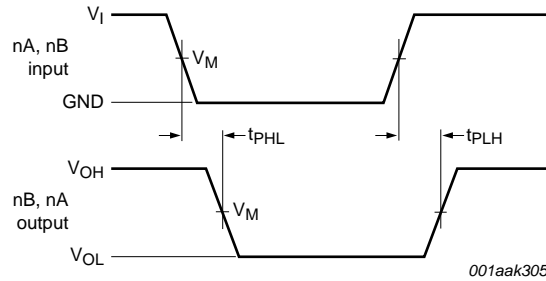
Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ	Max	
$t_{pd}$	propagation delay	nA, nB to nB, nA; see <a href="#">Figure 6</a> $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	<sup>[1][2]</sup>	-	0.25	ns
$t_{en}$	enable time	$n\overline{OE}$ to nA, nB; see <a href="#">Figure 7</a> $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	<sup>[2]</sup>	1.0	5.0	ns
$t_{dis}$	disable time	$n\overline{OE}$ to nA, nB; see <a href="#">Figure 7</a> $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	<sup>[2]</sup>	1.0	5.0	ns

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

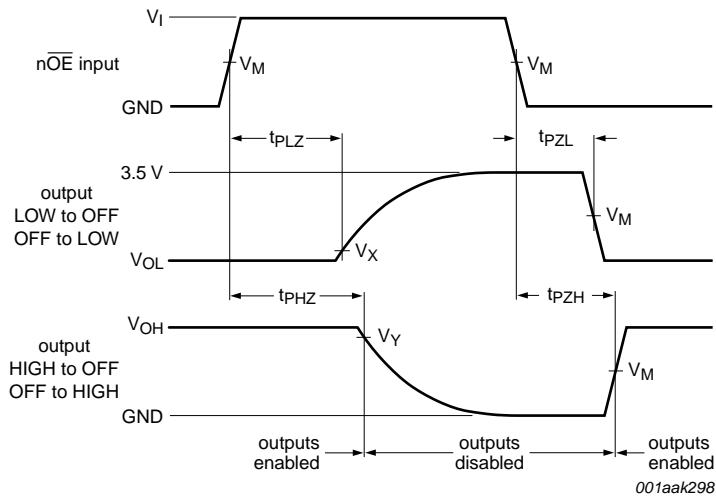
[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

12. Waveforms



Measurement points are given in [Table 9](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. The data input (nA, nB) to output (nB, nA) propagation delay times**



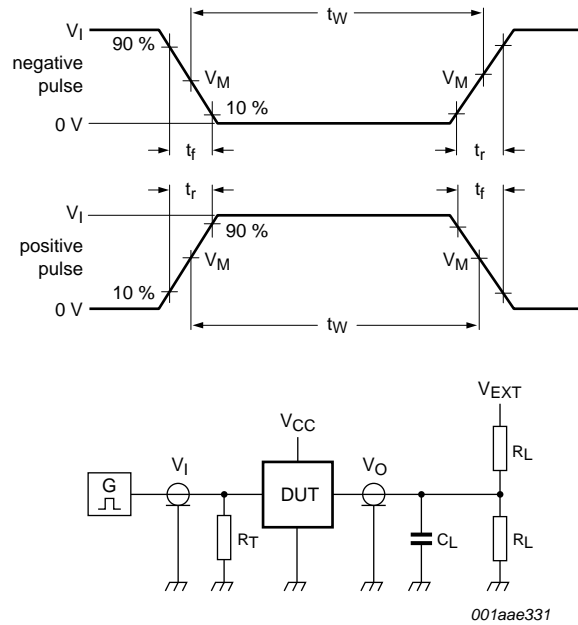
Measurement points are given in [Table 9](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. Enable and disable times**

**Table 9. Measurement points**

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

13. Test information



Test data is given in [Table 10](#).

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z<sub>o</sub> = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
V <sub>CC</sub> = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

14. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

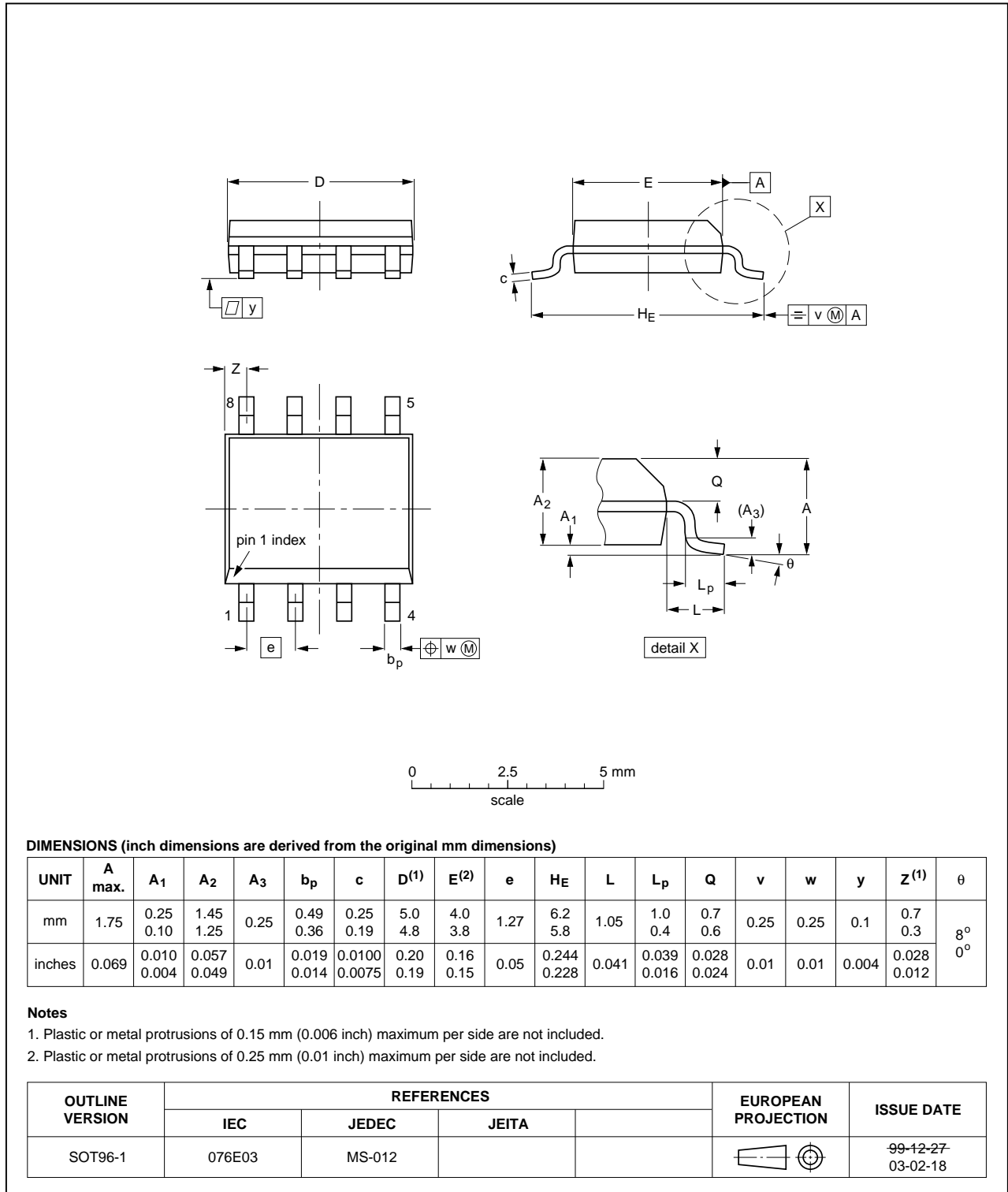


Fig 9. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm

SOT530-1

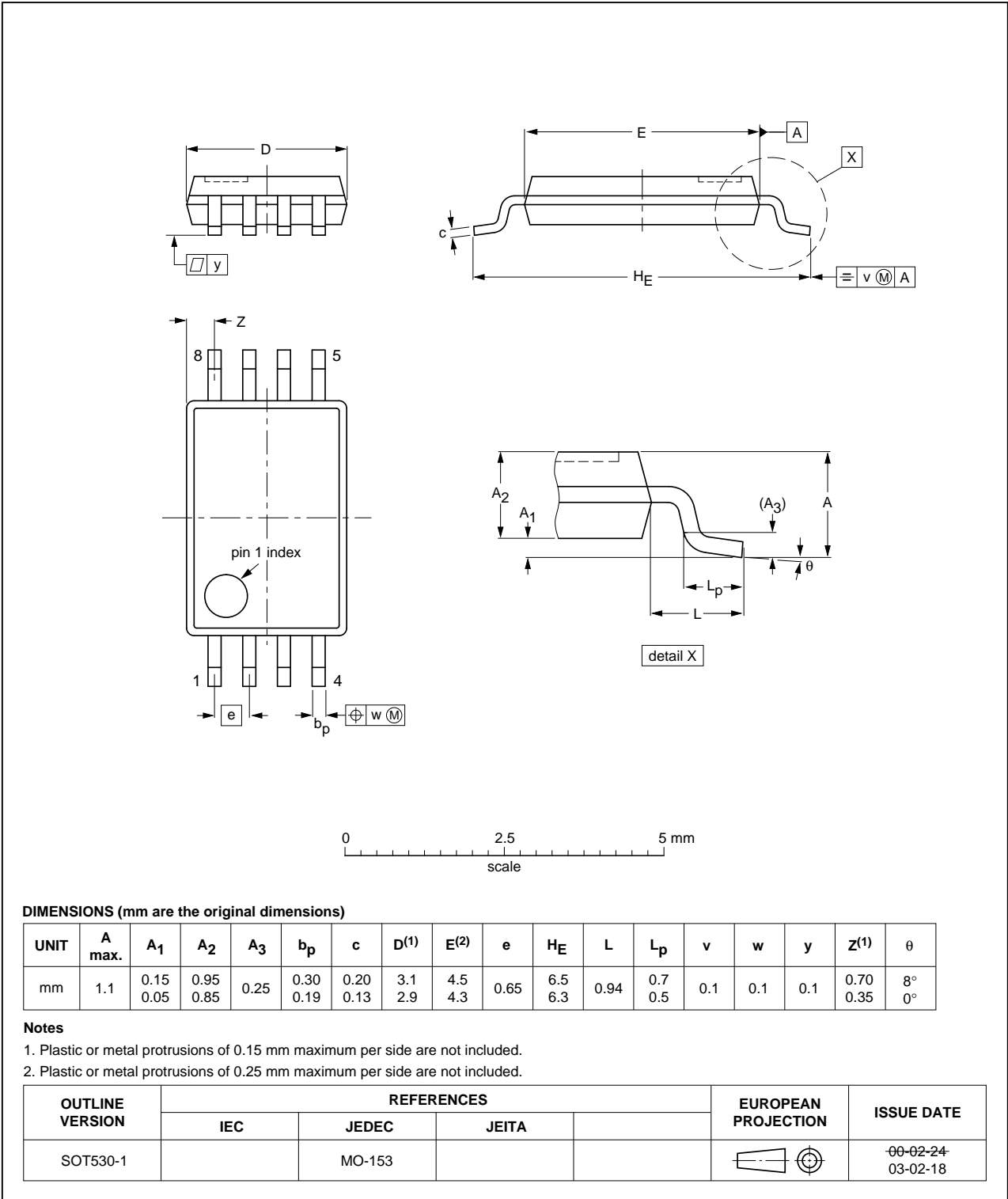


Fig 10. Package outline SOT530-1 (TSSOP8)



XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

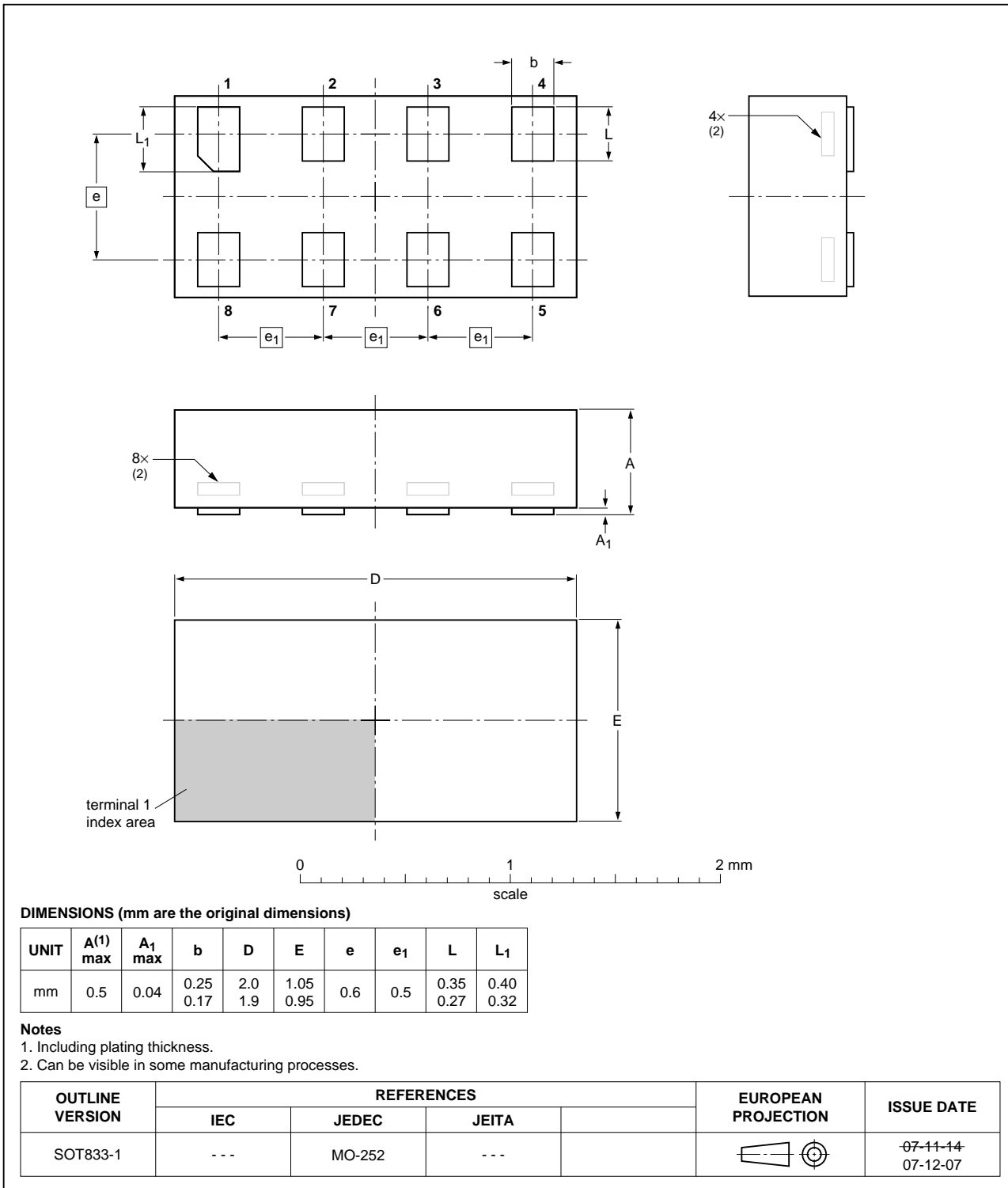


Fig 11. Package outline SOT833-1 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads;  
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2

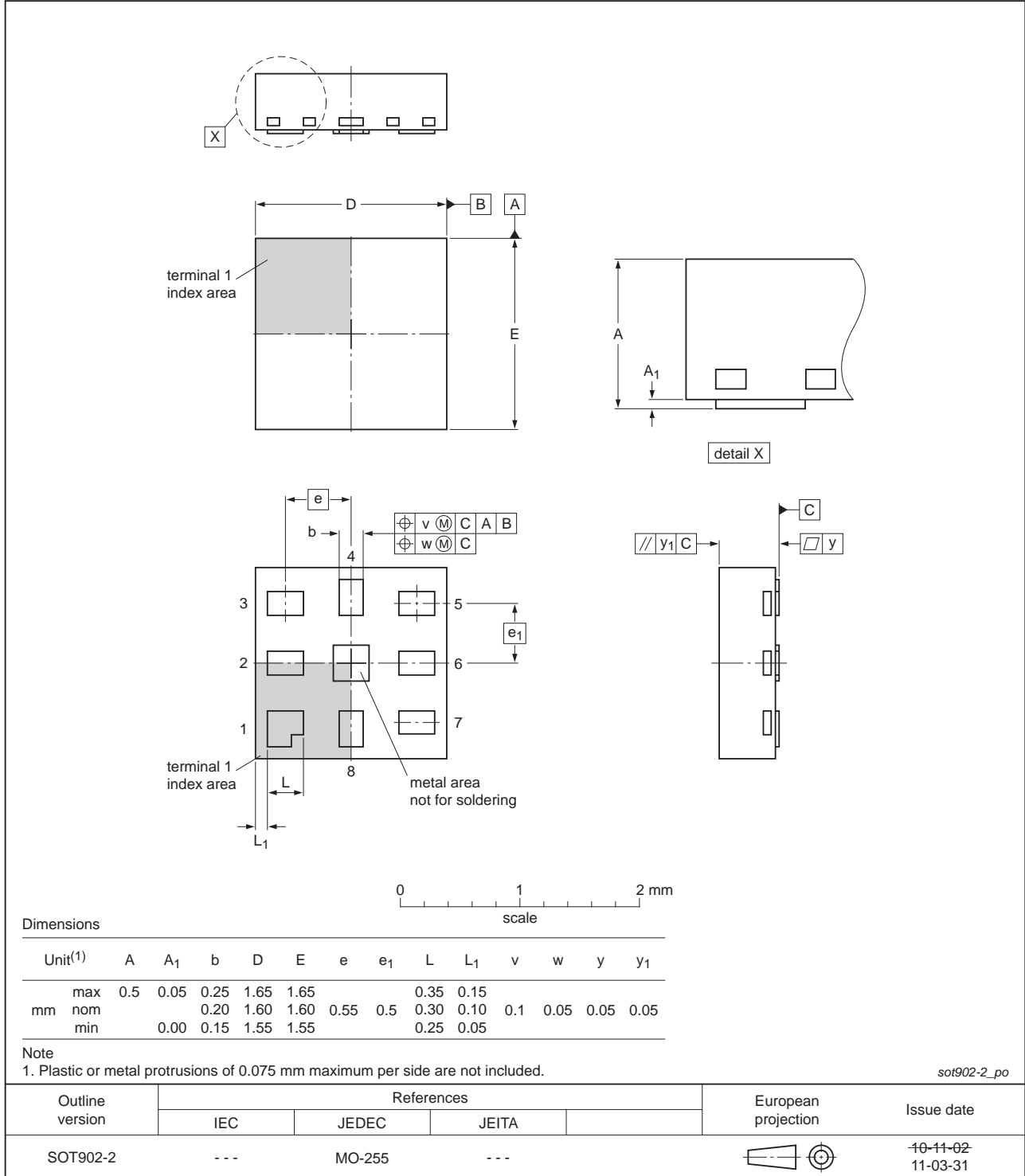


Fig 12. Package outline SOT902-2 (XQFN8)

## 15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

## 16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3306 v.7	20120501	Product data sheet	-	CBT3306 v.6
Modifications:	<ul style="list-style-type: none"> <li>For type number CBT3306GM the sot code has changed to SOT902-2.</li> </ul>			
CBT3306 v.6	20111122	Product data sheet	-	CBT3306 v.5
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
CBT3306 v.5	20100325	Product data sheet	-	CBT3306 v.4
CBT3306 v.4	20100218	Product data sheet	-	CBT3306 v.3
CBT3306 v.3	20091014	Product data sheet	-	CBT3306 v.2
CBT3306 v.2	20051117	Product data sheet	-	CBT3306 v.1
CBT3306 v.1	20011108	Product data	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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