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### 1. General description

The CBT3245A provides eight bits of high-speed TTL-compatible bus switching. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3245A is organized as one 8-bit bus switches with one output enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW, the switch is on and port A is connected to the B port. When  $\overline{OE}$  is HIGH, each switch is disabled. The CBT3245A is characterized for operation from -40 °C to +85 °C.

### 2. Features and benefits

- 5 Ω switch connection between two ports
- TTL-compatible control input levels
- Multiple package options
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115B exceeds 150 V
  - CDM JESD22-C101C exceeds 1000 V

### 3. Ordering information

#### Table 1. Ordering information

Type number	Package	Package							
	Temperature range	Name	Description	Version					
CBT3245AD	–40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1					
CBT3245ADB	–40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1					
CBT3245ADS	–40 °C to +85 °C	SSOP20[1]	plastic shrink small outline package; 20 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT724-1					
CBT3245APW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1					
CBT3245ABQ	–40 °C to +85 °C	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85$ mm	SOT764-1					

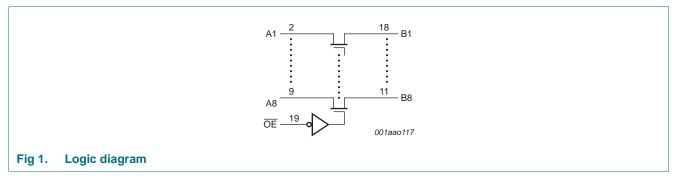
[1] Also known as QSOP20 package



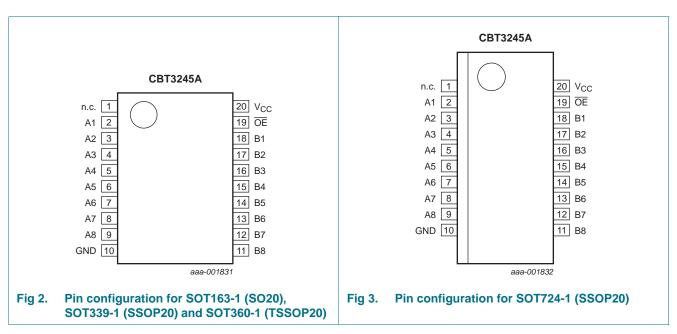
Octal bus switch

**CBT3245A** 

### 4. Functional diagram

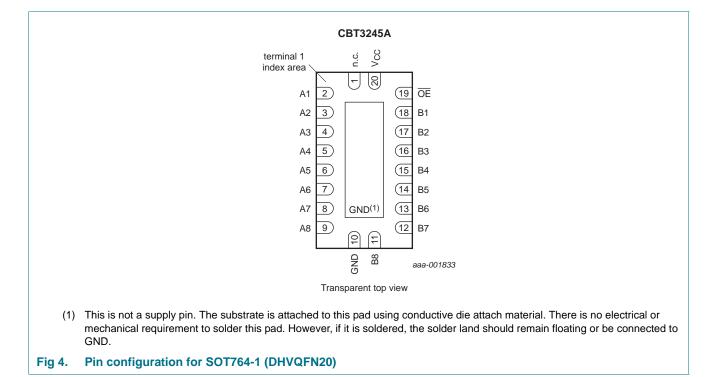


### 5. Pinning information



### 5.1 Pinning

#### **Octal bus switch**



### 5.2 Pin description

Table 2.	Pin description	
Symbol	Pin	Description
n.c.	1	not connected
A1 to A8	2, 3, 4, 5, 6, 7, 8, 9	data input/output (A port)
GND	10	ground (0 V)
B1 to B8	18, 17, 16, 15, 14, 13, 12, 1 <sup>4</sup>	1 data input/output (B port)
OE	19	output enable input (active LOW)
V <sub>CC</sub>	20	positive supply voltage

#### **Functional description** 6.

. ..

Table 3.	Function selection <sup>[1]</sup>	
Input OE		Input/output
OE		An, Bn
L		An = Bn
Н		Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

### 7. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1]</sup>  $T_{amb} = -40 \degree C$  to +85  $\degree C$ , unless otherwise specified.

anno	, , , , , , , , , , , , , , , , , , ,				
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
VI	input voltage		[2] -0.5	+7.0	V
l <sub>oк</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
Vo	output voltage		[2] -0.5	+7.0	V
lo	output current	V <sub>O</sub> < 0 V	-	±128	mA
I <sub>IK</sub>	input clamping current	$V_I = 0 V$	-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C

 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under <u>Section 8</u>, is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### 8. Recommended operating conditions

#### Table 5.Operating conditions

All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

Parameter	Conditions	Min	Тур	Max	Unit
supply voltage		4.0	-	5.5	V
HIGH-level input voltage		2.0	-	-	V
LOW-level input voltage		-	-	0.8	V
ambient temperature	operating in free air	-40	-	+85	°C
	supply voltage HIGH-level input voltage LOW-level input voltage	supply voltage HIGH-level input voltage LOW-level input voltage	supply voltage4.0HIGH-level input voltage2.0LOW-level input voltage-	supply voltage4.0-HIGH-level input voltage2.0-LOW-level input voltage	supply voltage4.05.5HIGH-level input voltage2.0-LOW-level input voltage-0.8

### 9. Static characteristics

#### Table 6.Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> =	Unit		
			Min	Typ <mark>[1]</mark>	Max	
V <sub>IK</sub>	input clamping voltage	$V_{CC} = 4.5 \text{ V}; \text{ I}_{I} = -18 \text{ mA}$	-	-	-1.2	V
l <sub>l</sub>	input leakage current	$V_{CC}$ = 5.5 V; $V_I$ = GND or 5.5 V	-	-	±5	μA
I <sub>CC</sub>	supply current	$V_{CC}$ = 5.5 V; I <sub>O</sub> = 0 mA; V <sub>I</sub> = V <sub>CC</sub> or GND	-	1	3	μA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 5.5$ V; one input at [2] 3.4 V, other inputs at $V_{CC}$ or GND	-	-	3.5	mA
CI	input capacitance	control pins; $V_I = 3 V \text{ or } 0 V$	-	3.2	-	pF
C <sub>io(off)</sub>	off-state input/output capacitance	port off; $V_1 = 3 V \text{ or } 0 V$ ; $\overline{OE} = V_{CC}$	-	6.6	-	pF

**Octal bus switch** 

Voltages are referenced to GND (ground = $0 V$ ).							
Symbol	Parameter	Conditions		T <sub>amb</sub> =	-40 °C to ⋅	+85 °C	Unit
				Min	Typ <mark>[1]</mark>	Мах	
R <sub>ON</sub>	ON resistance	$V_{CC} = 4.5 \text{ V}; \text{ V}_{I} = 0 \text{ V}; \text{ I}_{I} = 64 \text{ mA}$	[3]	-	5	7	Ω
		$V_{CC}$ = 4.5 V; $V_{I}$ = 0 V; $I_{I}$ = 30 mA	[3]	-	5	7	Ω
		$V_{CC}$ = 4.5 V; $V_{I}$ = 2.4 V; $I_{I}$ = –15 mA	[3]	-	10	15	Ω

 Table 6.
 Static characteristics ...continued

[1] All typical values are at V<sub>CC</sub> = 5 V,  $T_{amb}$  = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

[3] Measured by the voltage drop between the An and the Bn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (An or Bn) terminals.

### **10.** Dynamic characteristics

#### Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

Symbol	Parameter	Conditions	Conditions		T <sub>amb</sub> = -40 °C to +85 °C		
				Min	Max		
t <sub>pd</sub> propagation delay		An, Bn to Bn, An; see Figure 5	[1][2]				
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		-	0.25	ns	
t <sub>en</sub>	enable time	OE to An or Bn; see Figure 6	[2]				
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		1.0	5.9	ns	
t <sub>dis</sub>	disable time	OE to An or Bn; see Figure 6	[2]				
		$V_{CC}=5.0~V\pm0.5~V$		1.0	6.0	ns	

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

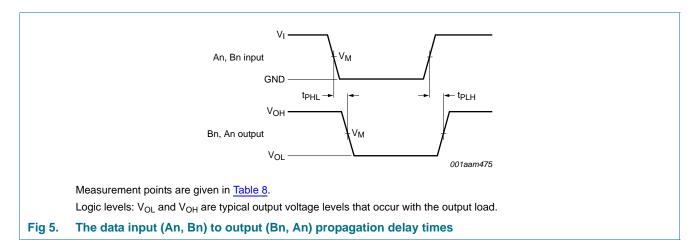
[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

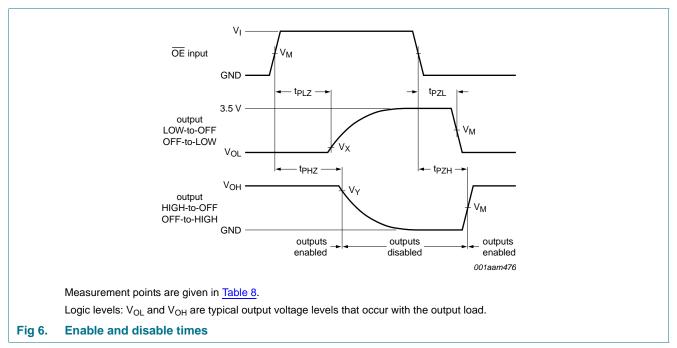
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

 $t_{\text{dis}}$  is the same as  $t_{\text{PLZ}}$  and  $t_{\text{PHZ}}.$ 

Octal bus switch

### 11. Waveforms



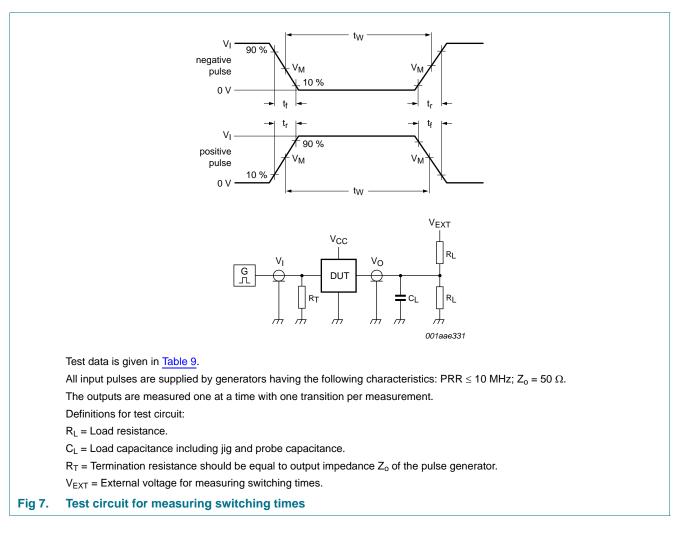


#### Table 8. Measurement points

Supply voltage	Input		Output		
V <sub>cc</sub>	VI	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
$V_{CC}$ = 5.0 V $\pm$ 0.5 V	GND to 3.0 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> – 0.3 V

CBT3245A Octal bus switch

### **12. Test information**

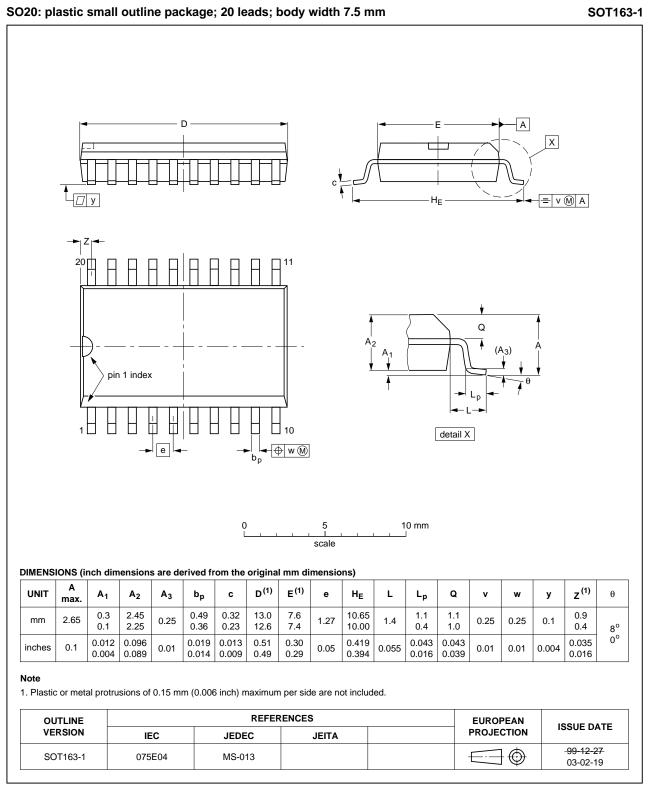


#### Table 9. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	RL	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
$V_{CC}$ = 5.0 V $\pm$ 0.5 V	GND to 3.0 V	$\leq$ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

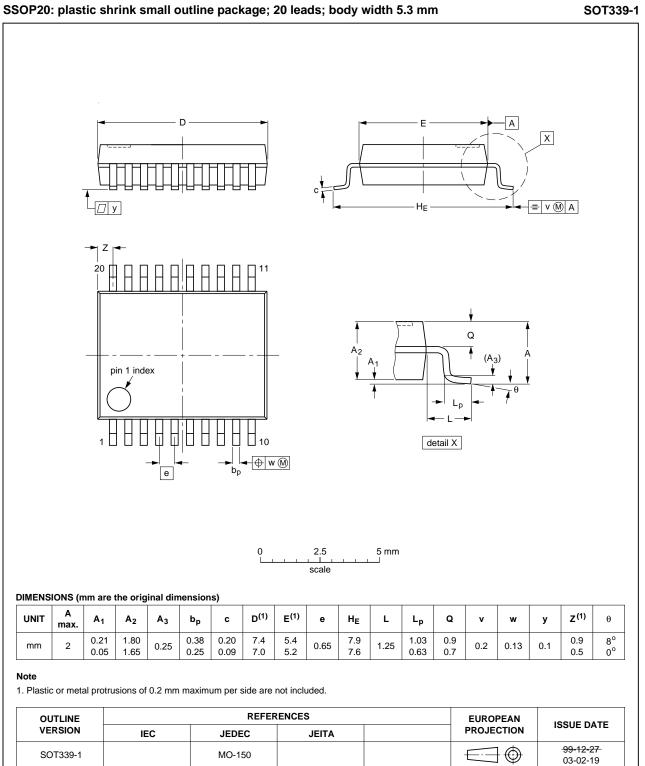
Octal bus switch

### 13. Package outline



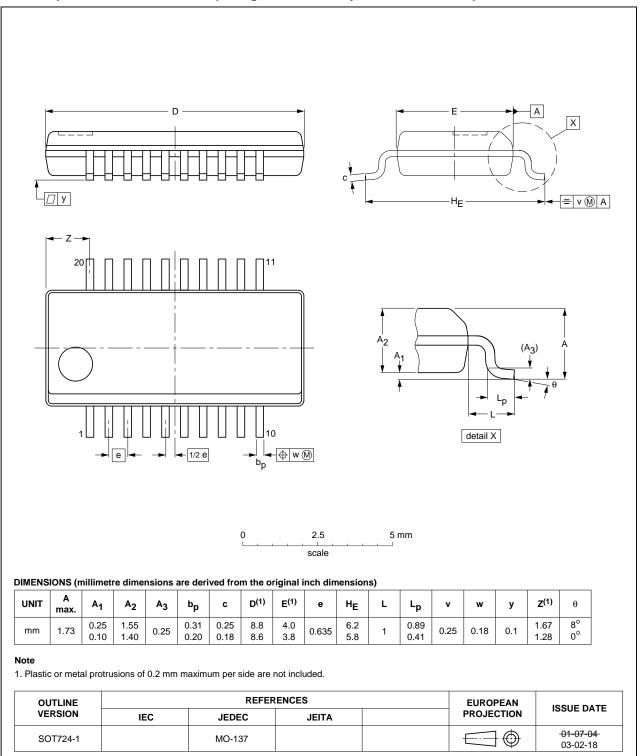
#### Fig 8. Package outline SOT163-1 (SO20)

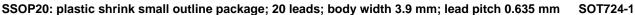
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#### Fig 9. Package outline SOT339-1 (SSOP20)

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#### Fig 10. Package outline SOT724-1 (SSOP20)

CBT3245A

**CBT3245A** 

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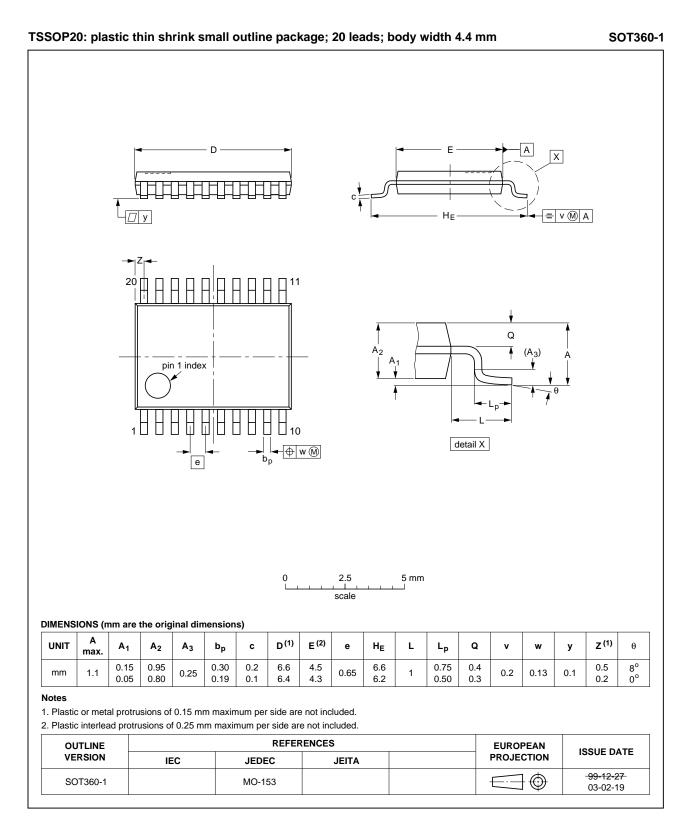
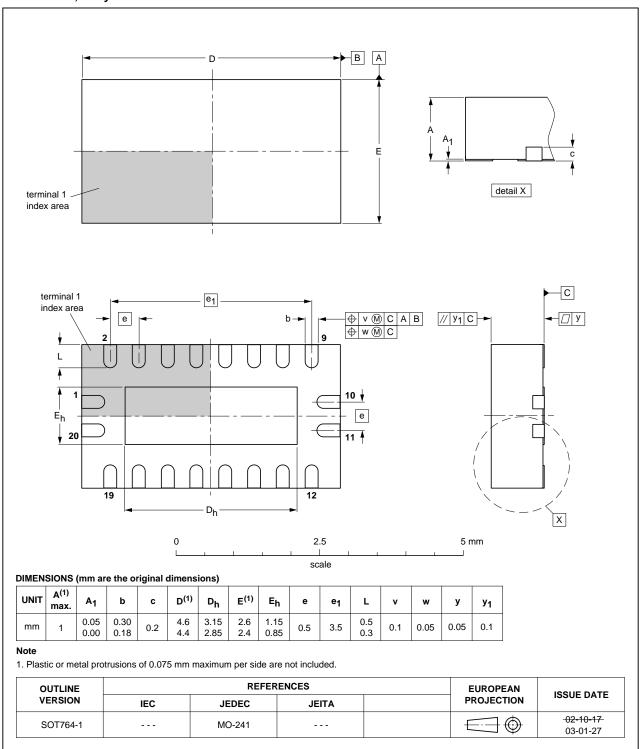


Fig 11. Package outline SOT360-1 (TSSOP20)

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#### DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm SOT764-1

#### Fig 12. Package outline SOT764-1 (DHVQFN20)

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### 14. Abbreviations

A	
Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
DUT	Device Under Test
HBM	Human Body Model
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

### **15. Revision history**

Table 11. Revisio	on history							
Document ID	Release date	Data sheet status	Change notice	Supersedes				
CBT3245A v.3	20120105	Product data sheet	-	CBT3245A v.2				
Modifications: • The format of this document has been redesigned to comply with the new identity guidelines o NXP Semiconductors.								
	<ul> <li>Legal texts I</li> </ul>	have been adapted to the ne	ew company name where	appropriate.				
	<ul> <li>Marking cod</li> </ul>	<ul> <li>Marking code removed from order information section.</li> </ul>						
	<ul> <li>Description</li> </ul>	of C <sub>I</sub> and C <sub>I/O</sub> corrected (err	ata).					
CBT3245A v.2	20020627	Product data sheet	-	CBT3245A v.1				
CBT3245A v.1	20020218	Product data sheet	-	-				

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#### 16.1 Data sheet status

Document status[1][2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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#### **Octal bus switch**

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