

DUAL OUTPUT LOW NOISE AMPLIFIER, 0.04 - 0.96 GHz

Typical Applications

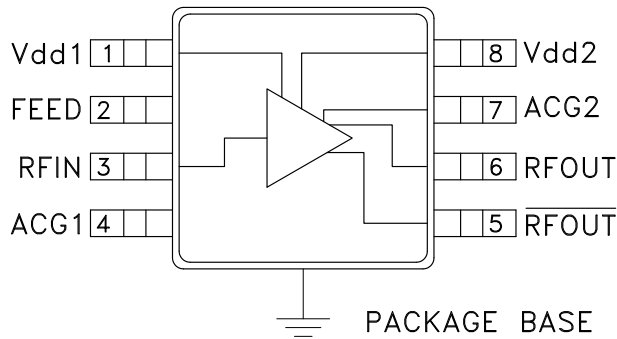
The HMC549MS8GE is ideal for:

- DTV Receivers
- Multi-Tuner Set Top Boxes
- PVRs & Home Gateways

Features

- Single-ended or Balanced Output
- High Output IP3: +27 dBm
- Low Noise Figure: 3.5 dB
- Single Positive Supply: +5V
- 75 Ohm Input

Functional Diagram



General Description

The HMC549MS8GE is a GaAs pHEMT MMIC Low Noise Amplifier that are ideal pre-amplifiers for CATV Set Top Box, Home Gateway, and Digital Television receiver operating between 40 and 960 MHz. This high dynamic range LNA has been optimized to provide 3.5 dB noise figure and +27 dBm output IP3 from a single supply of +5V @ 120 mA. The outputs of this LNA are extremely well balanced, and can be used to drive a differential input tuner with very high input IP2 requirements. This dual purpose LNA can also be used as an active splitter driving two single-ended input tuners. This LNA is housed in a RoHS compliant MSOP8G SMT package with exposed ground paddle.

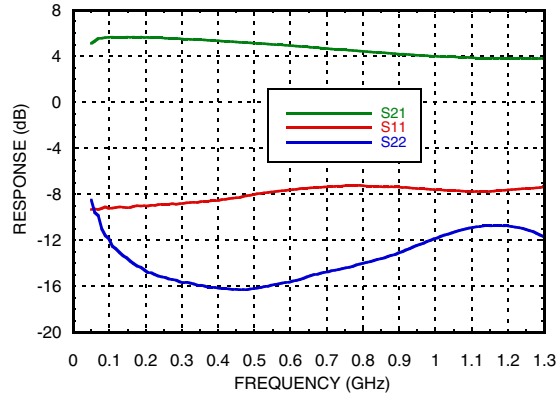
Electrical Specifications, 75 Ohm System, $T_A = +25^\circ\text{C}$, $V_{dd} = +5\text{V}$

Parameter*	Min.	Typ.	Max.	Units
Frequency Range	0.04 - 0.96			GHz
Gain	2	5		dB
Gain Variation over Temperature		0.01	0.02	dB/°C
Noise Figure		3.5	5.2	dB
Input Return Loss		8		dB
Output Return Loss		15		dB
Output Power for 1 dB Compression (P1dB)		12.5		dBm
Output Third Order Intercept (OIP3)		27		dBm
Output Second Order Intercept (OIP2)		52		dBm
Amplitude Balance		0.3		dB
Phase Balance		2		deg
Supply Current (I _{dd})		120		mA

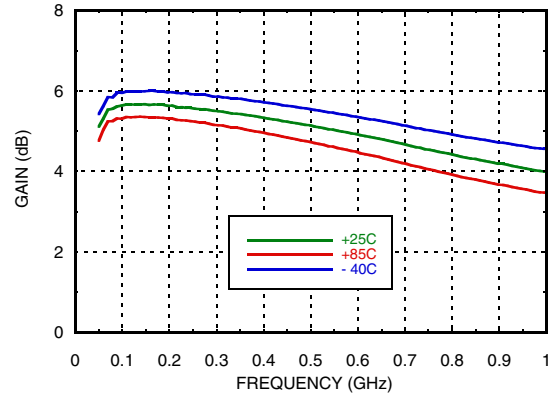
* Unless otherwise noted, all measurements performed with balun on the output.

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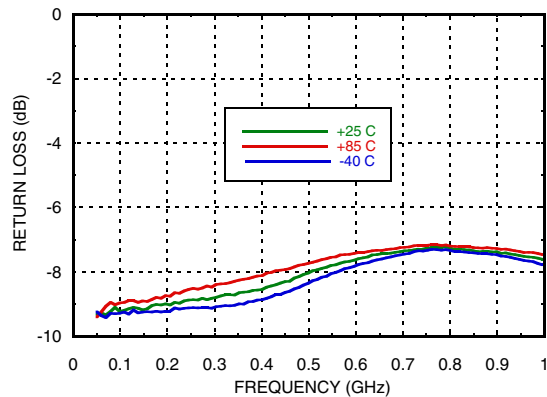
Broadband Gain & Return Loss



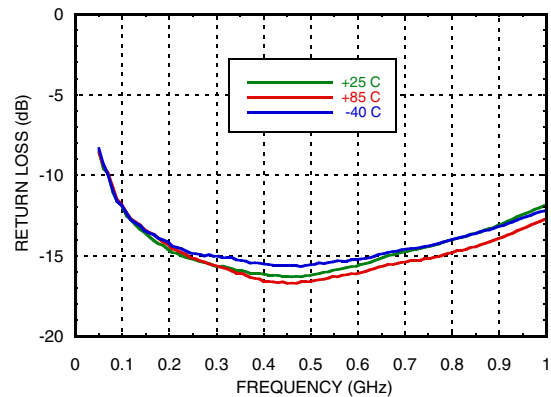
Gain vs. Temperature



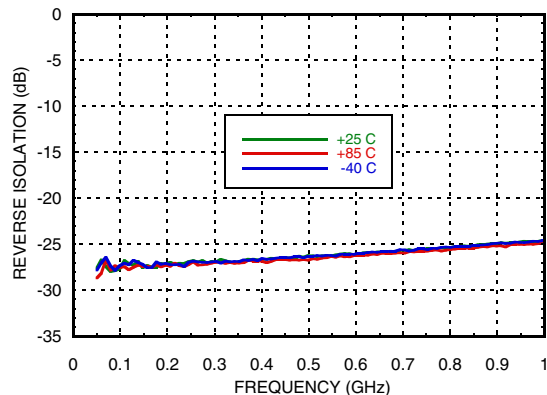
Input Return Loss vs. Temperature



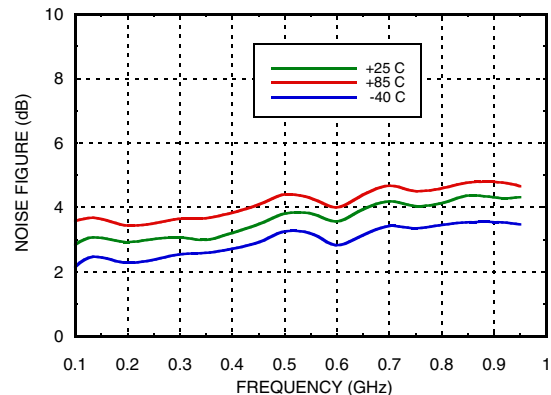
Output Return Loss vs. Temperature



Reverse Isolation vs. Temperature



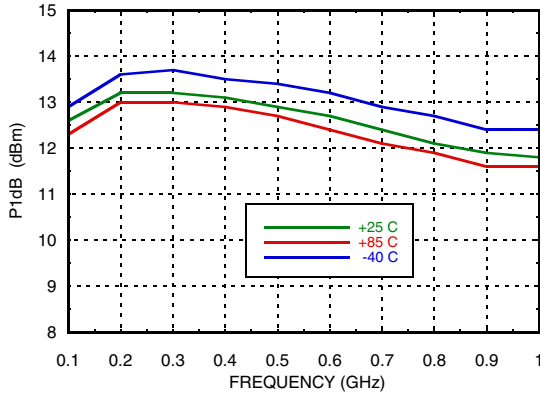
Noise Figure vs. Temperature



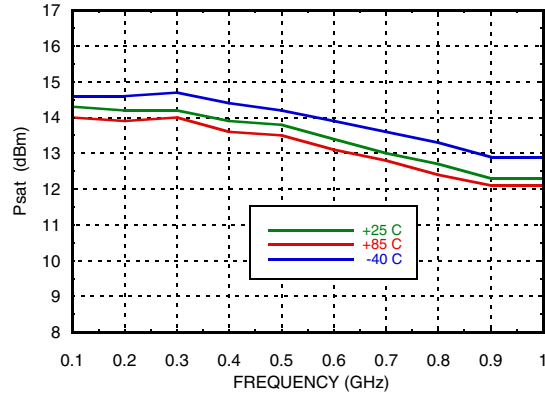
All measurements taken in 75 Ohm system.

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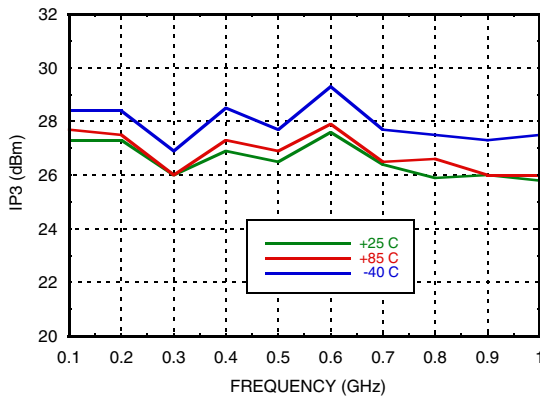
P1dB vs. Temperature



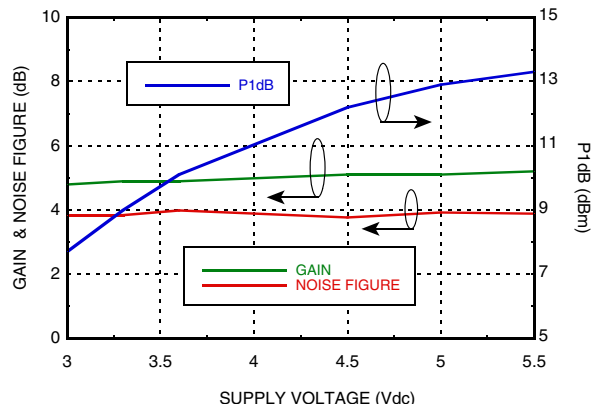
Psat vs. Temperature



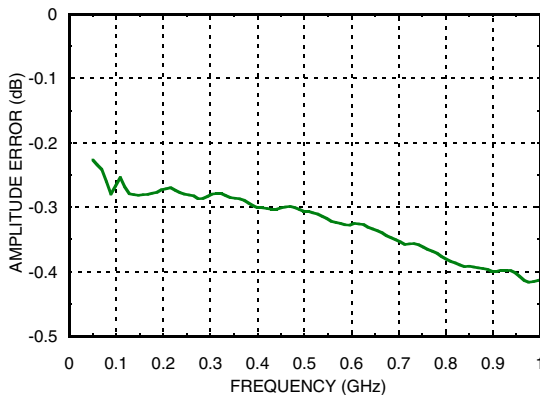
Output IP3 vs. Temperature



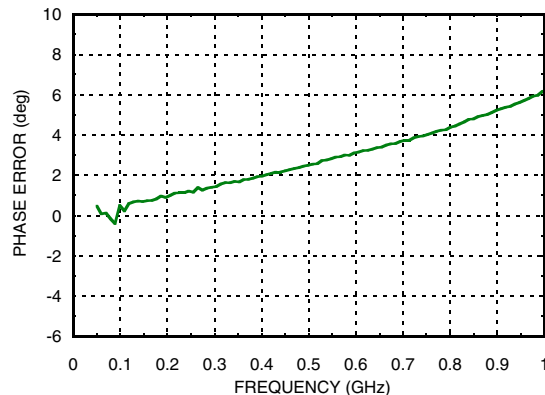
Gain, Noise Figure & P1dB vs. Supply Voltage @ 500 MHz



Amplitude Balance *



Phase Balance *



* Data taken without balun on the output.
All measurements taken in 75 Ohm system.

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Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+7V
RF Input Power (RFIN)	10 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 20 mW/°C above 85 °C)	1.32 W
Thermal Resistance (channel to ground paddle)	49 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

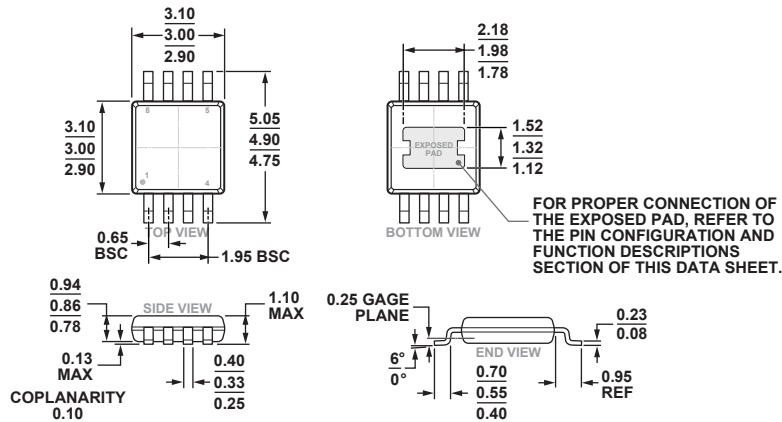
Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
3.0	117.1
3.3	117.5
3.6	117.9
4.5	118.5
5.0	119.0
5.5	119.3



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

Outline Drawing



COMPLIANT TO JEDEC STANDARDS MO-187-AA-T

8-Lead Small Outline Package with Exposed Pad [MINI_SO_EP]
(RH-8-3)
Dimensions shown in millimeters

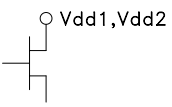
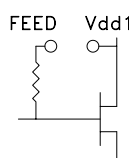
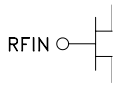
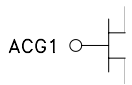
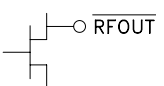
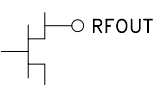
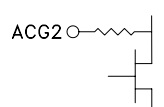
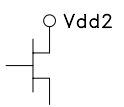
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[2]
HMC549MS8GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[1]	H549 XXXX

[1] Max peak reflow temperature of 260 °C

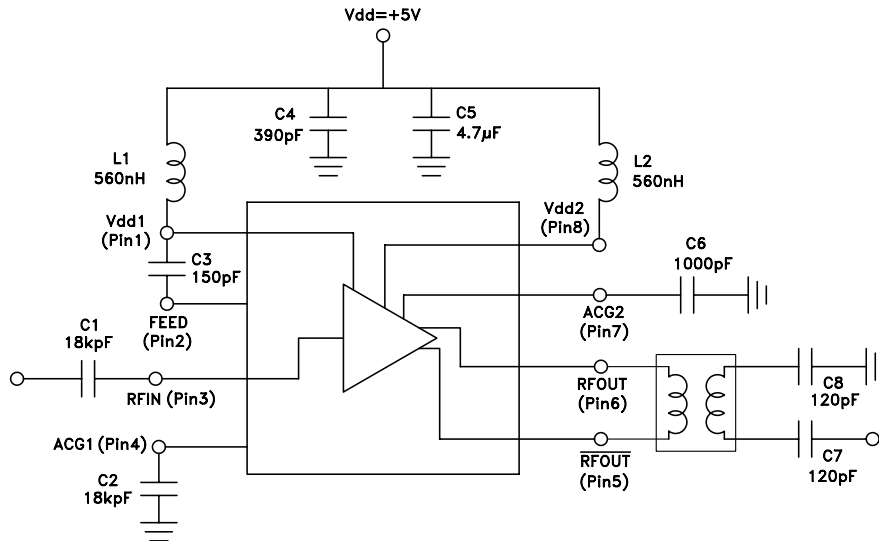
[2] 4-Digit lot number XXXX

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Pin Descriptions

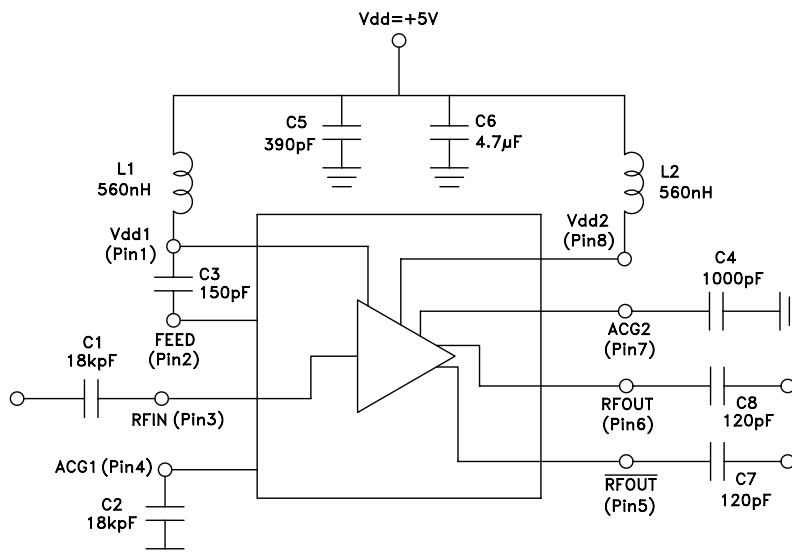
Pin Number	Function	Description	Interface Schematic
1, 8	Vdd1, Vdd2	Power supply voltage for the first stage. An external choke inductor is required. See application circuit.	
2	FEED	Feedback capacitor for the first stage.	
3	RFIN	This pin is DC coupled and requires a DC blocking cap. See application circuit.	
4	ACG1	This pin has to be terminated by an external capacitor. See application circuit.	
5	$\overline{\text{RFOUT}}$	RF differential output 2. This port is DC coupled.	
6	RFOUT	RF differential output 1. This port is DC coupled.	
7	ACG2	This pin has to be terminated by an external capacitor. See application circuit.	
8	Vdd2	Power supply voltage for second stage. An external choke inductor is required. See application circuit.	

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Application Circuit for 109236 - HMC549MS8GE (2-port)

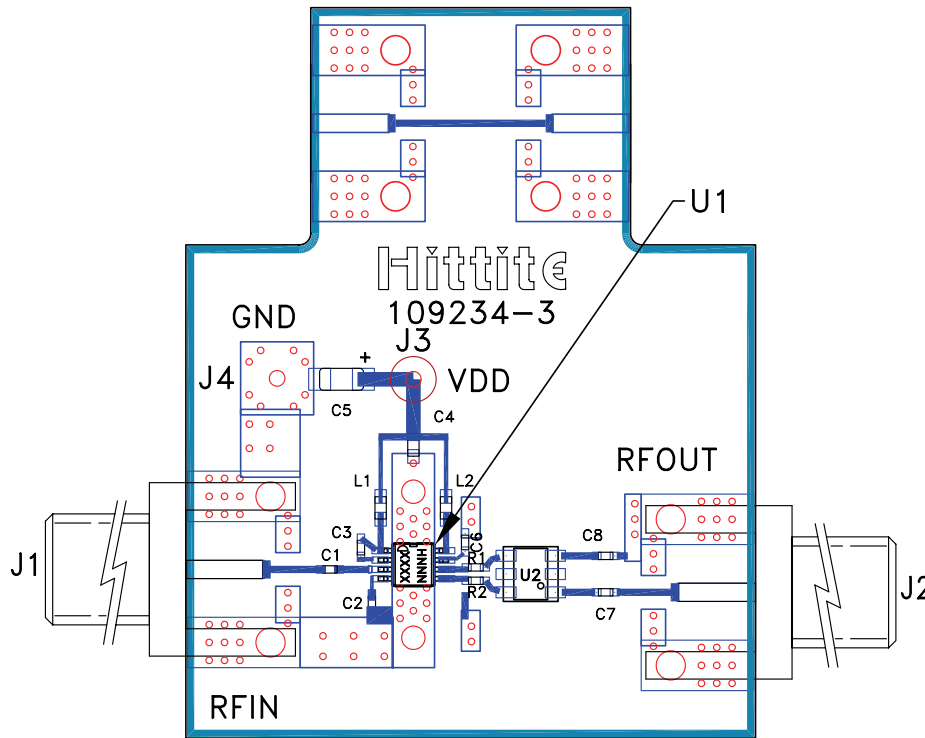


Application Circuit for 113184 - HMC549MS8GE (3-port)



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Evaluation PCB



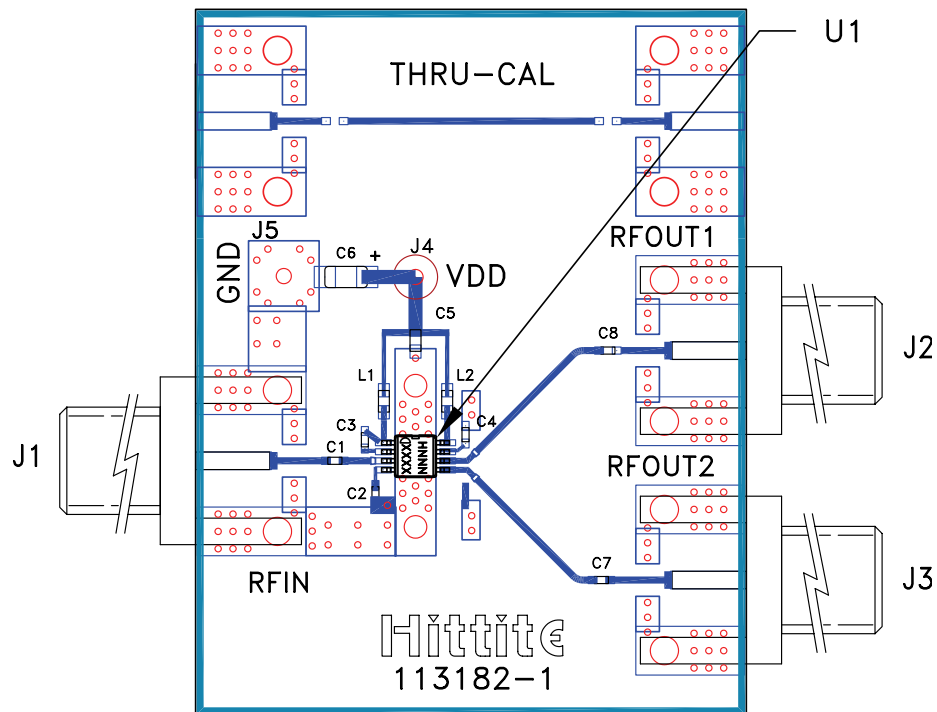
List of Materials for Evaluation PCB 109236 [1]

Item	Description
J1, J2	BOMAR F Type 75 Ohm Connectors
J3, J4	DC Pin
C1, C2	18 k μ F Capacitor, 0402 Pkg.
C3	150 pF Capacitor, 0402 Pkg.
C4	390 pF Capacitor, 0603 Pkg.
C5	4.7 μ F Capacitor, Tantalum
C6	1,000 pF Capacitor, 0402 Pkg.
C7, C8	120 pF Capacitor, 0402 Pkg.
L1, L2	560 nH Inductor, 0603 Pkg..
R1, R2	0 Ohm Resistor, 0603 Pkg.
U1	HMC549MS8GE Low Noise Amplifier
U2	ETC1-1-13 I:I Balun
PCB [2]	109234 Evaluation PCB

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 75 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices, upon request.

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: FR4

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Evaluation PCB

List of Materials for Evaluation PCB 113184 [1]

Item	Description
J1 - J3	BOMAR F Type 75 Ohm Connectors
J4, J5	DC Pin
C1, C2	18 kpF Capacitor, 0402 Pkg.
C3	150 pF Capacitor, 0402 Pkg.
C4	1,000 pF Capacitor, 0402 Pkg.
C5	390 pF Capacitor, 0603 Pkg.
C6	4.7 μ F Capacitor, Tantalum
C7, C8	120 pF Capacitor, 0402 Pkg.
L1, L2	560 nH Inductor, 0603 Pkg..
U1	HMC549MS8GE Low Noise Amplifier
PCB [2]	113182 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: FR4

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 75 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices, upon request.

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