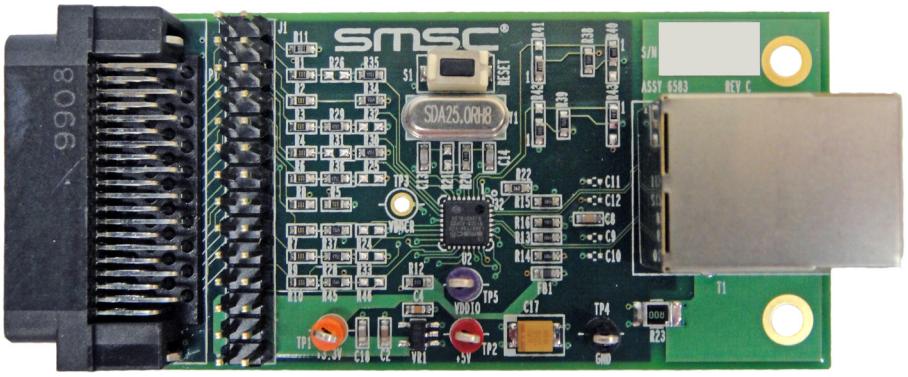
EVB8710 Evaluation Board User Manual



1 Introduction

The LAN8710A is a low-power, small form factor, highly integrated analog interface IC for high-performance embedded Ethernet applications. The LAN8710A requires only a single +3.3V supply and provides an integrated +1.2V supply to run the core digital logic.

The EVB8710 is a PHY Evaluation Board (EVB) that interfaces a Media Independent Interface (MII) MAC controller to the LAN8710A Ethernet MII PHY via a standard 40-pin MII connector. The LAN8710A is connected to an RJ45 Ethernet jack with integrated magnetics for 10/100 connectivity. A simplified block diagram of the EVB8710 can be seen in Figure 1.1.

Note: Revisions 1.1 and later of the EVB8710 Evaluation Board User Manual pertain to EVB8710 assembly number 6583. For information on the older, discontinued EVB8710 assembly number 7169AZ, refer to revision 1.0 of the EVB8710 Evaluation Board User Manual. For identification purposes, the EVB8710 assembly number is silkscreened onto the front of the evaluation board.

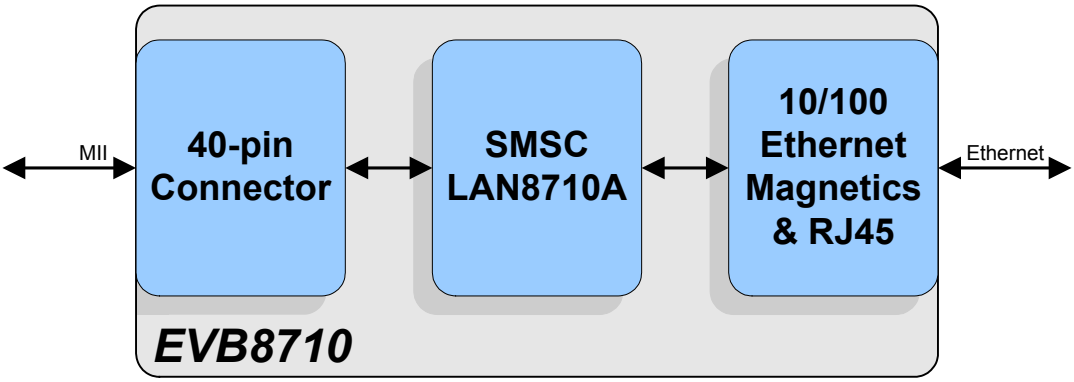


Figure 1.1 EVB8710 Block Diagram

Note: Though the LAN8710A supports an RMII mode of operation, the EVB8710 evaluation board does not support this mode.

1.1 References

Concepts and material available in the following documents may be helpful when reading this document.

Table 1.1 References

DOCUMENT	LOCATION
▪ SMSC LAN8710A Datasheet	http://www.smsc.com/lan8710a
▪ AN18-20 Migrating from the LAN8700 to the LAN8710A/LAN8720A ▪ AN8-13 Suggested Magnetics	http://www.smsc.com/lan8710a
▪ SMSC LAN8710A Evaluation Board Schematic	http://www.smsc.com/lan8710a

2 Board Details

This section includes the following EVB8710 board details:

- Power
- Configuration
- Mechanicals

2.1 Power

2.1.1 +5V Power

Power is normally supplied to the EVB8710's +3.3V regulator externally via the +5V power pins of the MII connector. If desired, the EVB8710 can be powered without +5V present on the MII connector by supplying +5V to the TP2 (red) test point with ground connected to pin 20 of the J1 header.

Note: Before connecting an external power supply to TP2, ensure power is not present on the MII connector's +5V pins. Connecting +5V simultaneously via the MII connector and TP2 may result in permanent damage to the board.

2.1.2 VDDIO Power

The LAN8710A's VDDIO power may be supplied at a voltage other than +3.3V by depopulating resistor R12 and supplying +1.6V to +3.6V externally via test point TP5 (purple), with ground connected to pin 20 of the J1 header.

Note: Before connecting an external power supply to TP5, ensure that resistor R12 has been removed. Connecting an external power supply to TP5 while resistor R12 is populated may result in permanent damage to the board.

2.1.3 +1.2V Power

The LAN8710A's internal +1.2V regulator can be optionally disabled. Refer to Section 2.2.4, "Internal +1.2V Regulator Configuration (REGOFF)," on page 6 for additional information.

2.2 Configuration

The following sub-sections describe the various board features and configuration settings. A top view of the EVB8710 is shown in Figure 2.1.

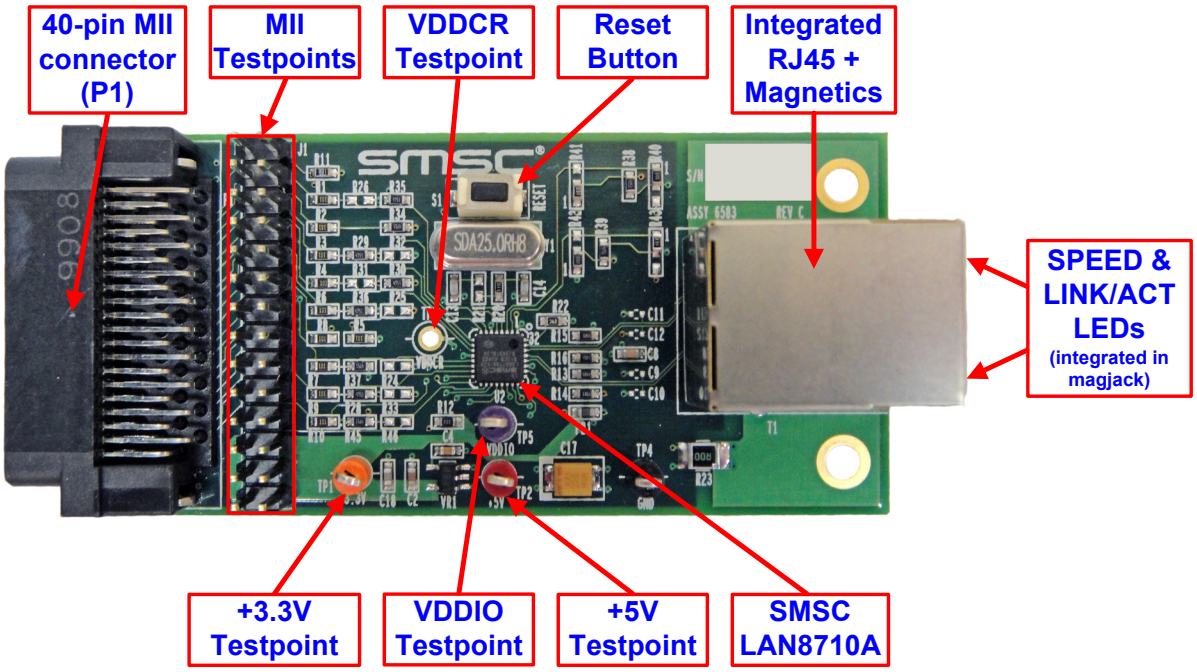


Figure 2.1 Top View of the EVB8710

2.2.1 PHY Address Configuration

The EVB8710 allows the user to configure the default PHY address at power-up via the PHYAD[2:0] configuration straps. Table 2.1 details the proper configuration required for each PHY address value. By default, all EVB8710 PHY address straps are configured to a value of “0”.

Table 2.1 PHYAD[2:0] Resistor Configuration

PHYAD[2:0]	PHYAD[2:0] PULL-UP/DOWN RESISTORS					
	PHYAD2		PHYAD1		PHYAD0	
	R26	R35	R25	R36	R24	R37
000 (Default)	*Depopulate*	Populate	*Depopulate*	Populate	*Depopulate*	Populate
001	*Depopulate*	Populate	*Depopulate*	Populate	Populate	*Depopulate*
010	*Depopulate*	Populate	Populate	*Depopulate*	*Depopulate*	Populate
011	*Depopulate*	Populate	Populate	*Depopulate*	Populate	*Depopulate*
100	Populate	*Depopulate*	*Depopulate*	Populate	*Depopulate*	Populate
101	Populate	*Depopulate*	*Depopulate*	Populate	Populate	*Depopulate*
110	Populate	*Depopulate*	Populate	*Depopulate*	*Depopulate*	Populate
111	Populate	*Depopulate*	Populate	*Depopulate*	Populate	*Depopulate*

2.2.2 Boot Mode Configuration

The EVB8710 can be configured to boot into a specific mode of operation at power-up via the MODE[2:0] configuration straps. Table 2.2 details the proper configuration required for each mode. By default, all EVB8710 MODE[2:0] straps are configured to a value of “1”.

Note: For additional details on each mode of operation, refer to the LAN8710A datasheet.

Table 2.2 MODE[2:0] Resistor Configuration

MODE[2:0]	MODE[2:0] PULL-UP/DOWN RESISTORS					
	MODE2		MODE1		MODE0	
	R28	R33	R29	R32	R30	R31
000 10BASE-T Half Duplex Auto-neg disabled	*Depopulate*	**Populate**	*Depopulate*	**Populate**	*Depopulate*	**Populate**
001 10BASE-T Full Duplex Auto-neg disabled	*Depopulate*	**Populate**	*Depopulate*	**Populate**	**Populate**	*Depopulate*
010 100BASE-TX Half Duplex Auto-neg disabled	*Depopulate*	**Populate**	**Populate**	*Depopulate*	*Depopulate*	**Populate**
011 100BASE-TX Full Duplex Auto-neg disabled	*Depopulate*	**Populate**	**Populate**	*Depopulate*	**Populate**	*Depopulate*
100 100BASE-TX Half Duplex Auto-neg enabled	**Populate**	*Depopulate*	*Depopulate*	**Populate**	*Depopulate*	**Populate**
101 Repeater mode	**Populate**	*Depopulate*	*Depopulate*	**Populate**	**Populate**	*Depopulate*
110 Power Down mode	**Populate**	*Depopulate*	**Populate**	*Depopulate*	*Depopulate*	**Populate**
111 (Default) All capable. Auto-neg enabled	**Populate**	*Depopulate*	**Populate**	*Depopulate*	**Populate**	*Depopulate*

2.2.3 nINT/TXER/TXD4 Pin Configuration (nINTSEL)

The nINT, TXER, and TXD4 functions share a common LAN8710A pin. This pin can operate in two functional modes: nINT (Interrupt) Mode and TXER/TXD4 Mode. The nINTSEL configuration strap is used to select one of these two modes. The EVB8710 must be properly configured for each mode as follows:

nINT Mode (Default EVB8710 Mode)

- Populate the 1-2 positions of R42 and R43 to pull-up the nINTSEL strap (nINT mode).
- Depopulate the 2-3 positions of R42 and R43.
- Depopulate R46.

TXER/TXD4 Mode

- Populate the 2-3 positions of R42 and R43 to pull-down the nINTSEL strap (TXER/TXD4 mode).
- Depopulate the 1-2 positions of R42 and R43.
- Populate R46.

Note: The nINTSEL configuration strap shares functionality with LED2. Therefore, LED2 may function active-high or active-low depending on the nINTSEL configuration. For additional information on the functionality of the nINT/TXER/TXD4 and LED2/nINTSEL pins, refer to the LAN8710A Datasheet and LAN8710A schematics.

2.2.4 Internal +1.2V Regulator Configuration (REGOFF)

The LAN8710A provides the ability to disable the internal +1.2V regulator. When the regulator is disabled, an external +1.2V must be supplied to the VDDCR pin (via TP3). Configuration of the internal regulator is controlled by the REGOFF configuration strap. The EVB8710 must be properly configured for each mode as follows:

Internal +1.2V Regulator Enabled (Default EVB8710 Mode)

- Populate the 1-2 positions of R40 and R41 to pull-down the REGOFF strap (enable regulator).
- Depopulate the 2-3 positions of R40 and R41.

Internal +1.2V Regulator Disabled

- Populate the 2-3 positions of R40 and R41 to pull-up the REGOFF strap (disable regulator).
- Depopulate the 1-2 positions of R40 and R41.

Note: The REGOFF configuration strap shares functionality with LED1. Therefore, LED1 may function active-high or active-low depending on the REGOFF configuration. For additional information on the LED1/REGOFF pin and the disabling of the internal 1.2V regulator (power sequencing requirements, etc.), refer to the LAN8710A Datasheet and LAN8710A schematics.

2.2.5 Clock Configuration

The EVB8710 can be clocked via the onboard crystal oscillator or an optional external clock.

Crystal Oscillator (Default)

The 25 MHz crystal Y1 is connected to the internal oscillator of the LAN8710A. A PLL circuit in the LAN8710A generates all the timing required by the PHY.

External Clock

The EVB8710 can be configured to use an external clock by removing crystal Y1 and resistor R20. A 25MHz +3.3V signal may then be applied to pin 1 of Y1 (which connects to pin 5 of the LAN8710A). Pin 2 of Y1 (which connects to pin 4 of the LAN8710A) should be left floating when using an external clock.

2.2.6 LEDs

Table 2.3 LEDs

REFERENCE	COLOR	INDICATION
LED1	Green	Link/Activity Active when the PHY has established a valid link with a link partner and blinks when activity is detected.
LED2	Yellow	Speed Active when a 100BASE-TX link has been established. Inactive when a 10BASE-T link has been established or during line isolation.

Note: LED1 and LED2 are located inside the RJ45 connector. LED1 and LED2 may function active-high or active-low depending on the configuration of the REGOFF and nINTSEL straps, respectively. Refer to the LAN8710A Datasheet and LAN8710A schematics for additional information.

2.2.7 Test Points

Table 2.4 Test Points

TEST POINT	DESCRIPTION	CONNECTION
TP1	+3.3V Test Point (Orange)	+3.3V
TP2	+5.0V Test Point (Red)	+5.0V
TP3	+1.2V VDDCR Test Point (Unpopulated) (Note 2.1)	+1.2V
TP4	Ground Test Point (Black)	Ground
TP5	VDDIO Test Point (Purple)	+3.3V (Note 2.2)

Note 2.1 VDDCR is the internal +1.2V regulated output. When REGOFF is enabled, the internal 1.2V regulator is disabled. In this case, an external 1.2V regulator must be supplied to test point TP3.

Note 2.2 The LAN8710A's VDDIO power may be supplied externally at a voltage other than +3.3V as described in Section 2.1, "Power," on page 3.

2.2.8 System Connections

Table 2.5 System Connections

PLUG/HEADER	DESCRIPTION	PART
T1	RJ45 with Integrated LEDs	Pulse J0011D01BNL
J1	2x14 MII Header **Note:** Refer Table 2.6 to for a full pin list	Adam Tech PH2-28-U-A
P1	40-pin Female MII Connector **Note:** Refer Table 2.7 to for a full pin list	Tyco 5173278-2

Table 2.6 J1 - 2x14 MII Header Pinout

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	nRST	15	TXD1
2	MDIO (Note 2.3)	16	TXD2
3	MDC	17	TXD3
4	RXD3/PHYAD2	18	CRS_DV/COL/MODE2
5	RXD2/RMIISEL	19	CRS
6	RXD1/MODE1	20	Ground
7	RXD0/MODE0	21	nINT (Note 2.4)
8	RXDV	22	VDDIO
9	RXCLK/PHYAD1	23	+3.3V
10	RXER/RXD4/PHYAD0	24	Ground
11	TXER/TXD4 (Note 2.4)	25	Ground
12	TXCLK	26	Ground
13	TXEN	27	Ground
14	TXD0	28	Ground

Note 2.3 Resistor R11 acts as a pull-up on the MDIO pin. In most situations, the MAC circuitry provides this pull-up and R11 is not required.

Note 2.4 Pins 11 and 21 of the J1 header must be configured to properly connect to the nINT/TXER/TXD4 pin of the LAN8710A. Depending on the configured mode, nINT or TXER/TXD4, R46 must be depopulated or populated. Refer to Section 2.2.3, "nINT/TXER/TXD4 Pin Configuration (nINTSEL)," on page 6 for additional information.

Table 2.7 P1 - 40-Pin Female MII Connector Pinout

PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION
1	+5V	11	TXER (Note 2.5)	21	+5V	31	GND
2	MDIO	12	TXCLK	22	GND	32	GND
3	MDC	13	TXEN	23	GND	33	GND
4	RXD3	14	TXD0	24	GND	34	GND
5	RXD2	15	TXD1	25	GND	35	GND
6	RXD1	16	TXD2	26	GND	36	GND
7	RXD0	17	TXD3	27	GND	37	GND
8	RXDV	18	COL	28	GND	38	GND
9	RXCLK	19	CRS	29	GND	39	GND
10	RXER	20	+5V	30	GND	40	+5V

Note 2.5 To use the TXER signal from the MAC, the nINT/TXER/TXD4 pin and R46 must be configured properly. Refer to Section 2.2.3, "nINT/TXER/TXD4 Pin Configuration (nINTSEL)," on page 6 for additional information.

2.2.9 Switches

Table 2.8 Switches

SWITCH	DESCRIPTION	FUNCTION
S1	Reset switch	When pressed, triggers a board reset.

2.3 Mechanicals

Figure 2.2 details the EVB8710 mechanical dimensions.

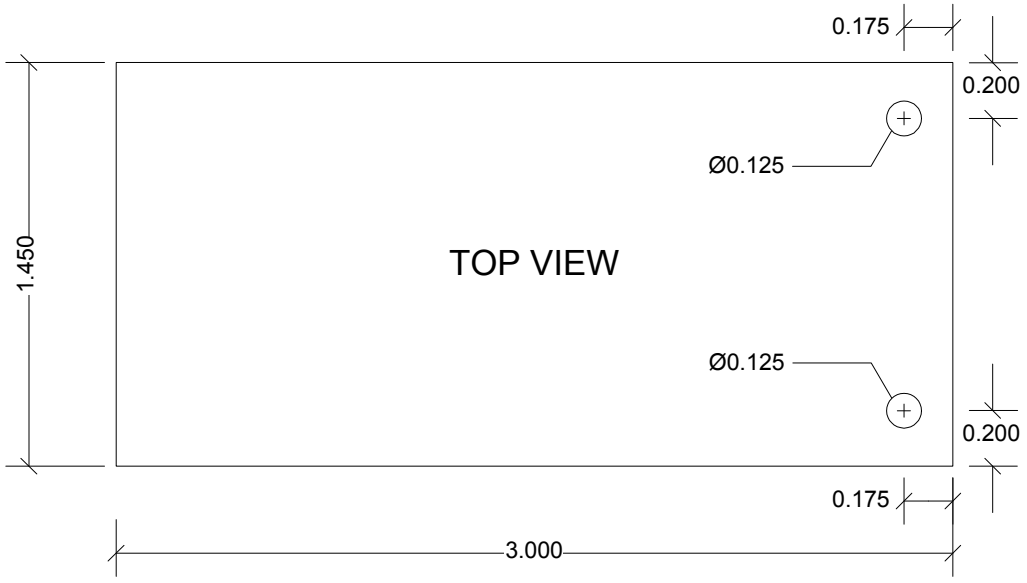


Figure 2.2 EVB8710 Mechanicals

3 User Manual Revision History

Table 3.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (05-24-10)	All	Entire document revised for new EVB version; consistency with latest EVB User Manual layout.
Rev. 1.0 (04-06-09)	Initial Release	

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