ALPHA & OMEGA SEMICONDUCTOR

# AON2403

## 12V P-Channel MOSFET

### General Description

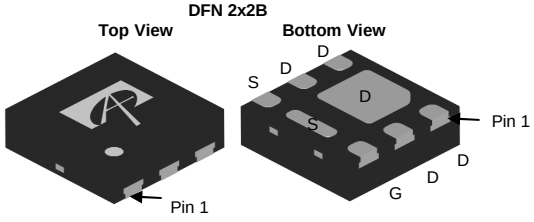
The AON2403 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

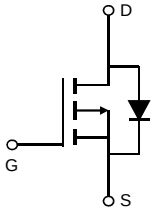
### Product Summary

| | |
|---|---|
| $V_{DS}$ | -12V |
| $I_D$ (at $V_{GS}$=-4.5V) | -8A |
| $R_{DS(ON)}$ (at $V_{GS}$ =-4.5V) | < 21mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$ =-2.5V) | < 28mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$ =-1.8V) | < 40mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$ =-1.5V) | < 54mΩ |

Green Product

DFN 2x2B




**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -12 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±8 | V |
| Continuous Drain Current [G] | $T_A$=25°C | $I_D$ | -8 | A |
| | $T_A$=70°C | | -6 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | -32 | A |
| Power Dissipation [A] | $T_A$=25°C | $P_D$ | 2.8 | W |
| | $T_A$=70°C | | 1.8 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | °C |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 37 | 45 | °C/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 66 | 80 | °C/W |

**Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=-250µA, $V_{GS}$=0V | -12 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=-12V, $V_{GS}$=0V | | | -1 | µA |
| | | $T_J$=55°C | | | -5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±8V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=-250µA | -0.3 | -0.6 | -0.9 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=-4.5V, $V_{DS}$=-5V | -32 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=-4.5V, $I_D$=-8A | | 16.5 | 21 | mΩ |
| | | $T_J$=125°C | | 19.3 | 25 | |
| | | $V_{GS}$=-2.5V, $I_D$=-6A | | 21.5 | 28 | mΩ |
| | | $V_{GS}$=-1.8V, $I_D$=-4A | | 30 | 40 | mΩ |
| | | $V_{GS}$=-1.5V, $I_D$=-1A | | 36 | 54 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=-5V, $I_D$=-8A | | 33 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=-1A,$V_{GS}$=0V | | -0.6 | -1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | -3.5 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=-6V, f=1MHz | | 1370 | | pF |
| $C_{oss}$ | Output Capacitance | | | 350 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 258 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | 10 | | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=-4.5V, $V_{DS}$=-6V, $I_D$=-8A | | 12.7 | 18 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 1.7 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 3.4 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=-4.5V, $V_{DS}$=-6V, $R_L$=0.75Ω, $R_{GEN}$=3Ω | | 11 | | ns |
| $t_r$ | Turn-On Rise Time | | | 25 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 70 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 41.5 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=-8A, dI/dt=100A/µs | | 20.7 | | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=-8A, dI/dt=100A/µs | | 5.2 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C.
B. The Power dissipation $P_D$ is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial $T_J$=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25° C.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

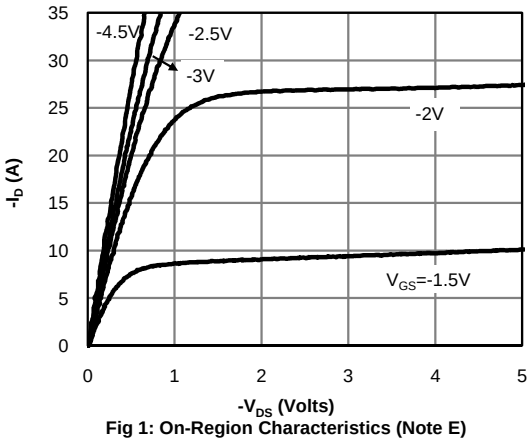



Fig 1: On-Region Characteristics (Note E)

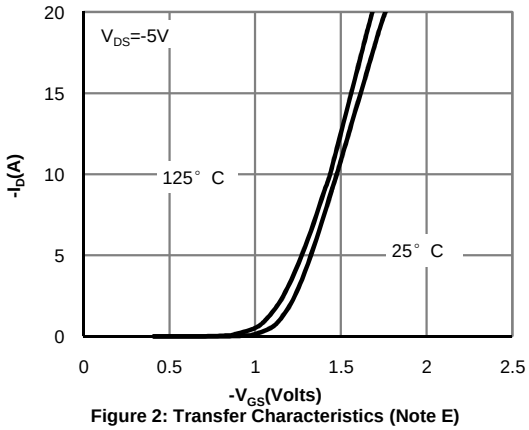



Figure 2: Transfer Characteristics (Note E)

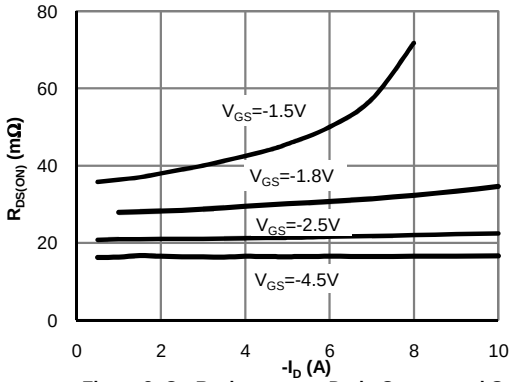



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

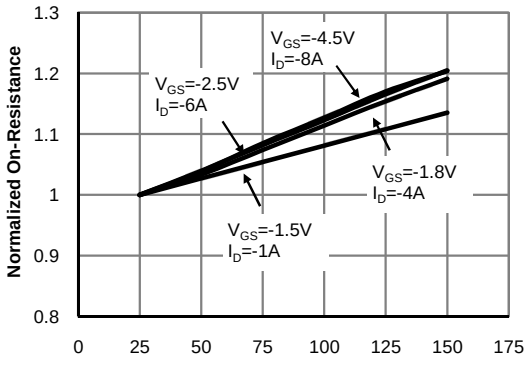



Figure 4: On-Resistance vs. Junction Temperature (Note E)

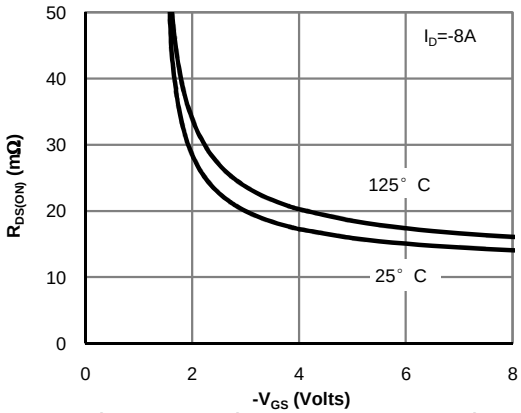



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

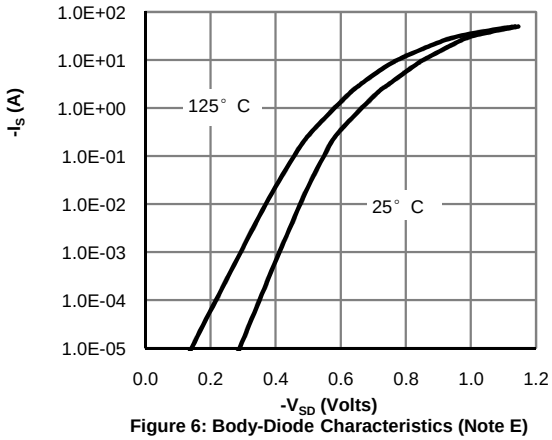



Figure 6: Body-Diode Characteristics (Note E)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

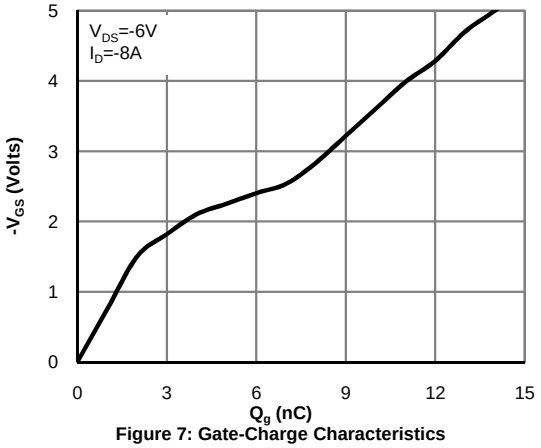



Figure 7: Gate-Charge Characteristics

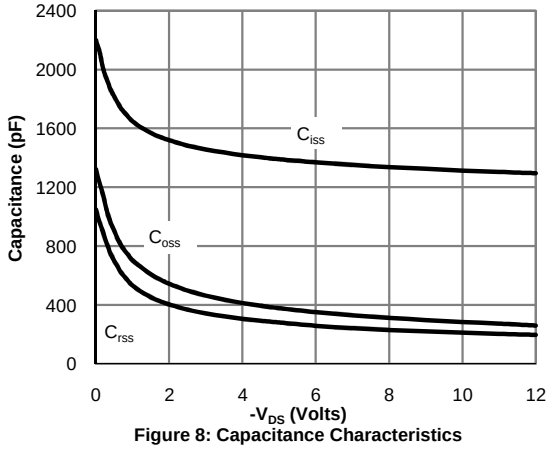



Figure 8: Capacitance Characteristics

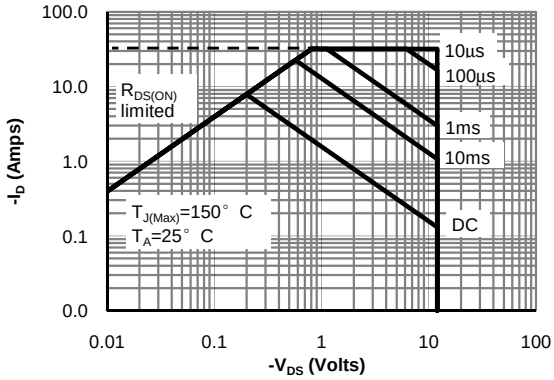



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

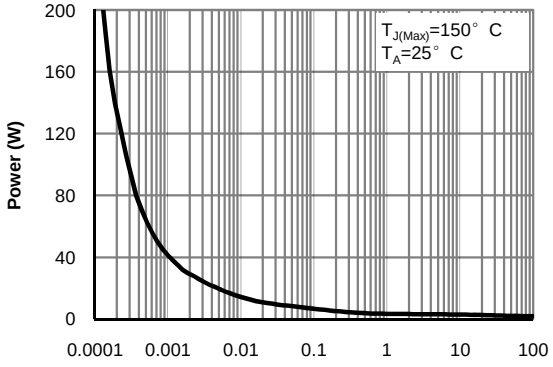



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

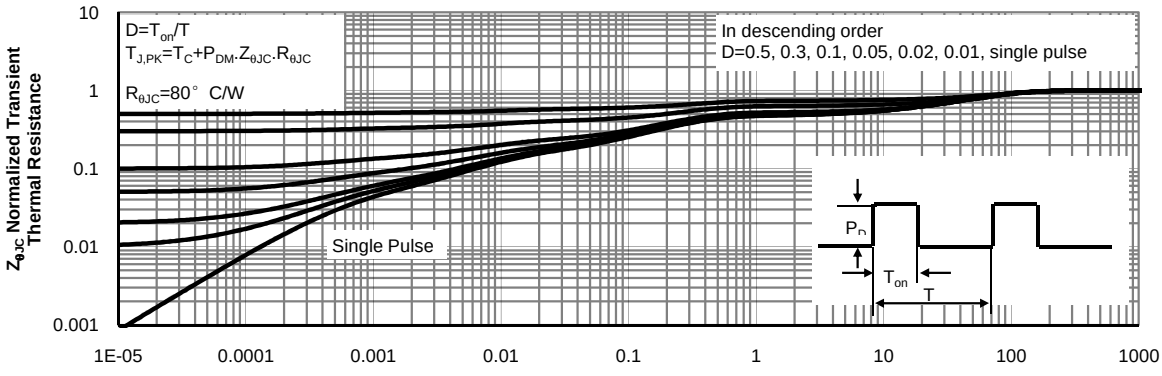
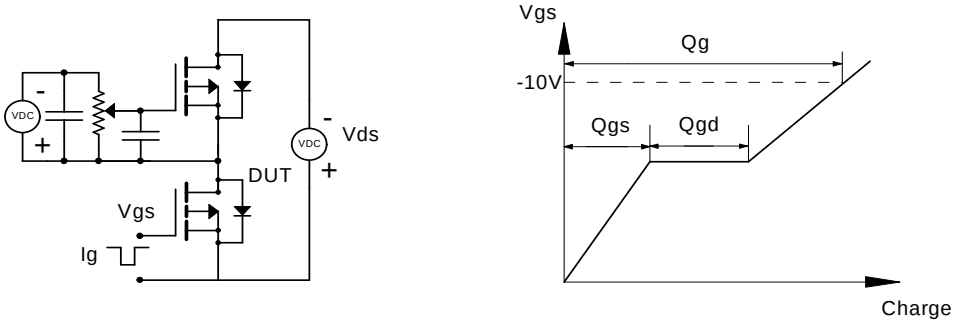
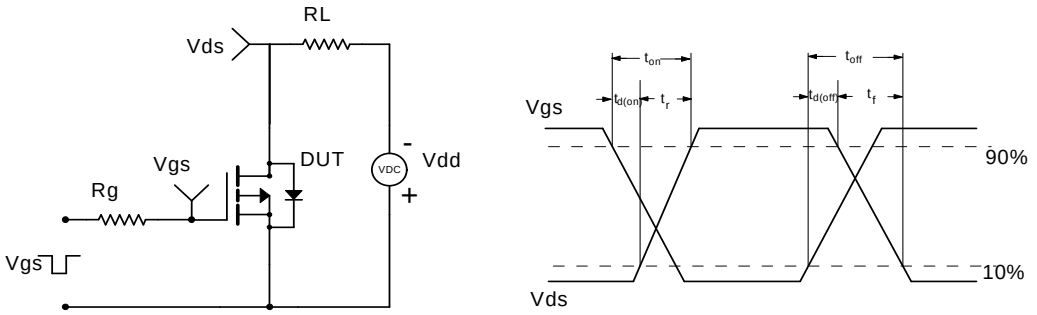



Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

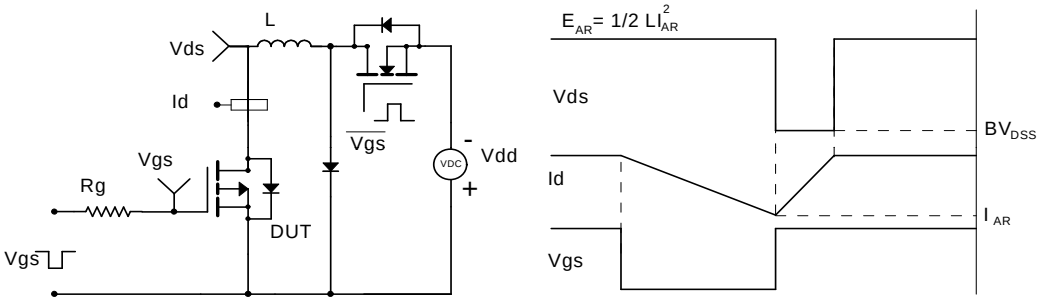
## Gate Charge Test Circuit & Waveform



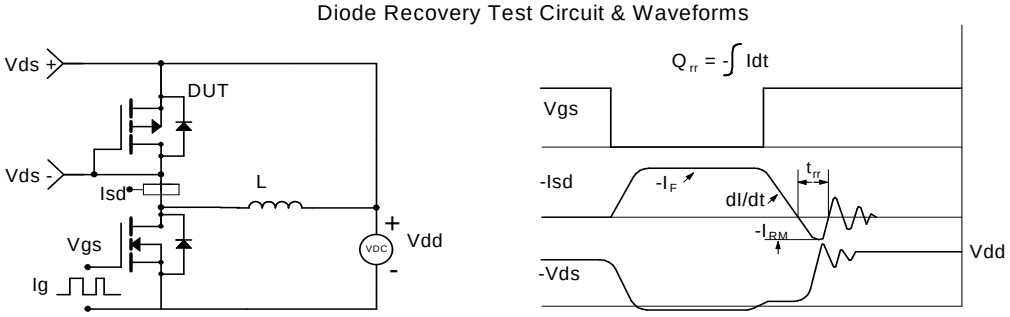

## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms



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