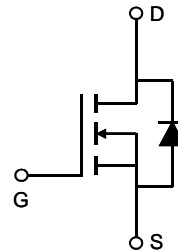
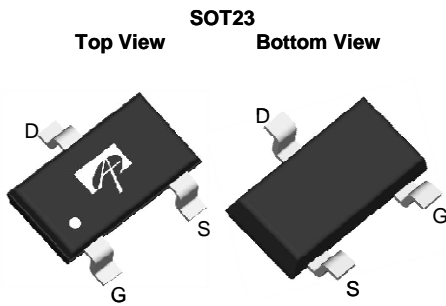


General Description

The AO3414 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.

Features

$V_{DS} = 20V$
 $I_D = 3A$ ($V_{GS} = 4.5V$)
 $R_{DS(ON)} < 62m\Omega$ ($V_{GS} = 4.5V$)
 $R_{DS(ON)} < 70m\Omega$ ($V_{GS} = 2.5V$)
 $R_{DS(ON)} < 85m\Omega$ ($V_{GS} = 1.8V$)



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ^A	$T_A=25^\circ C$	3	A
	$T_A=70^\circ C$	2.5	
Pulsed Drain Current ^B	I_{DM}	16	
Power Dissipation ^A	$T_A=25^\circ C$	1.4	W
	$T_A=70^\circ C$	0.9	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	70	90	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	100	125
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	63	80	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±8V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	0.4	0.7	1	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	16			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =4.5V, I _D =3A T _J =125°C		51 68	62 85	mΩ
		V _{GS} =2.5V, I _D =2.8A		58	70	
		V _{GS} =1.8V, I _D =2.5A		68	85	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =3A		11		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =10V, f=1MHz		260	320	pF
C _{oss}	Output Capacitance		48		pF	
C _{rss}	Reverse Transfer Capacitance		27		pF	
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		3	4.5	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =10V, I _D =3A		2.9	3.8	nC
Q _{gs}	Gate Source Charge		0.4		nC	
Q _{gd}	Gate Drain Charge		0.6		nC	
t _{D(on)}	Turn-On DelayTime	V _{GS} =5V, V _{DS} =10V, R _L =3.3Ω, R _{GEN} =6Ω		2.5		ns
t _r	Turn-On Rise Time		3.2		ns	
t _{D(off)}	Turn-Off DelayTime		21		ns	
t _f	Turn-Off Fall Time		3		ns	
t _{rr}	Body Diode Reverse Recovery Time	I _F =3A, di/dt=100A/μs		14	19	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =3A, di/dt=100A/μs		3.8		nC

A: The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

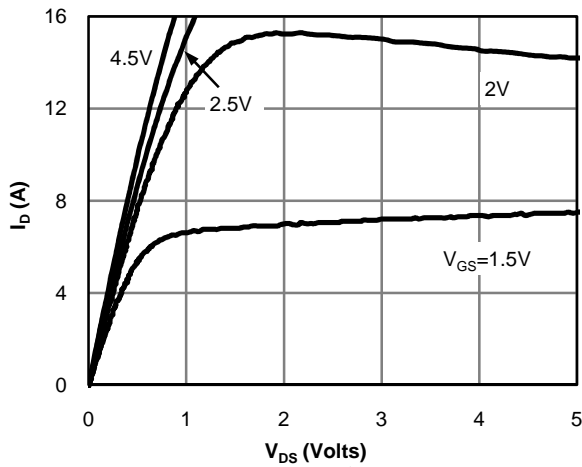


Figure 1: On-Region Characteristics

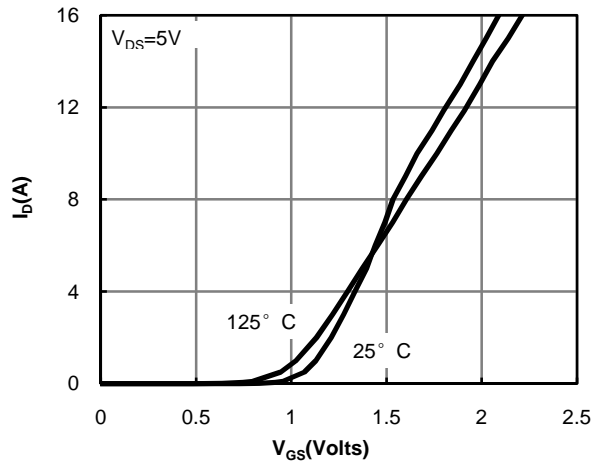


Figure 2: Transfer Characteristics

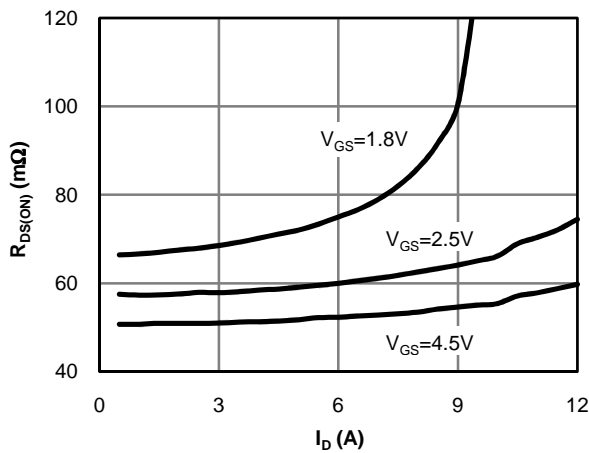


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

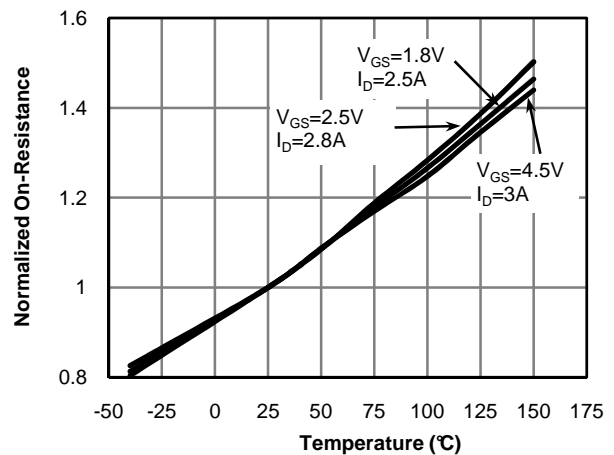


Figure 4: On-Resistance vs. Junction Temperature

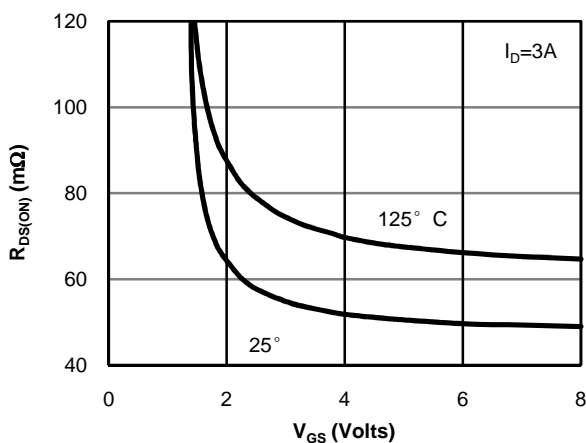


Figure 5: On-Resistance vs. Gate-Source Voltage

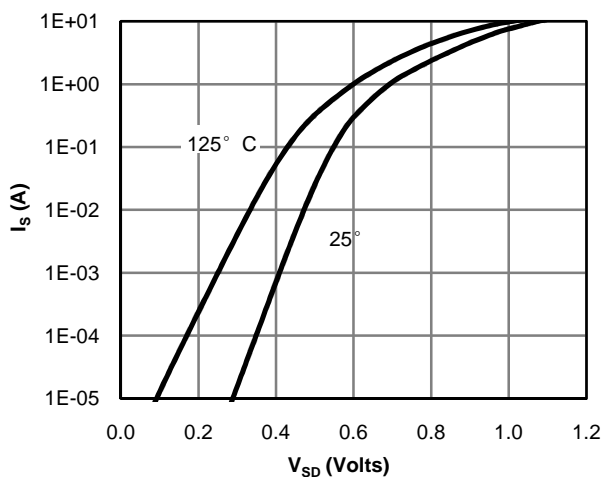


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

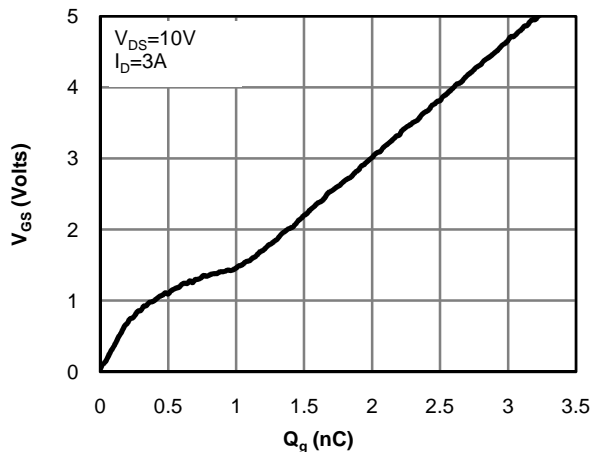


Figure 7: Gate-Charge Characteristics

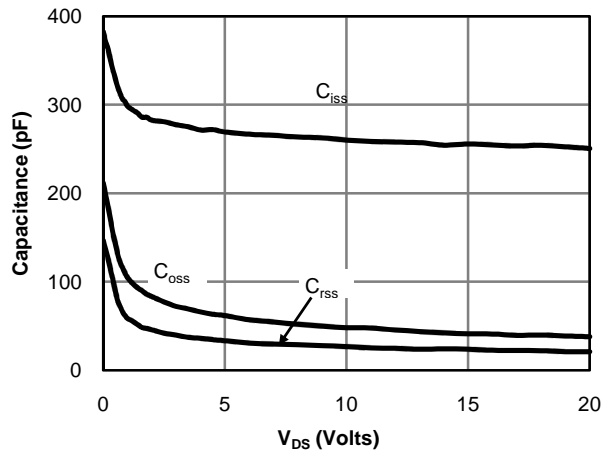


Figure 8: Capacitance Characteristics

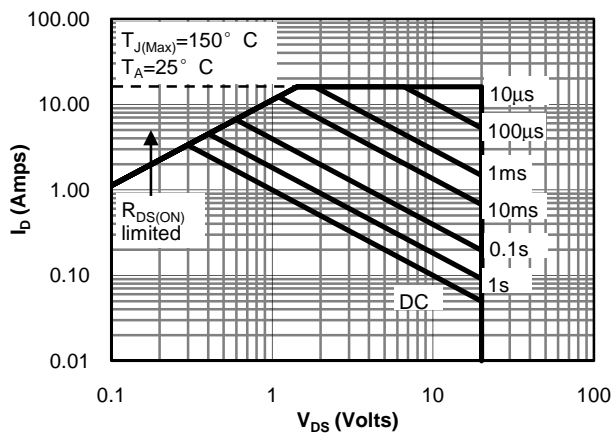


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

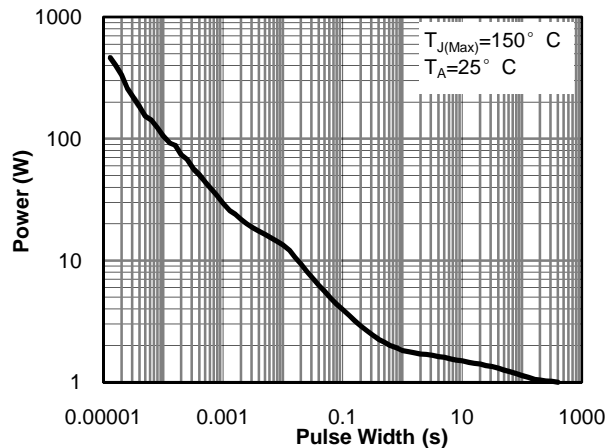


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

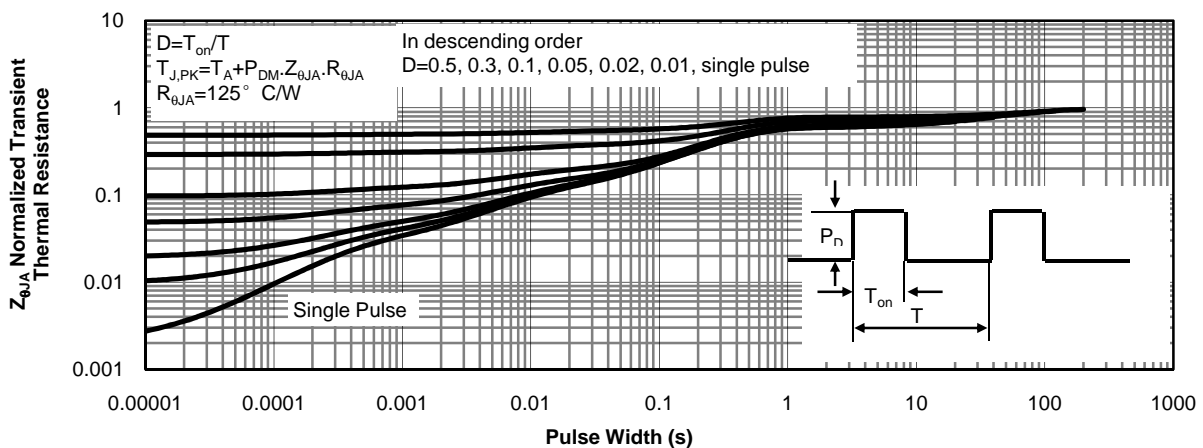
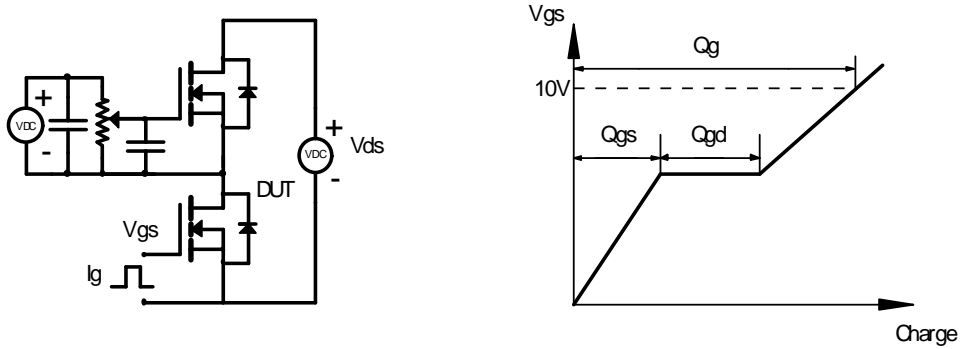
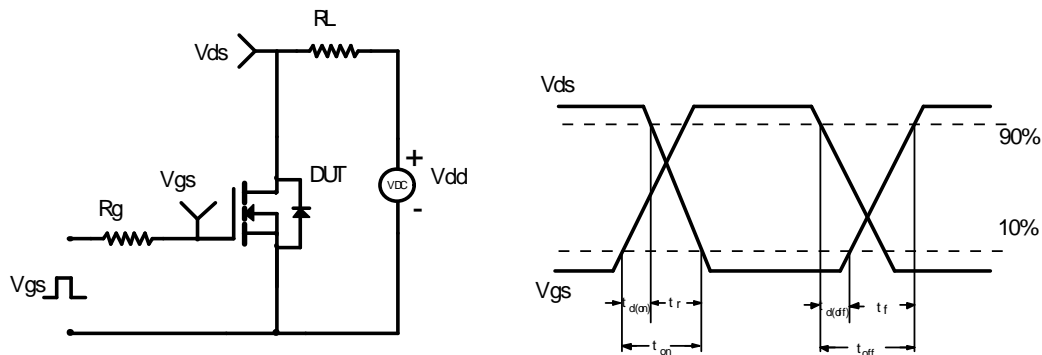


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

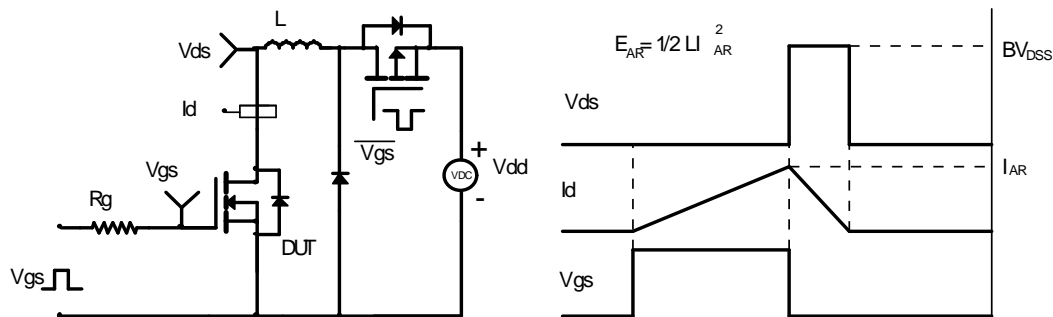
Gate Charge Test Circuit & Waveform



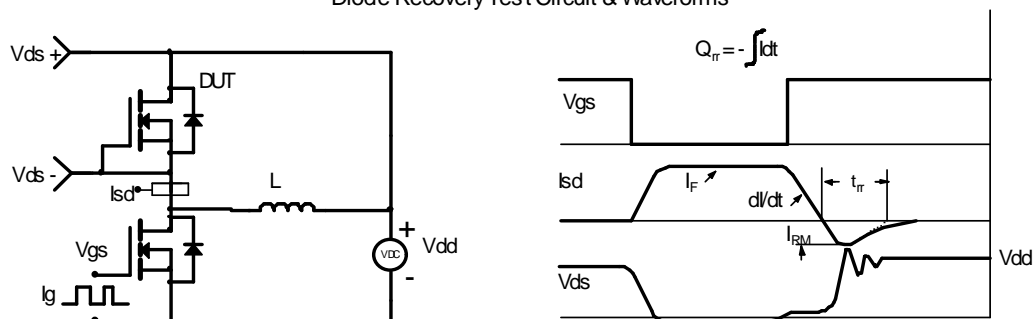
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



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