QorIQ LS1012A Reference Design Board Manual

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Overview

1.1 Introduction

The QorIQ LS1012A Reference Design board (LS1012ARDB) is a compact form-factor tool for evaluating LS1012A application solutions. The LS1012ARDB provides an Arduino shield expansion connector for easy prototyping of additional components, such as an NXP NFC Reader module.

The LS1012ARDB comes in a compact 5.59 in x 5.59 inch form factor that allows mounting in an enclosure. An SDIO based WiFi card (provided in kit) can be mounted in the SD connector to facilitate evaluation and development of low power WiFi connectivity solution. The system is lead-free and RoHS-compliant.

The LS1012A processor is built on the LS architecture combining one ARM® A53 processor core with the datapath acceleration and network, peripheral interfaces required for networking, wireless infrastructure, and the general-purpose embedded applications.

The LS1012ARDB onboard resources and debugging devices allow you to:
  • Upload and run code
  • Use the LS1012ARDB as a demonstration tool

A software application developed for the LS1012ARDB can run with various input/output data streams, such as PCIe, SGMII, or SATA connections. The board support package (BSP) and Application solutions kit (ASK) supported on the LS1012ARDB are developed using the Linux operating system.

1.2 Related documentation

Table 1-1 lists the additional documents that you can refer to, for more information about the LS1012ARDB.

Some of these documents may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local NXP field applications engineer or sales representative.

Table 1-1. Related documentation

Document	Description
QorIQ LS1012A Development System Getting Started Guide	Explains the LS1012ARDB settings and physical connections needed to boot the board.
QorIQ LS1012ARDB Errata	Lists and describes all known errata for the LS1012ARDB. It also describes the available workaround for each errata and their detailed explanation, where necessary.
QorIQ LS1012A Family Reference Manual	Provides a detailed description of the LS1012A processor and features, such as memory mapping, interfaces, chip features, and clock information.
QorIQ LS1012A Data Sheet	Contains the LS1012A information on pin assignments, electrical characteristics, power supply specifications, package information, and ordering information.
QorIQ LS1012A Chip Errata	Lists the details of all known silicon errata for LS1012A.
QorIQ LS1012A Design Checklist, AN5192	This document provides recommendations for new designs based on LS1012A. This document can also be used to debug newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

1.3 Acronyms and abbreviations

The following table lists the acronyms and abbreviations used in this document.

Table 1-2. Acronyms and abbreviations

Term	Description
BLE	Bluetooth low energy
DNP	Do not populate
DDR	Double Data Rate
DRAM	Dynamic random-access memory
DUART	Dual universal asynchronous receiver/transmitter
DUT	Device Under Test
EMI	Ethernet Management interface
eMMC	Embedded Multimedia Card
SDHC	Secure Digital High Capacity Card
SPI	Serial Peripheral Interface
FET	Field-effect transistor
GPIO	General-purpose input/output

Table continues on the next page...

Table 1-2. Acronyms and abbreviations (continued)

Term	Description
I2C	Inter-Integrated Circuit Multi-Master Serial Computer Bus
JTAG	Joint Test Action Group (IEEE 1149.1 standard)
LDO	Low-dropout
LSB	Least Significant Bit
MAC	Media access control
OTG	On-The-Go
PLL	Phased Lock Loop
PPFE	Programmable Packet Forwarding Engine
PS	Power supply
PSU	Power supply unit
RCW	Reset Configuration Word
REFCLK	Reference Clock (Clock Synthesizer Input Value)
RGMII	Reduced Gigabit Media Independent Interface
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDA	Serial data line
SDHC	Secure Digital High Capacity
SerDes	Serializer/deserializer; for example PCIe, SGMII, and SATA
SGMII	Serial Gigabit Media Independent Interface
SRAM	Static Random-Access Memory
SYSCLK	System Clock
SWD	Serial Wire Debug
TAP	Test Access Port; for example, USB TAP or Ethernet TAP
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USBCLK	USB Clock
WP	Write protected
HCSL	High Speed Current Steering Logic

1.4 LS1012ARDB features

The following table lists the features of the LS1012ARDB.

Table 1-3. LS1012ARDB features

LS1012ARDB feature	Specification	Description
Processor	LS1012A processor	LS1012A processor with single core[1]

Table continues on the next page...

Table 1-3. LS1012ARDB features (continued)

LS1012ARDB feature	Specification	Description
High-speed serial ports (SerDes)	3 SerDes lanes with speed up to 6 Gbit/s, for selected protocols.	• SGMII 1G PHY • One SATA connector with 22-pin power and signal connector. • Supports PCIe TXCLK 100 MHz for potential use by an external PCIe endpoint. • One half-mini PCIe slot supporting PCIe Gen1/2 cards
DDR controller	One 16-bit DDR3L SDRAM memory	• 1 GB memory • Supports data rates up to 1 GT/s.
Ethernet	Two Ethernet controllers	• Two quad-speed Ethernet MACs supporting SGMII 1G and RGMII 10/100/1000 Gbit/s. • RJ45 connector on RGMII supports PoE.
USB 2.0/3.0	One SuperSpeed USB 2.0/3.0 port and one USB 2.0 port	• USB 3.0 port is configured as On-The-Go (OTG) with a Micro-AB connector. • USB 2.0 port is a debug port (CMSIS DAP) and is configured always as Type-B device.
SDHC1		• Supports 1 SD card connector
SDHC2		• eMMC memory (512 MB)
SPI	SPI	• SC16IS752IBS SPI to Dual UART bridge • Arduino
QSPI	One QSPI controller	• Onboard 64 MB QSPI flash memory running at speed up to 50 MHz for single IO boot and 83.3 MHz for Dual IO boot. • Off-board QSPI emulation support • One additional virtual bank support.
Serial ports	UART (Console) 2x UARTs (from SC16IS752IBS)	• UART1 (Without flow control for console) • 2x UART (with flow control) from SC16IS752IBS to KW41 and Arduino headers.
SAI	Audio interface	• One SAI port, SAI 2 with full duplex support, available for use through Arduino connector
I2C		• One I2C bus with connectivity to accelerometer, magnetometer, KW41, and other devices for controlling and monitoring the board.
Debug features		• ARM Cortex® 10-pin JTAG connector for LS1012A • SWD connector for KW41 • CMSIS DAP through K22 microcontroller
Package		• Package type is 9.6 mm x 9.6 mm, 211 Flip Chip Land Grid Array (FC-LGA) • Socket and heat sink are included
Clocks		• 25 MHz clock for LS1012A • 25 MHz Reference clock for the SGMII PHY • 25 MHz reference clock for the RGMII PHY • Reference clock for mini PCIe slot with option to feed from TXCLK (SERDES Lane A) of LS1012A • Crystal for K22 • Crystal for K41
Power supplies		• 12 V DC input through Adaptor or PoE • 3.3 V and 5 V and onboard supply

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Table 1-3. LS1012ARDB features

LS1012ARDB feature	Specification	Description
		• USB 3.0/2.0 OTG (Type A and Type B support). Battery charging support from USB3.0/2.0 Type AB connector • 0.9 V, 1.35 V, and 1.8 V for VDD/Core and other board interfaces

1. For details about features of the LS1012A SoC, see *QorIQ LS1012A Family Reference Manual*.

1.5 LS1012ARDB block diagrams

Figure 1-1 shows the LS1012ARDB block diagram.
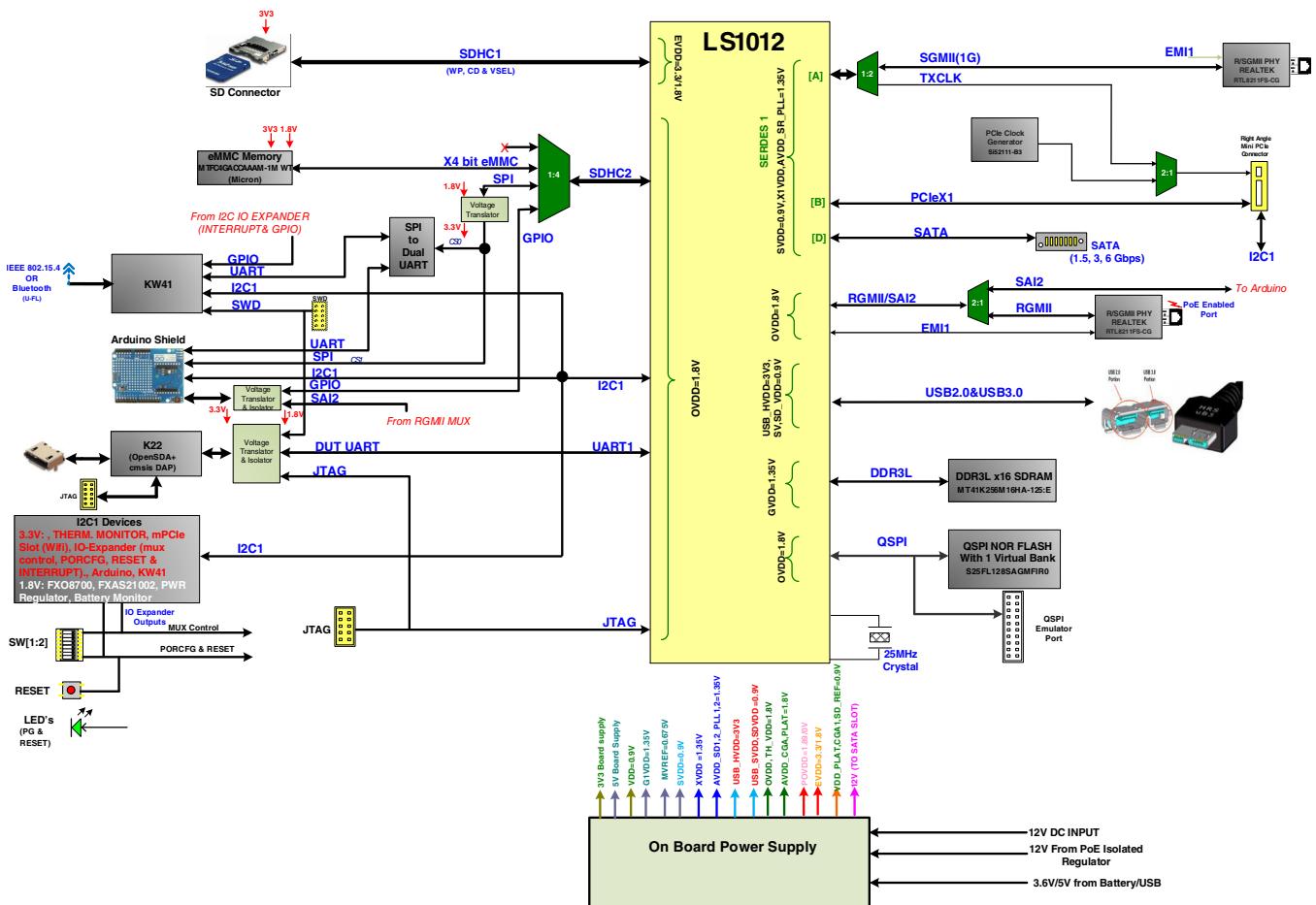
Figure 1-1. LS1012ARDB block diagram

1.6 LS1012ARDB interface

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The following figures show the LS1012ARDB chassis front and rear views.
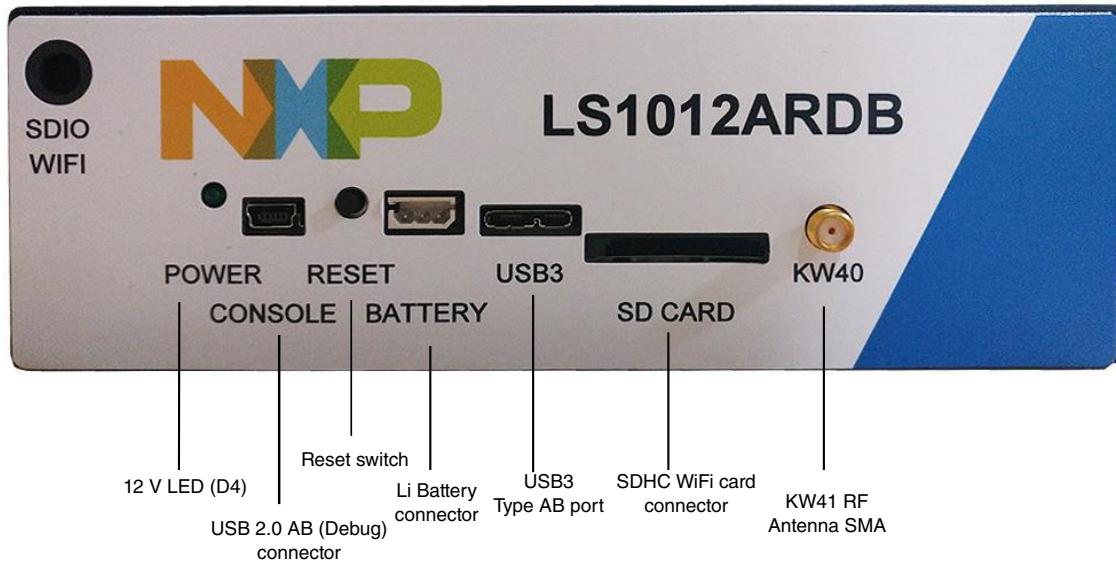
Figure 1-2. Front panel
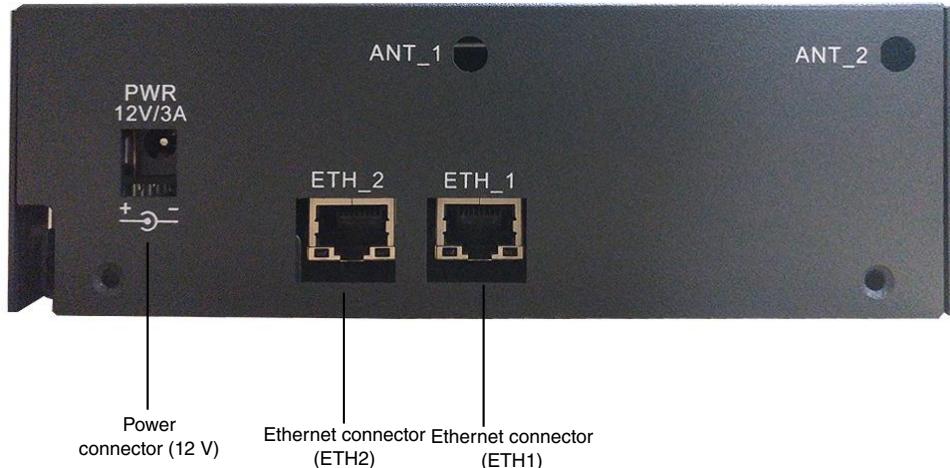
Figure 1-3. Back panel

The following figures show the LS1012ARDB top and bottom views.

Power connector (12 V)

POE

Half Mini PCIe slot

Power switch

FAN connector (12 V)

Remote Reset

RESET LED (RED)

12 V LED (Green)

SATA 22 Pin (Signal + Power)

DIP switches

I2C connector (DNP by default)

KW41 onboard F-Antenna

Ardiuno connectors

KW41 RF Antenna SMA

USB 3.0 Type AB connector

Li battery connector

Reset switch

Debug USB (CMSIS DAP)

Power-Good LED
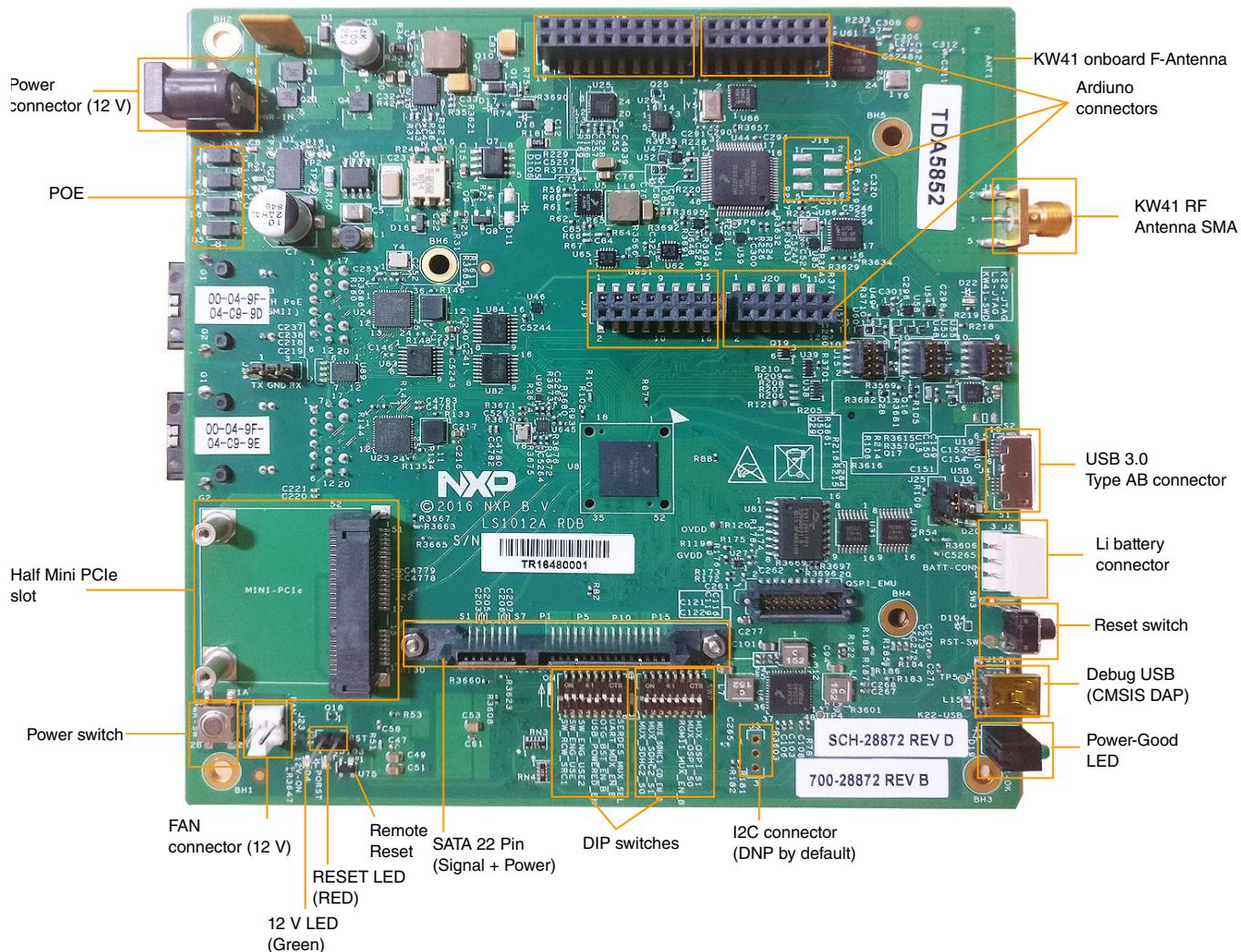
Figure 1-4. LS1012ARDB top view

Ethernet connector (ETH2) Ethernet connector (ETH1)

SD Card connector
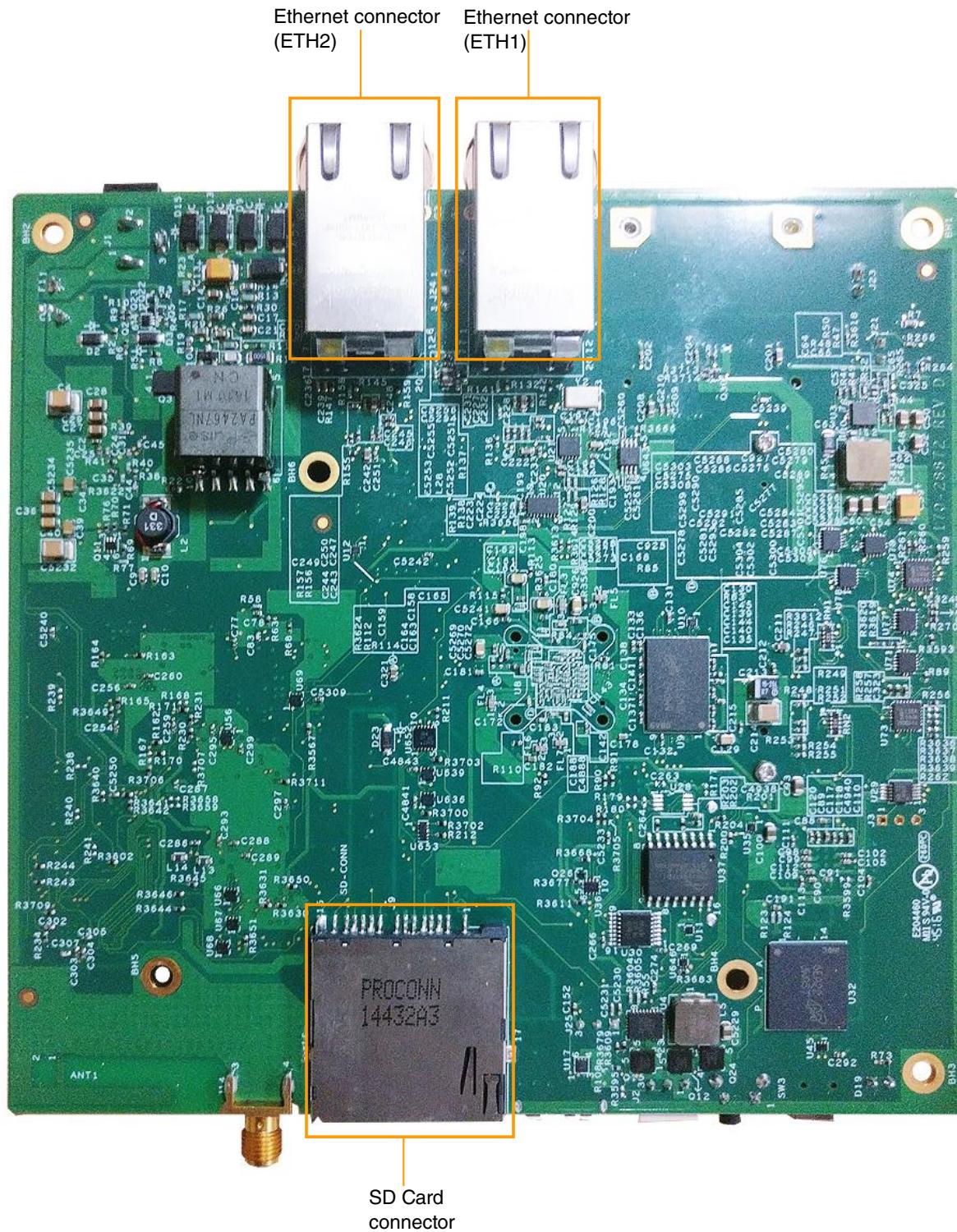
Figure 1-5. LS1012ARDB bottom view

Chapter 2
LS1012ARDB Functional Description

2.1 Processor

The LS1012ARDB includes the QorIQ LS1012A processor that features an advanced 64-bit ARM® Cortex®-A53 processor core with ECC-protected L1 and L2 cache memories along with datapath acceleration and network, peripheral interfaces required for networking, wireless infrastructure, and general purpose embedded applications.

NOTE
For details about features of the LS1012A processor, see *QorIQ LS1012A Family Reference Manual*.

2.2 Power supplies

The LS1012ARDB power supplies (PS) provide all the voltages necessary for the correct operation of the LS1012A processor, DDR3L, QSPI memory, and other onboard peripherals.

In addition to meeting required power specifications, the following goals guide the power supply architecture:
  • DUT-specific power rails are instrumented such that current measurement is possible.
  • All power supplies can be configured according to hardware specifications.

The following figure shows the LS1012ARDB power supplies.
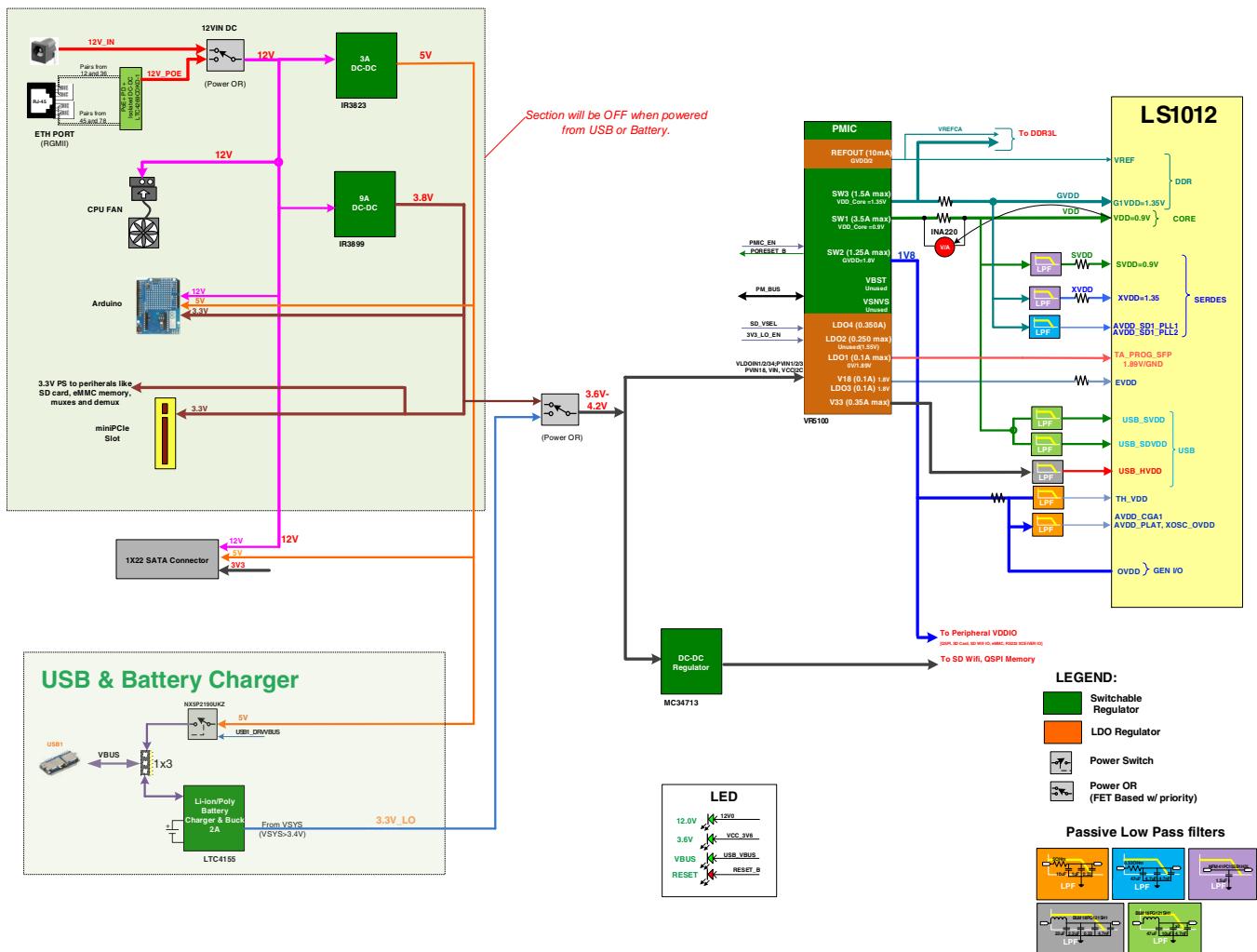
Figure 2-1. LS1012ARDB power supplies

2.2.1 Primary power supply

The LS1012ARDB can be powered up through an external 12 V DC power adaptor, a PoE system, or a battery backed USB port (USB 3.0 Type AB).

The specifications of the DC adapter are as follows:

- **Input:** 100/240 V AC, 50-60 Hz
- **Output:**
  - 12 V, 3 A DC power supply adapter (36 W) - Standard
- **Connector Size:** 5.5 mm (Outside barrel) x 2.1 mm (Inside Barrel), Center positive

The DIP switch SW1[5] can be used to enable the battery backed USB powered mode. If the SW1[5] is ON and 12 V source (DC power adaptor or PoE port) is removed, the board will be powered from the USB port or battery.

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The specifications of the battery are as follows:
- 3.6 V - 4.2 V Li-Ion/Li-Poly batteries
  It is preferred to use a battery with capacity higher than 2500 mAh. The battery charger monitors the temperature of the battery to avoid any damage. Refer to the figure to properly connect the battery terminals to the LS1012ARDB.

NOTE

The default configuration of the charger supports an NTC of 100 kilo-ohm at 25 °C. For NTC values other than 100 kilo-ohm, change the bias resistant R3609.
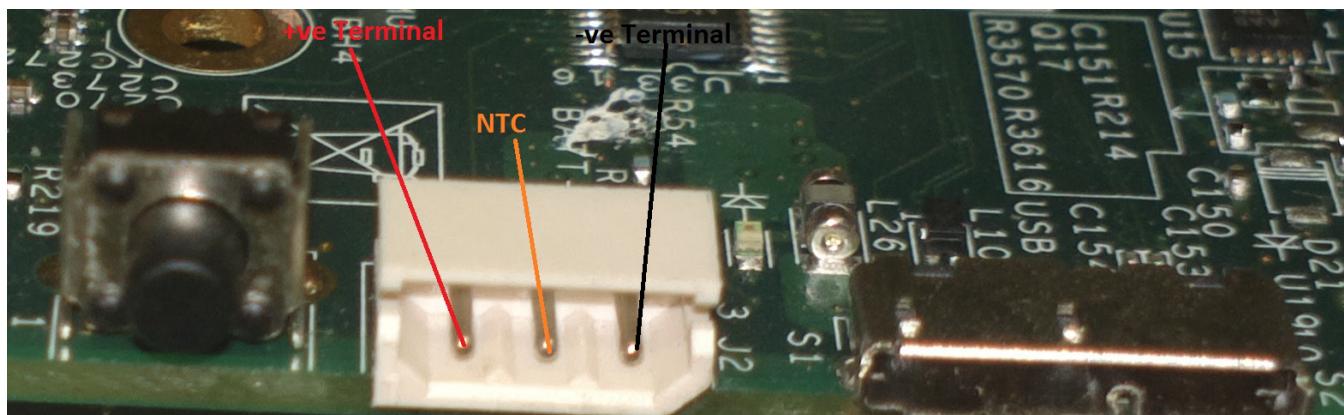
Figure 2-2. Battery

2.2.2 LS1012ARDB power supply delivery system

The following table lists different power supply components used to generate various LS1012ARDB power supply rails.

Table 2-1. LS1012ARDB power supply devices

Source voltage rail	Output voltage rail	Reference designator	Vendor	Device	Description
12V_IN	VCC_12V (3 A)	J1		12 V DC power connector	12 V power supply for 3.3 V and 5 V power regulators, SATA 3.0 connector
POE_12V	VCC_12V (2.1 A)	U1	Linear Technology	Power-over-Ethernet system that can pass power in addition to data over the Ethernet cable, LTC4269CDKD-1	

Table continues on the next page...

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Table 2-1.   LS1012ARDB power supply devices (continued)

Source voltage rail	Output voltage rail	Reference designator	Vendor	Device	Description
VCC_12V	VCC_5V (3 A)	U3	International Rectifier	IR3823	5 V power supply for USB 3.0 controller, SATA 3.0 controller, Arduino
VCC_12V	VCC_3V8 (9 A)	U2	International Rectifier	IR3899MTR1PBF	3.8 V power supply for secondary regulators VR5100 and MC34713.
USB1_PWR	VCC_3V6_BB	U4	Linear Technology	LTC4155	USB power manager and battery charger for 3.6 V - 4.2 V Li-Ion/Li-Poly batteries
VCC_3V6	VCC_3V3	U5	NXP	MC34713EP	3.3 V power supply for SD card, eMMC memory, mini PCIe slot, SATA 3.0 controller, Arduino
VCC_3V6	VCC_1V35 (1. 5 A) VCC_0V9 (3.5 A) VCC_1V8 (1.25 A) VCC_VREF (10 mA) VCC_POVDD EVDD_EN VCC_1V8_ANA HVDD_EN	U6	NXP	MC34VR5100A1EP	Power supply for: • LS1012A power supplies • DDR3L memory • 1.8 V general I/O voltage for QSPI memories, SD Card, SD Wifi IO, eMMC

2.2.3   LS1012ARDB power supply operation

This topic explains:
  • Power-ON
  • Current and power measurement

2.2.3.1   Power-ON

The LS1012ARDB is powered using an external DC PS, PoE port, or a battery backed USB power manager/battery charger. When external DC connector or Ethernet port is used to power the board, the power supply provided by the battery/USB is turned off.

The external DC PS or onboard PoE system provides 12 V DC voltage. The 12 V voltage powers primary power supply regulators (U2 and U3). U2 provides power supply to secondary regulators (U5 and U6). The secondary regulators generate power supply for peripherals, such as SD card, eMMC memory, mini PCIe slot, SATA connector, LS1012A and KW41. U3 provides power supply to SATA controller and Arduino.

Alternatively, the board can be powered from the USB port or the 3.6 V - 4.2 V Li-Ion/Li-Poly batteries that can be charged from the USB port.

The DIP switch SW1[5] can be used to enable the battery backed USB powered mode. If the SW1[5] is ON and 12 V source (DC power adaptor or PoE port) is removed, the board will be powered from the USB port or battery.

Table 2-2 describes the Power-ON sequence as implemented on the LS1012ARDB.

Table 2-2.   Power-ON process - DC adapter/PoE system

Step	Indication	Specifics	Description
1	Green LED (D14)	12 V	• Indicates 12 V PS ready status. Powered either by the external AC-DC adapter (12 V DC_IN) or PoE.
2	Green LED (D19)	5 V	• 5 V PS for SATA, USB, and Arduino/Freedom cards
		3.8 V	• Indicates 3.8 V PS ready status • Acts as source PS for secondary regulators, VR5100 and MC34713 • This power is given preference over the power supply from the battery backed USB power supply
3		3.3 V	• Power supply for 3.3 V powered devices.
		1.8 V	Power supplies provided by secondary regulator VR5100
		1.35 V	• Provides power to peripherals and LS1012A IO and PLL supplies (AV DD_PLAT, V DD_CGA1, AVDD_REF, AV DD_SD1_PLL1, AVDD_SD1_PLL2, OVDD, EV DD, XOSC_OV DD, USB_HVDD, G1VDD, and X1VDD)
4		0.9 V	• LS1012A core supplies: VDD, S1VDD, USB_SDVDD, USB_SVDD
5	Red LED (D103)		• Reset LED is deasserted.

Table 2-3.   Power-ON process - USB battery

Step	Indication	Specifics	Description
1	Green LED	R_USB1_LED	• Indicates USB supply is available on board. • Depending on the OTG configuration, this supply can either be sourced by the onboard LTC4155 battery charger with powerpath manager) or from the USB connector.
2	Green LED (D19)	VCC_3V6_BB	• This supply is generated by LTC4155 either from the USB 5 V input or a Li-ion/poly battery.
3		3.3 V	• Indicates 3.3 V power is ready
		1.8 V	Power supplies provided by secondary regulator VR5100
		1.35 V	

Table continues on the next page...

Table 2-3. Power-ON process - USB battery (continued)

Step	Indication	Specifics	Description
			• Provides power to peripherals and LS1012A IO and PLL supplies (AV DD_PLAT, V DD_CGA1, AVDD_REF, AV DD_SD1_PLL1, AVDD_SD1_PLL2, OVDD, EV DD, XOSC_OV DD, USB_HVDD, G1VDD and X1VDD)
4	Core power supply	0.9 V	• LS1012A core supplies: VDD, S1VDD, USB_SDVDD, USB_SVDD
4	Red LED (D103)		• Reset LED is deasserted.

2.2.3.2 Current and power measurement

Current/power measurements are performed by measuring voltage over fixed current shunts. The voltage reading over the shunts indicates the current values.

Current/power measurement of the LS1012A 0.9 V power domains are done by using the INA220 (U29) current/voltage/power monitor. INA220 measures current across a 2mOHM shunt resistor. The INA220 monitor is accessible through I2C controller of LS1012A.

For other power domains, such as 1.35 V, 1.8 V, and 3.3 V, 10 mohm resistors are available for current and power measurement.

The INA220 current/power monitor circuitry features are as follows:

- Reports current, voltage, and power.
- High over-temperature accuracy of 0.5 % (max).
- Current shunt sensors are 2 mohm for 0.9 V power pools.
- User-programmable calibration.
- Fast (3.4 MHz) 2-wire mode.

2.2.4 Voltage regulation

The following table explains the LS1012ARDB voltage regulation.

Table 2-4. LS1012ARDB Voltage Regulation

Power	Voltage	Device	Description
Core, VDD	0.9 V (3.5 A max)	VR5100 SW1	Powers the LS1012A SoC Core voltage
G1VDD	1.35 V	VR5100 SW3	Powers the LS1012A SoC DDR circuitry
VCC_VREF	0.675 V	VR5100 VREF LDO	

Table continues on the next page...

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Table 2-4. LS1012ARDB Voltage Regulation (continued)

Power	Voltage	Device	Description
X1VDD	1.35 V	VR5100 SW3	Powers the LS1012A SoC SerDes I/O circuitry
SVDD	0.9 V	VR5100 SW1	
AVDD_SD1_PLL1			
AVDD_SD1_PLL2			
XOSC_VDD		VR5100 SW3	VDD supply for LS1012 crystal oscillator
USB_SVDD		VR5100 SW1	Powers the LS1012A SoC USB circuitry
USB_SDVDD			
USB_HVDD	3.3 V	VR5100 V33 LDO	
POVDD		VR5100 LDO1	LS1012A SoC fuse Programming voltage
			POVDD can be enabled through I2C either from LS1012A or external I2C master.
			Otherwise, these pins are pulled down to the ground
OVDD	1.8 V (0.1 A)	VR5100 SW3	General I/O voltage
XOSC_OVDD		VR5100 SW2	OVDD supply for LS1012A crystal oscillator
EVDD		VR5100 VSD LDO	Powers the SDHC interface
			SDHC1_VSEL specifies whether to set the EVDD voltage to 3.3 V (Default) or 1.8 V

2.3 Reset

Reset to and from the LS1012A processor and other devices on the LS1012ARDB are managed by the I2C IO-expander and other discrete components.

The reset sequence can be triggered from various sources. Table 2-5 summarizes the reset activity.

Table 2-5. Reset activity

Reset Source	Reset Reason	Actions taken
Power ON	Initialization after a power cycle.	All the onboard devices are reset after a power cycle. PLL and clock circuitry initialize to default configuration.
SW3 or J21	Reset switch	No power cycle. All devices are reset. PORESET is asserted to LS1012A.
LS1012A debugger reset (J11/U44)	Reset from K22 CMSIS DAP/JTAG debugger	PORESET to LS1012A.
KW41 debugger reset (J15/U44)	Reset from K22 CMSIS DAP/JTAG debugger	Reset to KW41 MCU.
RESET_REQ_B	Reset request from LS1012A	All devices are reset.

Table continues on the next page...

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Table 2-5.   Reset activity (continued)

		PORESET to LS1012A.
I2C IO expander (I2C address 0x25)	Reset request from LS1012A or any external I2C master on J3	Reset the peripherals based on values programmed in IO Expander registers. See *IO expander datasheet for PCAL9555AHF* for register details.

The reset is asserted for about 140 ms after all power supplies are stable. This is to meet the LS1012A 100 ms reset specification. Power failure after system operation also asserts the reset to all the devices on the board.

2.4   Device configuration

The processor uses hardware-sampled pins to configure various portions of the device. The rest of the portions of the device are configured from data in RCW.

The LS1012ARDB configuration pins are described in the following table. These signal values are controlled by DIP switch, SW1. A reset cycle to LS1012A, samples the latest values on the DIP switch.

Table 2-6.   POR configuration requirements

Configuration signal	Nets sampled	Switch preset	Description
cfg_eng_use cfg_eng_use2	cfg_eng_use - CLK_OUT cfg_eng_use_2 - QSPI_A_DAT0	SW1 [3:2]	Transconductance configuration requirement of XOSC: • 00 - 0.21x • 01 - 0.55x • 10 - 0.66x • 11 - 1.00x
cfg_rcw_src1	UART1_SOUT	SW1 [1]	RCW source. • 1'b0 - Hard coded source RCW • 1'b1 - QSPI is the RCW source (default)

2.5   Clocks

The architecture of the LS1012ARDB clocks is shown in the following figure.
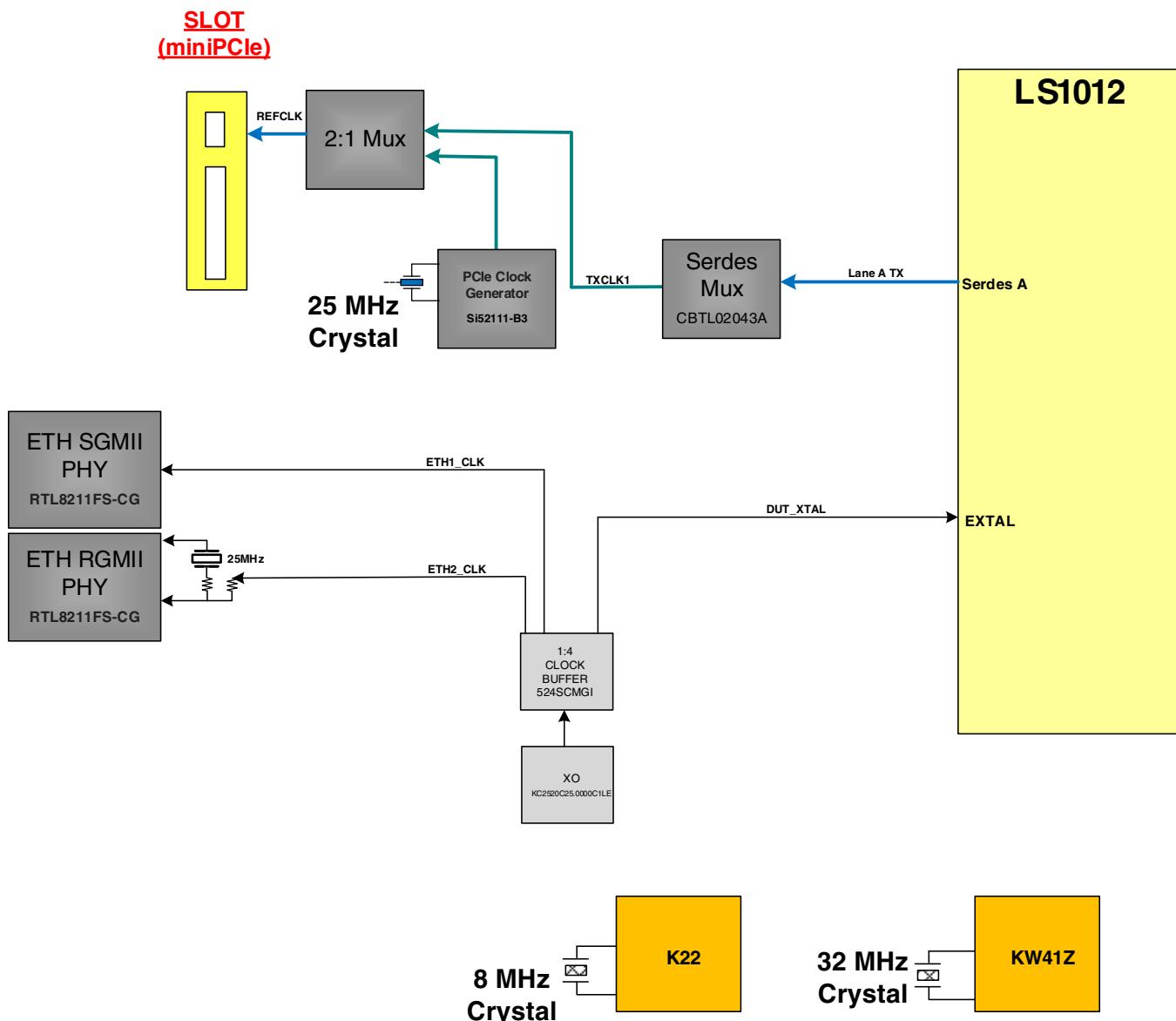
Figure 2-3. Clock architecture

The following table summarizes the LS1012ARDB clock distribution.

Table 2-7.   LS1012ARDB clocks

Clock	Frequency	Destination	Device
25MHz (EXTAL)	25 MHz	Input clock for SoC	25MHz oscillator : KC2520C25.0000C1LE00 (MFG-Kyocera) and Fan out buffer 524SCMGI (MFG-IDT)524SCMGI
CLK_OUT_25M_ETH1 (1.8 V)	25 MHz	Reference clock for the SGMII PHY	• Additive phase jitter = 50fs
CLK_OUT_25M_ETH2 (1.8 V)	25 MHz	Reference clock for the RGMII PHY	• Output skew = 50 ps (typical) • Low cost clock buffer • Input/Output clock frequency up to 200 MHz
PCIE_CLK	100 MHz	Reference clock for mini PCIe slot	Si52111-B3

Table continues on the next page...

Table 2-7. LS1012ARDB clocks (continued)

Clock	Frequency	Destination	Device
			• Low power HCSL differential output buffer • 25 MHz Crystal or clock input • PCIe Gen 1/2 compliant
SD1_TX_CLK	100 MHz	Reference clock for mini PCIe slot	LS1012A SoC
8MHz XTAL for K22	8 MHz	Crystal clock for K22	Crystal
EXTAL_32M	32 MHz	Crystal clock for KW41Z	Crystal

2.6 Double data rate (DDR) memory

The LS1012ARDB supports one 16-bit, 1 GB DDR3L SDRAM memory, running at data rates up to 1 GT/s. The part number is Micron MT41K512M16HA-125.

Following are the characteristics of the LS1012A DDR3L memory controller:

- Up to 1.0 GT/s
- Supports 16-bit operation (no ECC support)
- Support for x8, x16 devices
- Supports 1 chip select, D1_MCS_B
- The VR5100 VREF LDO takes 1.35 V supply and provides 0.675 V VREF supply to the DDR3L controller.

The memory module is powered from VCC_1V35 (1.35 V) and VCC_VREF (0.675 V) voltages provided by the VR5100 power controller (U6).

The memory interface includes all the necessary termination and I/O power, and is routed so as to achieve maximum performance of the memory bus, as shown in the following figure.

DDR3L x16 Memory
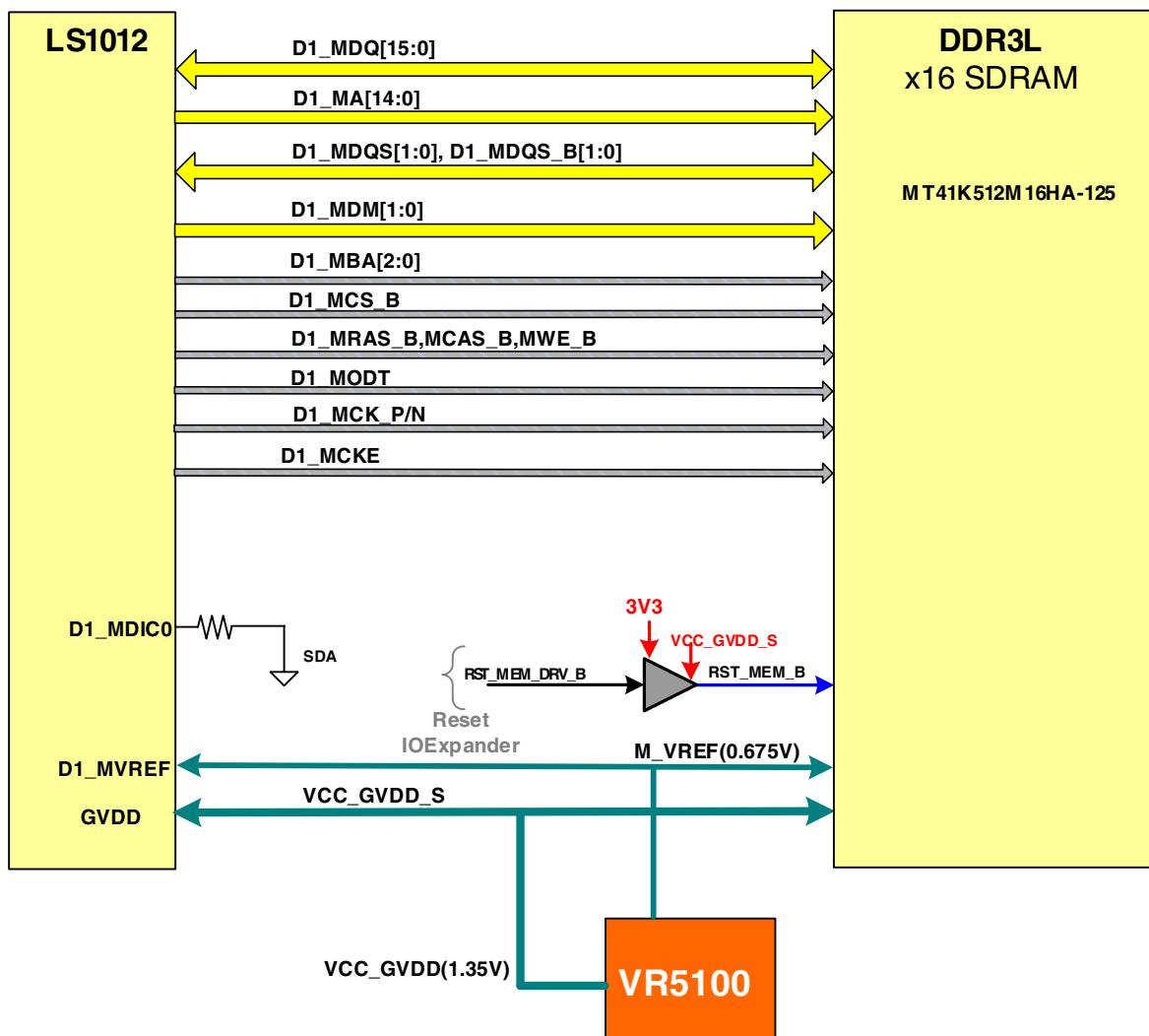
Figure 2-4. DDR3L controller

2.7 Serializer/deserializer (SerDes)

The LS1012A SerDes block provides one high-speed serial communication lane, supporting a variety of protocols, such as SATA, PCIe, and SGMII. SeeTable 2-10 for details about the SerDes protocols supported on the LS1012A processor. The following table lists the components used to support the different SerDes options.

Table 2-8. LS1012ARDB SerDes embedded devices

Manufacturer	Part number	Description
3M	5622-2222-ML	• SATA 3.0 header (22 pin)
NXP SEMI	CBTL02043A	• 2:1 mux/demux switch

Table continues on the next page...

Table 2-8.   LS1012ARDB SerDes embedded devices (continued)

Manufacturer	Part number	Description
		• I2C IO Expander/DIP SW controls the SerDes1 muxes • Lane A mux on TX lane for SGMII (1G) or PCIe TXCLK functionality
	CONN PCI EXP 52	• Half-mini PCIe slot • Supports PCIe Gen1/2 add-in cards
Realtek	RTL8211FS-CG	• SGMII 1G PHY

2.7.1   SerDes options

The following figure shows the SerDes lanes different routing options and possible SerDes combinations as implemented on the board. It provides a detailed drawing of what can be used for each interface option.

SERDES Interface

	SERDES LANES			RGMII	CFG_SD_MUX _SEL
	A	B	D		
P1.0	UNUSED	UNUSED	UNUSED		
P1.1	SGMII 2.5G	SGMII 2.5G	SATA	DISABLE	NA
P1.2	UNUSED	UNUSED	SATA	ENABLE	NA
P1.3	SGMII 1G	PCIe X1	SATA	ENABLE	0
P1.4	SGMII 1G	SGMII 1G	PCIe X1	DISABLE	NA
P1.5	SGMII 2.5G	SGMII 2.5G	PCIe X1	DISABLE	NA
P1.6	SGMII 2.5G	SGMII 1G	PCIe X1	DISABLE	NA
P1.7	TX_CLK	PCIe X1	SATA	ENABLE	1
P1.8	SGMII 1G	TX_CLK	PCIe X1	ENABLE	NA

Only P1.7 and P1.3 are supported on RDB.

Notes and Assumptions:
- Only TX for lane A is passed through MUX1 and MUX2.
- Place ac capacitors on TX lanes near the source.
- TX_CLK is a fixed 100MHz clock output for potential use by an external PCIe Endpoint.

Figure 2-5. SerDes architecture

The following table provides the lanes and speeds supported on the SerDes protocols.

Table 2-9.   Lanes and speeds supported on SerDes protocols

Mode	Lane supported	Speed
SGMII 1G	x1	1.25 Gbit/s
SATA	x1	1.5/3/6 Gbit/s
PCIe TXCLK	x1	100 MHz
PCIe	x1	2.5/5 Gbit/s

2.7.2   SerDes configuration and setup

DIP switch SW2 [1] is used to configure the SerDes multiplexer control signal, CFG_SERDES_MUX_SEL. Software can override the DIP switch settings by writing to the IO-expander directly, if required.

The clock ratio between each of the two SerDes PLLs and their respective externally supplied SD1_REF_CLK1/SD1_REF_CLK1_B inputs is determined by a set of RCW Configuration fields-SRDS_PRTCL_S1, SRDS_PLL_REF_CLK_SEL_S1, and SRDS_DIV_*_S1-as shown in this table.

Table 2-10.   LS1012A Supported SerDes Options

SRDS_PRCTL_S1 RCW[128:143]	SRDS_PLL_REF_CLK_SEL_S1	A	B	C	D	RGMII	Per Lane PLL Mapping
0x3508	0b11	sg.m1 (1G)	PCIe (x1)	Unused	SATA	MAC2	1122
0x9508	0b11	TX_CLK	PCIe (x1)	Unused	SATA	MAC2	1112

2.8   Ethernet controller

The LS1012A processor supports two Ethernet MACs, which connect to the onboard PHYs using the RGMII or SGMII protocols.

The RJ45 Ethernet jack on the LS1012ARDB has in-built magnetics.

2.8.1   SGMII port

The onboard Ethernet PHY, Realtek RTL8211FS PHY (U23), can connect to the LS1012A processor MAC1 using SGMII protocol over SerDes lane A.

Notes and Assumptions:
- MAC connected to Serdes lane B is the same MAC connected to the RGMII interface. so RGMII and SGMII (lane B) can not be use at a time.
- If the Serdes is configured for 2 SGMII interfaces, then the RGMII interface is unused (tristated unless the pinmuxing control register is configured for functionality other than EC1 RGMII).

HARDWARE BOOTSTRAP SETTINGS:
- PHY_AD[2:0] = 010: PHY Addr = 0b00010
- CFG_LDO[1:0] = 10: 1.8V (supplied by internal LDO)
- CFG_MODE[2:0] = 011 : UTP ⌠ SGMII
- TXDLY = 1: RGMII TXC clock skew = 2.0ns (through Register setting #17.8)
- RXDLY = 1: RGMII TXC clock skew = 2.0ns

CONFIG Pin	Configuration
LED0	PHYAD[0]
RXC	PHYAD[1]
RXCTL	PHYAD[2]
RXD0	RXDLY
LED1	CFG_LDO[0]
LED2	CFG_LDO[1]
RXD1	CFG_MODE[0]
RXD2	CFG_MODE[1]
RXD3	CFG_MODE[2]

Figure 2-6. SGMII port

Table 2-11.   Hardware bootstrap for Ethernet PHY settings

| Setting	Description
PHY_AD[2:0] = 010	PHY Addr = 0b00010
CFG_LDO[1:0] = 10	1.8 V (supplied by internal LDO)
CFG_MODE[2:0] = 011	UTP > SGMII
TXDLY = 1	RGMII TXC clock skew = 2.0 ns (through Register setting #17.8)
RXDLY = 1	RGMII TXC clock skew = 2.0 ns

2.8.2 RGMII port

The RGMII port is connected to the onboard Ethernet PHY, Realtek RTL8211 PHYs (U24), as shown in the following figure. The RGMII port on LS1012ARDB supports the Power over Ethernet (PoE), which can power the PoE circuit to provide 12 V supply (12V_PoE) to the board, in addition to data over the RJ45 cable.

RGMII port is muxed with SAI2 that can be used as audio interface through an Arduino shield.

See I2C mux select IO-expander for muxing details.

LS1012A RGMII operates on OVDD, which is 1.8 V.
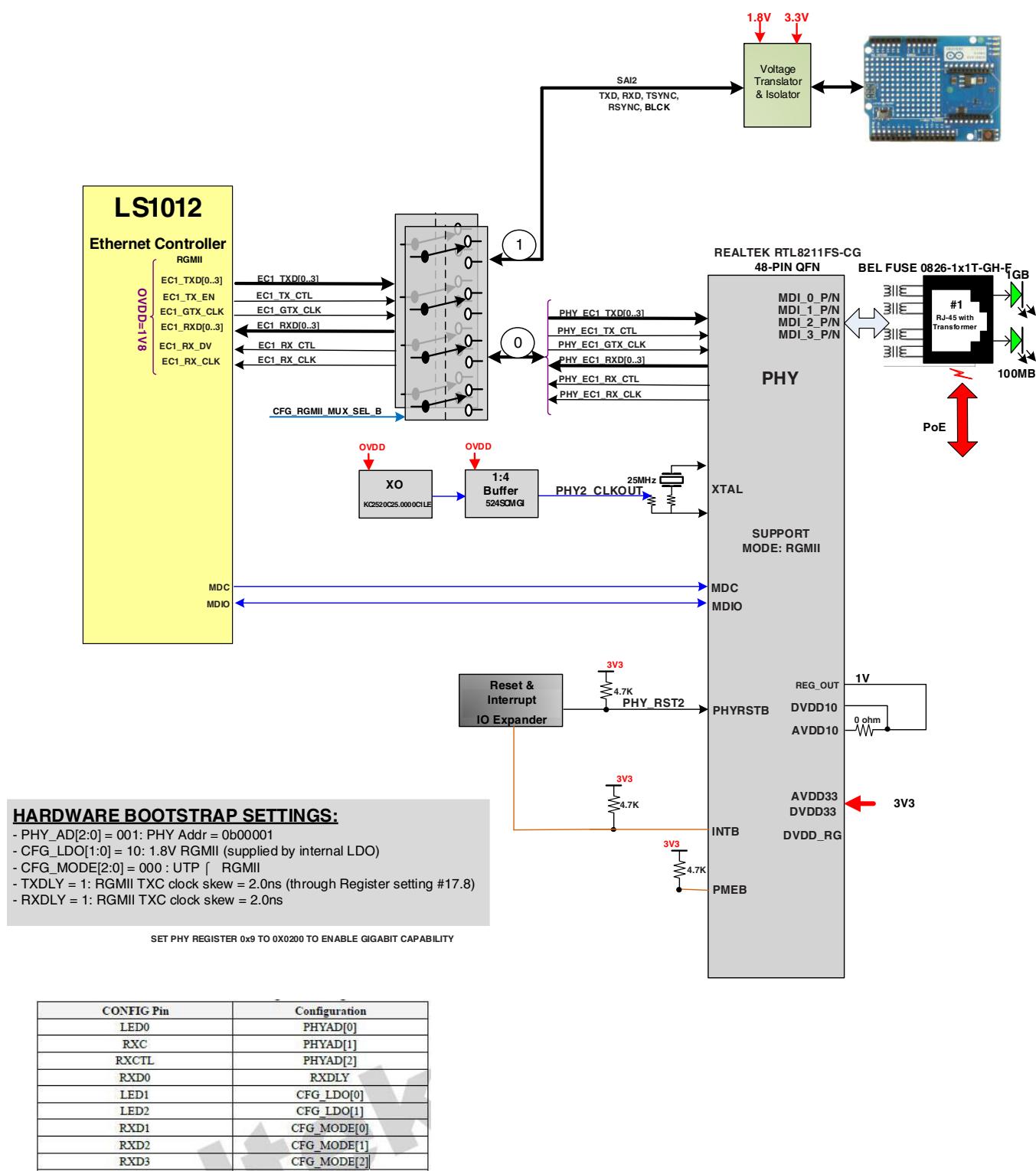
Figure 2-7. RGMII port

HARDWARE BOOTSTRAP SETTINGS:
- PHY_AD[2:0] = 001: PHY Addr = 0b00001
- CFG_LDO[1:0] = 10: 1.8V RGMII (supplied by internal LDO)
- CFG_MODE[2:0] = 000 : UTP ∫ RGMII
- TXDLY = 1: RGMII TXC clock skew = 2.0ns (through Register setting #17.8)
- RXDLY = 1: RGMII TXC clock skew = 2.0ns

SET PHY REGISTER 0x9 TO 0X0200 TO ENABLE GIGABIT CAPABILITY

CONFIG Pin	Configuration
LED0	PHYAD[0]
RXC	PHYAD[1]
RXCTL	PHYAD[2]
RXD0	RXDLY
LED1	CFG_LDO[0]
LED2	CFG_LDO[1]
RXD1	CFG_MODE[0]
RXD2	CFG_MODE[1]
RXD3	CFG_MODE[2]

Table 2-12.   Hardware bootstrap for Ethernet PHY settings

Setting	Description
PHY_AD[2:0] = 001	PHY Addr =

Table continues on the next page...

Table 2-12. Hardware bootstrap for Ethernet PHY settings (continued)

Setting	Description
	0b00001
CFG_LDO[1:0] = 10	1.8 V RGMII (supplied by internal LDO)
CFG_MODE[2:0] = 000	UTP > RGMII
TXDLY = 1	RGMII TXC clock skew = 2.0 ns (through Register setting #17.8)
RXDLY = 1	RGMII TXC clock skew = 2.0 ns

2.9 SAI interface

The LS1012A SAI (Serial Audio Interface) can be used to support either I2S 2-channel audio or TDM-style multi-channel audio.

The LS1012ARDB supports full duplex SAI2 port through the Ardiuno connector (J17). SAI2 port supports both a Tx and a Rx interfaces at an instance.

The SAI Audio blocks can be clocked with the internal system clock. If a precise frequency of operation is required other than this, then the external SAI clocks (TXCLK or RXCLK) can be configured to be inputs to the system.

The SAI interface on the LS1012ARDB is muxed with RGMII. For details, see RGMII port.

2.10 USB interface

The LS1012ARDB supports one SuperSpeed USB 2.0/3.0 port. The USB port is configured as On-The-Go (OTG) with a Micro-AB connector. The following figure shows the USB 2.0/3.0 PHY controller architecture.

Based on the OTG configuration, the PHY can either operate in Type-A or Type-B mode.

In type A mode:
- Board is powered from the 12 V external power supply or the 5 V PoE controlled and monitored through the power switch U15 (MAX1558H). Jumper should be mounted on J25 connector's 2-3.
- For battery powered mode, SW1[6] enables LTC4155 to enable the OTG boost regulator on USB1 DRVVBUS assertion, to generate 5 V power supply. Jumper should be mounted on J25 connector's 1-2.

In type B mode:

- U15 should always be in disabled state as the USB1 DRVBUS will be always de-asserted.
- If powered by external 12 V/ PoE, the board is not powered from the USB 5 V power rail. Jumper should be mounted on J25 connector's 2-3.
- If in battery backed USB powered mode, LTC4155 powers the board. Jumper should be mounted on J25 connector's 1-2.
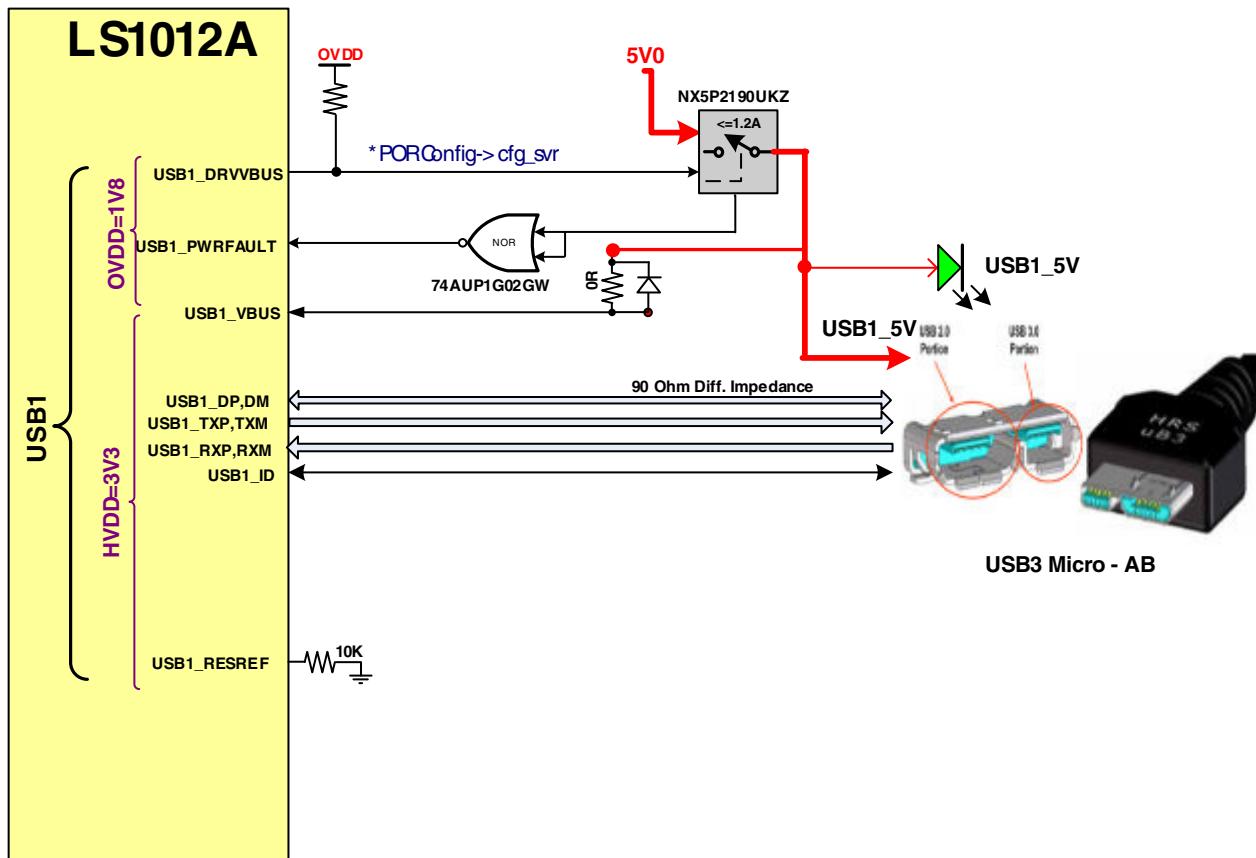
Figure 2-8. USB 2.0/3.0 PHY architecture

2.11   I2C ports

The LS1012ARDB support one I2C bus:

- The LS1012A I2C1 is attached to all local devices on the LS1012ARDB.
- The level shifter device (NTSX2102GU8H) is used on the LS1012ARDB I2C1 bus, to convert the LS1012A 1.8 V to 3.3 V signals for the I2C devices.
- The I2C1 bus has three possible masters, LS1012A processor, KW41, and remote access (external off-board connection).

The LS1012ARDB I2C connection scheme is shown in the following figure.
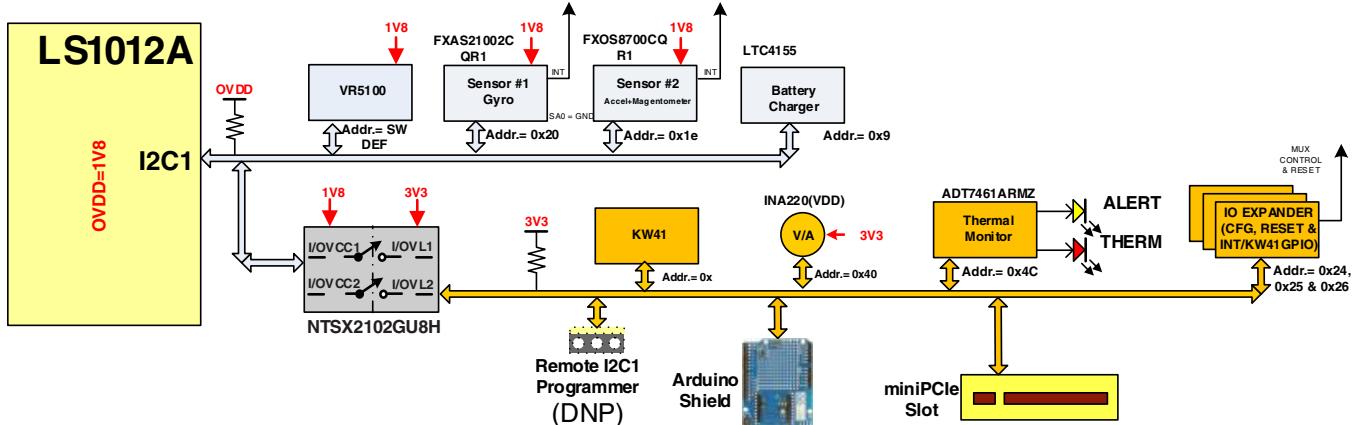
Figure 2-9. I2C

2.11.1 I²C devices and addresses

The LS1012A I2C1 interface operates at 1.8 V OVDD power supply. Table 2-13 summarizes the I2C bus device addresses.

NOTE
7-bit addresses do not include the R/W bit as an address member, though some datasheets might do so. For consistency, all I2C addresses are 7 bits of addresses only.

Table 2-13. I2C bus device map

I2C bus	I2C address	Device	Notes
I2C1	Software defined	Kinetis 32-bit MCU - NXP MKW41Z512VHT4	• Wireless MCU
	0x20	3-Axis Digital Angular Rate Gyroscope - NXP FXAS21002CQR1	• Used for measuring angular rates up to ±2000°/s, with output data rates (ODR) from 12.5 to 800 Hz.
	0x1e	6-Axis Sensor with Integrated Linear Accelerometer and Magnetometer - NXP FXOS8700CQR1	• Used to provide dynamically selectable acceleration full scale ranges of ±2 g/±4 g/±8 g and a fixed magnetic measurement range of ±1200 µT.
	0x9	3.6 V - 4.2 V Li-Ion/Li-Poly batteries - LTC4155	• Used to power the board in battery-backed USB powered mode.
	0X08	Voltage regulator - NXP MC34VR5100A1EP	Provides power supply for: • LS1012A power supplies • DDR3L memory • 1.8 V general I/O voltage for QSPI memories, SD Card, SD Wifi IO, eMMC
	n/a	Arduino Shield	• Provides support for Ardiuno and Freedom shield expansion

Table continues on the next page...

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Table 2-13.   I2C bus device map (continued)

I2C bus	I2C address	Device	Notes
	0x40	VDD current measurement - INA220	• Used for current/power measurements on LS1012A VDD/Core voltage.
		miniPCIe Slot - CONN PCI EXP 52	• Supports PCIe Gen1/2 add-in cards
	0x24, 0x25, 0x26	IO expander (CFG, RESET, and INT/ KW41GPIO) - NXP PCAL9555AHF	• Provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion for the I2C bus

2.12   QSPI interface

The LS1012RDB supports QSPI as the primary system boot source. The LS1012RDB features are as follows

- Onboard QSPI flash for boot image with a virtual bank support
- Off-board QSPI emulation support

LS1012A supports only one QSPI controller with 1 chip select. The RDB doesn't support the quad mode, only single and dual bit modes are supported. The following figure shows the QSPI interface on the LS1012RDB.
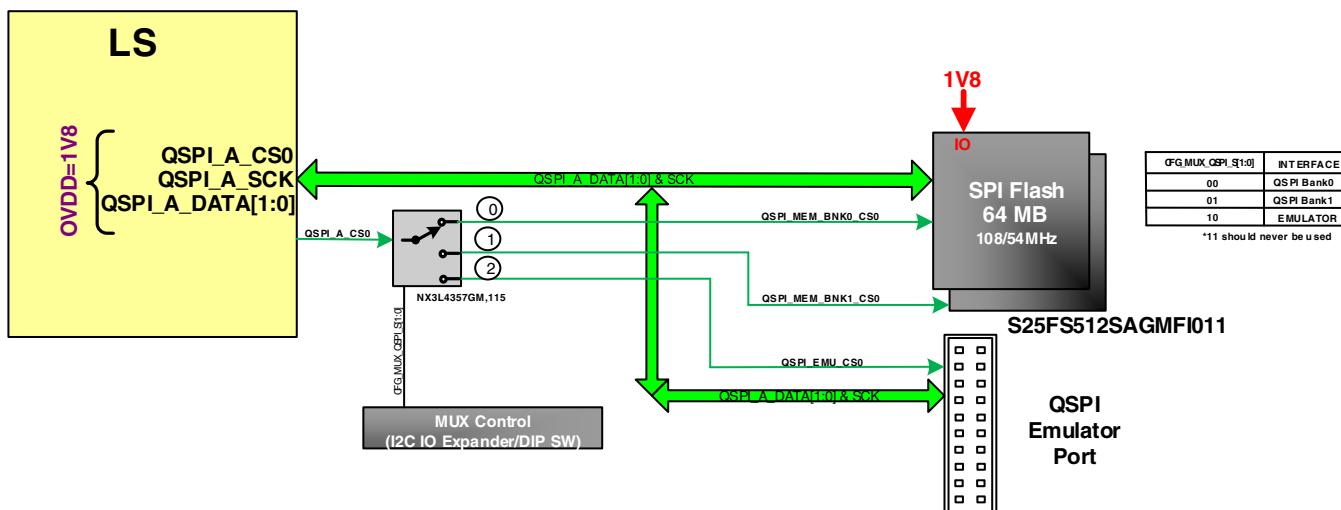

Figure 2-10. QSPI interface

2.12.1   QSPI NOR flash memory

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The LS1012ARDB supports onboard Spansion S25FS512SAGMFI011 quad-SPI serial flash memory with 64 MB space. There are two virtual banks on the RDB that can be selected through CFG_MUX_QSPI_S[1:0]. See Table 2-14 for more details.

2.12.2   QSPI NOR emulator

The LS1012ARDB supports the use of external QSPI NOR programmers or emulators using a 20-pin 0.05" pitch header, SamTec TFM-110-02-S-D-SN-K-TR or equivalent. The pinout is shown in the following figure.

(key)	1	2	CS_B
RESET_B	3	4	CS1_B
GND	5	6	IO Voltage
CLK	7	8	DQ2
DQ3	9	10	DQ1
	11	12	DQ0
	13	14	
	15	16	
	17	18	
	19	20	

Figure 2-11. QSPI emulator header

This header may be used with the DediProg EM100PISP emulator with Intel ISP adapter-B.

2.12.3   QSPI device mapping

A dual 1:3 switch, NX3L4357GM,115 (U35) drives the QSPI chip-select signals to QSPI NOR flash memory (2 virtual banks) or the QSPI emulator. The mux/demux devices are controlled by onboard DIP switch and IO expander.

The following table shows the LS1012ARDB QSPI device mapping.

NOTE
- Only QSPI can be used as RCW/PBI source.
- The POR config is muxed on QSPI_DATA0.

Table 2-14.   LS1012ARDB QSPI device mapping

CFG_MUX_QSPI_S[1:0]	Controlled by	Interface
00	SW2[8:7] I2C IO expander - IO1_1, IO1_0	Bank 1 of 64 MB QSPI NOR flash memory - S25FS512SAGMFI011 (U37)
01		Bank 2 of 64 MB QSPI NOR flash memory - S25FS512SAGMFI011 (U81)
10		QSPI emulator - TFM-110-02-S-D-SN-K-TR (J8)
11		Do not use (causes bus contention)

2.13   SDHC interface

The LS1012ARDB supports two eSDHC controllers, eSDHC1 and eSDHC2. The eSDHC controllers support a large variety of devices, both in terms of width as well as the ability to use special signals to accelerate data transfer.

The following figure shows the overall connections of the SDHC portion.
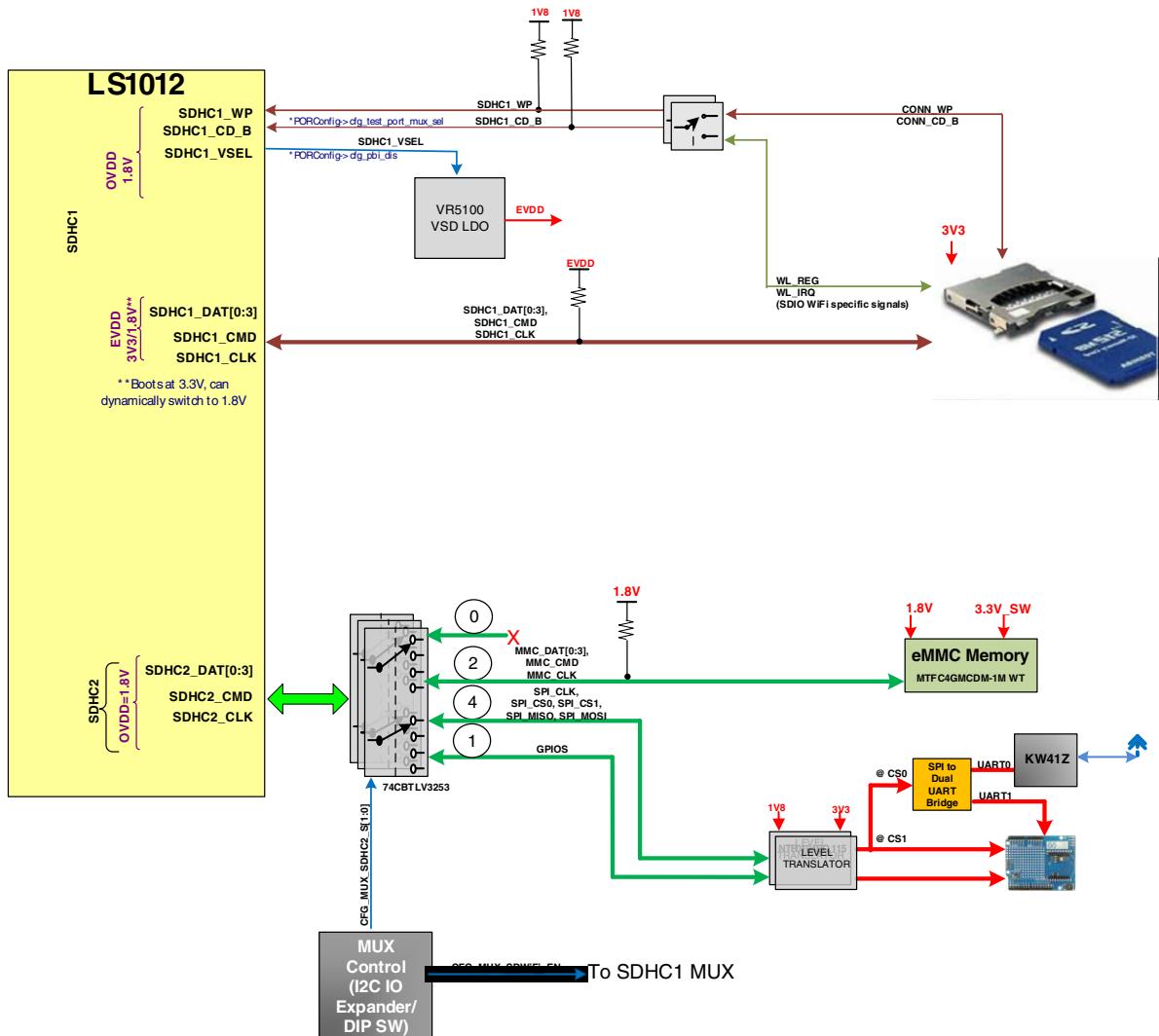
Figure 2-12. SDHC architecture

2.13.1 SDHC1 interface

The LS1012A SDHC1 controller is connected to the onboard SDHC connector. SD cards and MMC memories (using SD-MMC adapter) can be used on this connector. The connector also provides write protect and card detect mechanical switches.

In addition, the onboard power regulator, VR5100 VSD (U7), provides power switch control from 3.3 V to 1.8 V for the EVDD power supply of LS1012A SDHC1 IOs. The following table shows how the power provided to the SDHC devices is controlled.

Table 2-15. SDHC memory power control

Configuration Signals	Value	Description
SDHC1_VSEL	0	3.3 V (Default)
	1	1.8 V (After SDHC_VSEL check)

2.13.1.1 Using SD WiFi card with LS1012ARDB

The latest revisions of LS1012ARDB (revision D and above) contain SD Wifi card as a part of the board kit. The SD WiFi card is used to enable SDHC based WiFi using Murata SN8000 module.

The SDIO WiFi component on the board (SN8000 from Murata) can support WiFi 802.15a/b/g. The SDIO interface for the device can support maximum speed up to 52 MHz.

Antenna details for the Murrata WiFi module:
- Part no: W1049B050
- Manufacturer: Pulse

NOTE
For more details about Murrata WiFi module antenna, see Data sheet.

To use the SD WiFi card:
1. Insert the SD WiFi card into the SD connector. The opening for SD connector is at the front side of chassis as shown in Figure 1-2.
2. Insert the SD WiFi card as shown in the figure below.

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Figure 2-13. SD WiFi card

NOTE
SD connectors in rev D is different from prior revisions.
The card orientation while insertion is also different.

3. The SD WiFi card provides access to the co-existence signals through a jumper.

Pin Number	Co-existence Signals
J2.1	BTCX_TXCONF
J2.2	BTCX_STATUS
J2.3	BTCX_RF_ACTIVE
J2.4	GND

2.13.2   SDHC2 interface

Three dual 1:4 mux/demux devices, 74CBTLV3253DS (U30, U31, U33) drive the SDHC2 signals to eMMC, SDIO WiFi, SPI, and Ardiuno shield.

The following table shows the LS1012ARDB SDHC2 device mapping.

Table 2-16. LS1012ARDB SDHC device mapping

CFG_MUX_SDHC2_S[1:0]	Controlled by	Interface
00	IO expander - IO0_3, IO0_2	No device
01	DIP switch - SW2 [2:1]	GPIO (To Arduino)
10		eMMC Memory
11		SPI

The 512 MB eMMC memory used on RDB can support speed up to HS200.

2.14 SPI interface

Refer Figure 2-12 for the SPI interface architecture on the LS1012ARDB.

The LS1012ARDB SPI features are as follows:

- SPI bus interface is connected to a dual-channel high performance UART that can connect to the KW41Z MCU and the Ardiuno shield.
- The same port can also be used to communicate with the KW41Z microcontroller for BLE support and for reading ADC data of the sensors on the Arduino connector.
- LS1012A SPI bus is muxed with LS1012A SDHC1 IOs. Muxes are used on the board to select between the available options.

The following table describes the SPI devices used on the LS1012ARDB.

Table 2-17. SPI master mode onboard memories

Device	Maximum clock frequency (MHz)	Voltage range	Capacity	SPI CS
KW41Z	TBD	3.3 V	TBD	SPI_CS0
Ardiuno Shield		3.3 V		SPI_CS1

2.15 UART serial ports

The following table shows the LS1012ARDB UART connections.
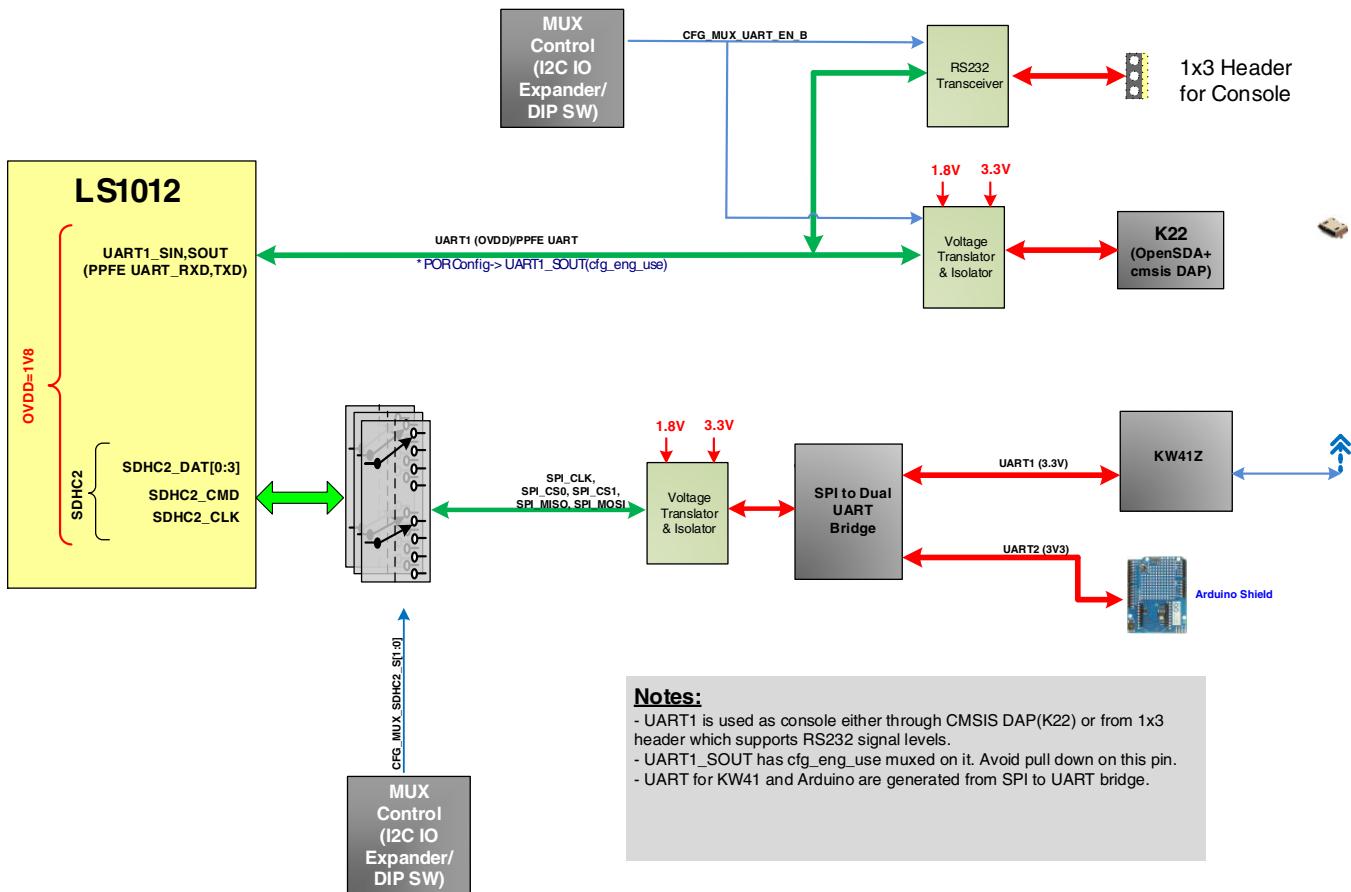
Figure 2-14. UART architecture

The LS1012A processor consists of two UART controllers, out of which only UART1 is used on RDB.

The UART1 port of LS1012A can be used to provide debug console through K22 microcontroller or through a RS232 1x3 header. The UART1 connection is configured through CFG_UART_MUX_EN_B controlled from SW1[7] and IO0_0 [1]. See Switch configuration and I2C mux select IO-expander for switch and IO expander details.

Table 2-18. UART connections

CFG_UART_MUX_EN_B	Controlled by	Description
1'b0	IO expander - IO0_0 DIP switch - SW2 [7]	LS1012A UART1 is connected to K22 UART0.
1'b1		LS1012A UART1 connects to LTC2801, which provides RS232 level TX-RX on 1x3 header (J24).

2.16 Ardiuno

The LS1012ARDB supports a Freedom board or an Ardiuno shield on connectors J16 to J20 to provide broad range of board expansion options.

Arduino supports following interfaces:
- SPI connectivity from LS1012A on CS1.
- UART connectivity through LS1012A SPI to UART bridge.
- I2C connectivity from KW41 and LS1012A.
- Audiuno half duplex support through LS1012A SAI2 interface.
- Analog sensor outputs for KW41 ADC.

2.17 MKW41Z512VHT4 MCU

The MKW41Z SoC is an ultra low-power, highly integrated single-chip device that enables Bluetooth Low Energy (BLE) or IEEE® Std. 802.15.4/ZigBee RF connectivity for portable, extremely low-power embedded systems. The MKW41Z SoC family integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range supporting a range of FSK/GFSK and O-QPSK modulations, and ARM Cortex®- M0+ CPU, 160 KB flash memory and 20 KB SRAM, BLE Link Layer hardware, 802.15.4 packet processor hardware and peripherals optimized to meet the requirements of the target applications. The following figure shows the KW41Z architecture on the LS1012ARDB.

KW41 & K22
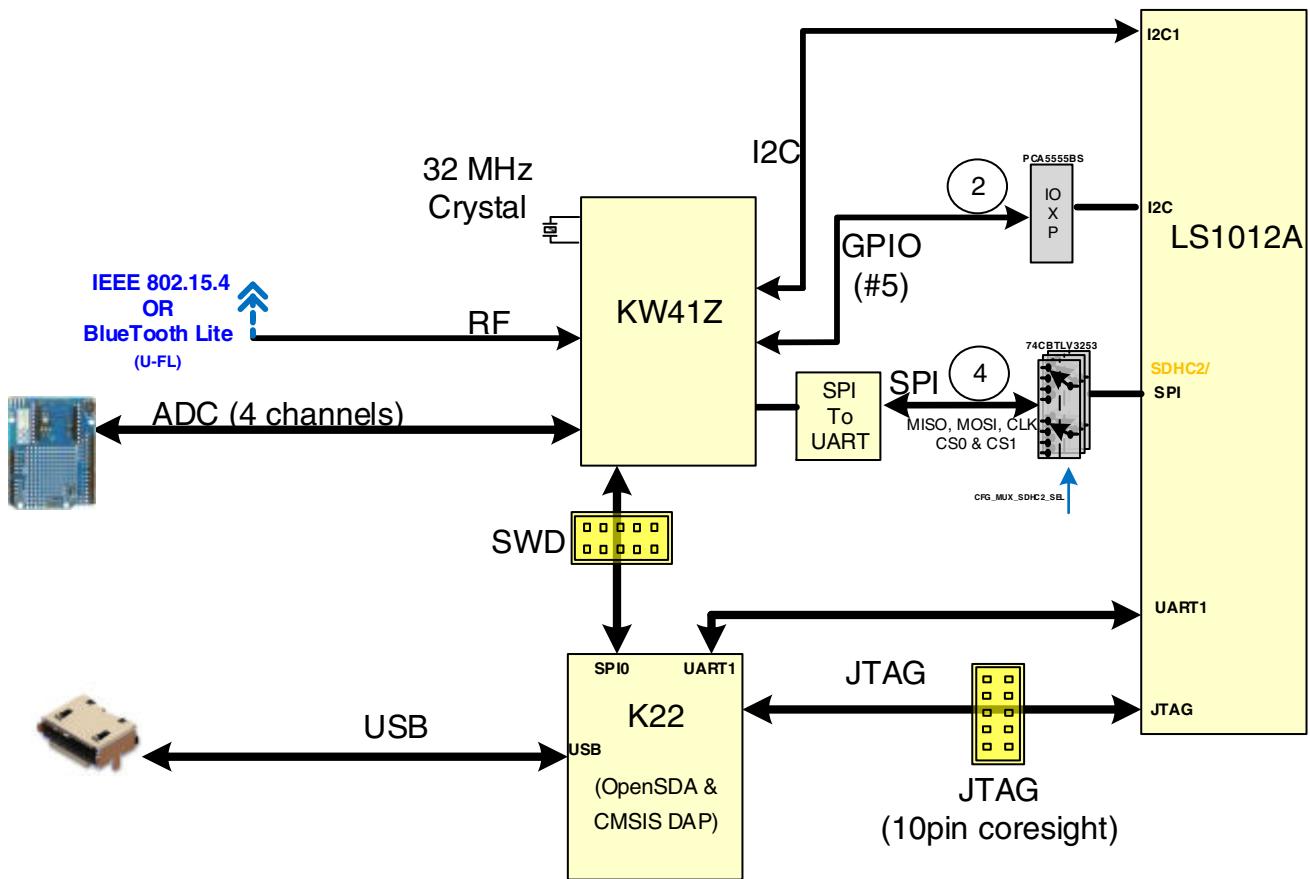
Figure 2-15. MKW41Z512VHT4 MCU

KW41 supports following interfaces:
- I2C bus to all the devices on the board. See I^{2}C devices and addresses for details.
- UART to provide connectivity from LS1012A through a SPI to UART bridge.
- ADC inputs for analog sensor inputs from Arduino connectors.
- SWD interface for debug from CMSIS DAP or external SWD debugger.
- Antenna interface for BLE and Zigbee IEEE 802.15.4. The antenna part number is W24-ASMA-M. For datasheet, see http://www.inventeksys.com/wp-content/uploads/ W24-SSMA_Functional_Spec-200031-1.2.pdf

2.18   JTAG port

The LS1012ARDB consists of the LS1012A SoC and KW41 and K22 microcontrollers, each of which have dedicated debug connectors.
- J15 SWD connectors can be used by an external SWD debugger to debug KW41.

- J11 and J12 can be used by external debuggers, such as CWTAP, DSTREAM to debug LS1012A and K22 respectively
- Apart from the JTAG connectors, K22 MCU can be used as a CMSIS DAP on the LS1012ARDB. The CMSIS DAP provides low speed debug functionality for the LS1012A SoC.

2.18.1   CMSIS-DAP

This section describes the MBED circuit on the LS1012ARDB. MBED is an open standard serial and debug adapter. It bridges serial and debug communications between a USB host and an embedded target processor, as shown in the figure below.
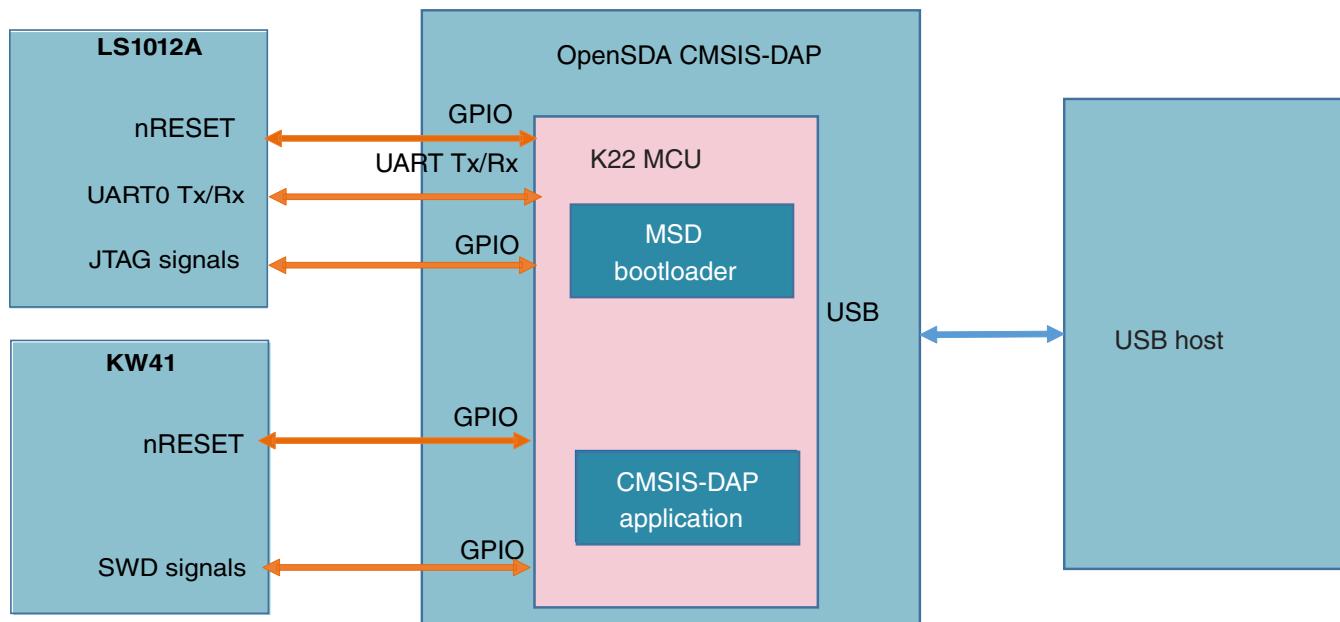
Figure 2-16. CMSIS-DAP

CMSIS-DAP is managed by a Kinetis K22 MCU built on the ARM Cortex-M4 core. The Kinetis K22 includes an integrated USB controller that can operate at clock rates of up to 120 MHz. The CMSIS-DAP circuit includes a status LED. In addition, signal connections are available to implement a UART serial channel.

CMSIS-DAP features a mass storage device (MSD) bootloader, which provides a quick and easy mechanism for loading different CMSIS-DAP applications, such as flash programmers, run control debug interfaces, serial-to-USB converters, and so on.

NOTE
Only LS1012A debug is supported from CMSIS DAP. KW41 can be debugged only from the JTAG connector, J15.

2.19 GPIO pins

LS1012A has no dedicated GPIO pins; instead, GPIO functions are multiplexed internally on other signals, which must be enabled either through RCW word or dynamically through registers in LS1012A. Additionally LS1012A provides GPIOs through Interrupt and GPIO IO-expander (0x26).

Table 2-19. LS1012ARDB - GPIO mapping

Primary function	GPIO function	Connections on RDB
KW41 PTA16	KW41_GPIO_1	Connects to KW41 through Interrupt and GPIO IO-expander (U88)
KW41 PTA17	KW41_GPIO_2	Connects to KW41 through Interrupt and GPIO IO-expander (U88)
KW41 PTA18	KW41_GPIO_3	Connects to KW41 through Interrupt and GPIO IO-expander (U88)
KW41 PTA19	KW41_GPIO_4	Connects to KW41 through Interrupt and GPIO IO-expander (U88)
KW41 PTB0	KW41_GPIO_5	Connects to KW41 through Interrupt and GPIO IO-expander (U88)
LS1012A SDHC2_CLK	GPIO_1[24]	Connects LS1012A to Arduino through 1.8 V to 3.3 V translators
LS1012A SDHC2_DAT0	GPIO_1[25]	Connects LS1012A to Arduino through 1.8 V to 3.3 V translators
LS1012A SDHC2_DAT1	GPIO_1[26]	Connects LS1012A to Arduino through 1.8 V to 3.3 V translators
LS1012A SDHC2_DAT2	GPIO_1[27]	Connects LS1012A to Arduino through 1.8 V to 3.3 V translators
LS1012A SDHC2_DAT3	GPIO_1[28]	Connects LS1012A to Arduino through 1.8 V to 3.3 V translators
LS1012A SDHC2_CMD	GPIO_1[29]	Connects LS1012A to Arduino through 1.8 V to 3.3 V translators

2.20 Temperature

LS1012A has an on-die TMU module that can be used for temperature measurements. LS1012A also has a thermal diode on the die, which allows direct temperature measurement. The internal temperature monitor in LS1012A is used for reading the die temperature, and trigger software interrupts upon thermal over-temperature conditions. These temperature warnings and alarm signals can be used by software running on LS1012A to reduce the power dissipation and protect DUT from over-temperature failure.

NOTE

ADT7461 circuitry is not mounted, by default, on the LS1012ARDB.

Chapter 3
Board Configuration and Debug Support

3.1 Introduction

This chapter explains the steps you need to perform to configure the LS1012ARDB. You can use switches and IO expanders available in a board to set up the board.

3.2 Switch configuration

The LS1012ARDB consists of the switches to allow easy configuration of various features required by the software developers. The following table explains the switches available in the LS1012ARDB.

Table 3-1. Switch configuration

Switch	Option	Description
SW1 [1]	SW_RCW_SRC1	0 - Hard coded source 3 (Reserved)
		1 - QSPI is the RCW source (default)
SW1 [2]	SW_ENG_USE	XOSC Transconductance Multiplier
SW1 [3]	SW_ENG_USE2	**{SW_ENG_USE2, SW_ENG_USE}**

SW1 [3]	SW1 [2]	Values
0	0	0.21x
0	1	0.55x
1	0	0.66x
1	1	1.00x (default)

Switch	Option	Description
SW1[4]	Reserved	Default value is 0
SW1[5]	BATT_POW_EN_B	Enable Battery backed USB powered use case
		0 - Power for RDB sourced only from 12V based regulator (default)

Table continues on the next page...

Table 3-1. Switch configuration (continued)

Switch	Option	Description
		1 - Power for RDB is sourced from USB port/Battery if 12V is removed.
SW1 [6]	BATT_OTG_BST_EN_B	OTG 5 V VBUS enable 0 - USB1 DRVVBUS enables the VBUS boost regulator of LTC4155 1 - Disable VBUS Boost regulator of LTC4155 (default)
SW1 [7]	CFG_UART_MUX_EN_B	0- LS1012A UART1 is connected to K22 UART0 for CMSIS DAP debug. (default) 1 - LS1012A UART1 is translated to RS232 levels and is available on 1x3 header (J24).
SW1 [8]	CFG_SERDES_MUX_SEL	SERDES Lane A MUX selection 0 - SGMII 1G to PHY (default) 1 - PCIe TX clock to mini PCIe connector
SW2 [1]	CFG_MUX_SDHC2_S0	SDHC 2 interface demultiplexer select lines
SW2 [2]	CFG_MUX_SDHC2_S1	**CFG_MUX_SDHC2_S[1:0]**

SW2 [2]	SW2 [1]	Values
0	0	No device
0	1	GPIO (to Arduino)
1	0	eMMC Memory
1	1	SPI

Switch	Option	Description
SW2[3]	CFG_MUX_SD_CD_EN_B	Enable OOB IRQ on SDHC1_CD only when SD WiFi card is used. CD functionality is unavailable when OOB IRQ is enabled and SD WiFi card is used on SDHC1 J9 connector. 0 - SDHC1 CD is always enabled (Default) 1 - GPIO1[21] shall be used as OOB IRQ Trigger from the SD WiFi card. For other cards, CD functionality can be enabled.
SW2 [6]	CFG_RGMII_MUX_EN_B	RGMII interface demultiplexer select 0 -> RGMII enabled (default) 1 -> SAI2 enabled (through Arduino)
SW2 [7]	CFG_MUX_QSPI_S0	QSPI chip-select demultiplexer select
SW2 [8]	CFG_MUX_QSPI_S1	**CFG_MUX_QSPI_S[1:0]**

SW2 [8]	SW2 [7]	Values
0	0	CS routed to SPI memory bank 1 (default)
0	1	CS routed to SPI memory bank 2

Table 3-1. Switch configuration

Switch	Option	Description		
		SW2 [8]	**SW2 [7]**	**Values**
		1	0	CS routed to Emulator
		1	1	Invalid (Never use this option, as it causes bus contention)

3.3 I2C IO expanders

The LS1012ARDB consists of two I2C IO expanders, MUXSEL and Reset.

3.3.1 I2C mux select IO-expander

The I2C IO-expander for mux select s used to control the muxing of various onboard interfaces. Default power-on configurations are set from the DIP switch SW1 and SW2. The IO expander can be used to override the values on the demultiplexer select lines. The part number of the I2C mux select expander used on the LS1012ARDB is PCAL9555AHF (U73) and I2C address of the expander is 0x24. The following table explains the mapping of the I2C expander pins with the signals.

Table 3-2. I2C expander for mux - fields

Pins	Signal	Description
IO0_0	CFG_UART_MUX_EN_B	0 - LS1012A UART 1 is connected to CMSIS DAP (K22)
		1 - LS1012A UART 0 is connected to 1x3 header through a RS232 transceiver.
IO0_1	CFG_SERDES_MUX_SEL	SERDES Lane A MUX selection
		0 - SGMII 1G to PHY
		1 - PCIe TX clock to mini PCIe connector
IO0_2	CFG_MUX_SDHC2_S0	SDHC 2 interface demultiplexer select lines
IO0_3	CFG_MUX_SDHC2_S1	**CFG_MUX_SDHC2_S[1:0]**

Table continues on the next page...

Table 3-2.   I2C expander for mux - fields (continued)

Pins	Signal	Description		
		SW2 [2]	**SW2 [1]**	**Values**
		0	0	No device
		0	1	GPIO (to Arduino)
		1	0	eMMC Memory
		1	1	SPI
IO0_4	Reserved			
IO0_5	Reserved			
IO0_6	Reserved			
IO0_7	CFG_RGMII_MUX_EN_B	RGMII interface demultiplexer select 0 - RGMII enabled 1 - SAI 2 enabled (through Arduino)		
IO1_0	CFG_MUX_QSPI_S0	QSPI chip-select demultiplexer select		
IO1_1	CFG_MUX_QSPI_S1	**CFG_MUX_QSPI_S[1:0]**		
		SW2 [8]	**SW2 [7]**	**Values**
		0	0	CS routed to SPI memory bank 1 (default)
		0	1	CS routed to SPI memory bank 2
		1	0	CS routed to Emulator
		1	1	Invalid (Never use this option, as it causes bus contention)
IO1_2	Reserved			
IO1_3	These fields can be inverted and used for revision info. BRD_REV_B[4:0] b11101- Rev C			
IO1_4	b11111 - Rev A			
IO1_5	b11110 - Rev B			
IO1_6	b11101- Rev C			
IO1_7	b11100 - Rev C1			
	b11011- Rev C2			

Table 3-2.   I2C expander for mux - fields

Pins	Signal	Description
	b11010 - Rev D	

3.3.2   I2C reset IO-expander

The I2C IO-expander for reset is used to reset the onboard interfaces. The part number of the I2C reset expander used on the LS1012ARDB is PCAL9555AHF (U74) and I2C address of the expander is 0x25. The following table explains the mapping of the I2C expander pins with the signals.

Table 3-3.   I2C expander for mux - fields

Pins	Signal	Description
IO0_0	IOXP_RST_DDR3L_B	Resets the DDR3L interface
IO0_1	IOXP_RST_ETH1_B	Resets ETH1 interface
IO0_2	IOXP_RST_ETH2_B	Resets ETH2 interface
IO0_3	IOXP_RST_GYRO_B	Resets Gyroscope
IO0_4	IOXP_RST_ACCEL_B	Resets Accelerometer
IO0_6	IOXP_RST_eMMC_B	Resets the eMMC memory
IO0_7	IOXP_RST_QSPI_EMU_B	Resets QSPI emulator
IO1_0	IOXP_RST_QSPI_MEM_B	Resets NOR flash memory
IO1_1	IOXP_RST_PCIE1_B	Resets mini PCIe
IO1_2	IOXP_RST_ARD_B	Resets Ardiuno shield
IO1_3	IOXP_RST_KW40_B	Resets KW41

3.3.3   I2C interrupt and GPIO IO-expander

The I2C IO-expander for interrupt and GPIO is used to generate interrupt signals and provide GPIO pons for KW41. The part number of the I2C reset expander used on the LS1012ARDB board is PCAL9555AHF (U88) and I2C address of the expander is 0x26. The following table explains the mapping of the I2C expander pins with the signals.

Table 3-4. I2C expander for interrupt and GPIO - fields

Pins	Signal	Description
IO0_0	KW41_GPIO_1	Provides GPIO to KW41
IO0_1	KW41_GPIO_2	Provides GPIO to KW41
IO0_2	KW41_GPIO_3	Provides GPIO to KW41
IO0_3	KW41_GPIO_4	Provides GPIO to KW41
IO0_4	KW41_GPIO_5	Provides GPIO to KW41
IO0_5	Reserved	
IO0_6	ARD_PC9	Provides GPIO connection to Arduino connector J16.4 pin.
IO0_7	ARD_PC10	Provides GPIO connection to Arduino connector J17.8 pin.
IO1_0	Reserved	
IO1_1	Reserved	
IO1_2	Reserved	
IO1_3	BRDG_IRQ_B	IRQ signal from SPI to dual UART bridge
IO1_4	THERM_FAULT_B	Indicates thermal fault interrupt
IO1_5	INT_ACCEL_B	Initiates Accelerometer
IO1_6	INT_GYRO_B	Initiates Gyroscope
IO1_7	IRQ_ETH_B	IRQ signal from the Ethernet interfaces
INT	IRQ_IOXP_B	Generates IRQ signal to LS1012A through the GPIO_1[13] (on LS1012A QSPI DATA[2])

3.4 Power-monitoring LEDs

The board includes LEDs for power or reset monitoring, which inform the user about the status of different power rails, resets, and board faults. The LS1012ARDB LEDs are listed in the following table.

Table 3-5. LS1012ARDB LEDs

LED legend	Description (when LED is ON)	Reference designator	LED color
12V ON	Indicates 12 V PS ready status	D4	Green
3.3V ON	Indicates 3.3 V PS ready status	D19	Green
USB VBUS ON	Indicates that USB 5 V power is available on the connector	D20	Green
SDA_LED	Indicates SDA (K22) is active	D22	Green
PORST	DUT is in reset (POREST is asserted)	D24	Red

Appendix A
LS1012ARDB drawings

This section explains:

- LS1012ARDB top-side view
- LS1012ARDB bottom-side view

A.1 LS1012ARDB top-side view

NOTE

For a clear view of the board top-side view, please zoom-in on the Figure.
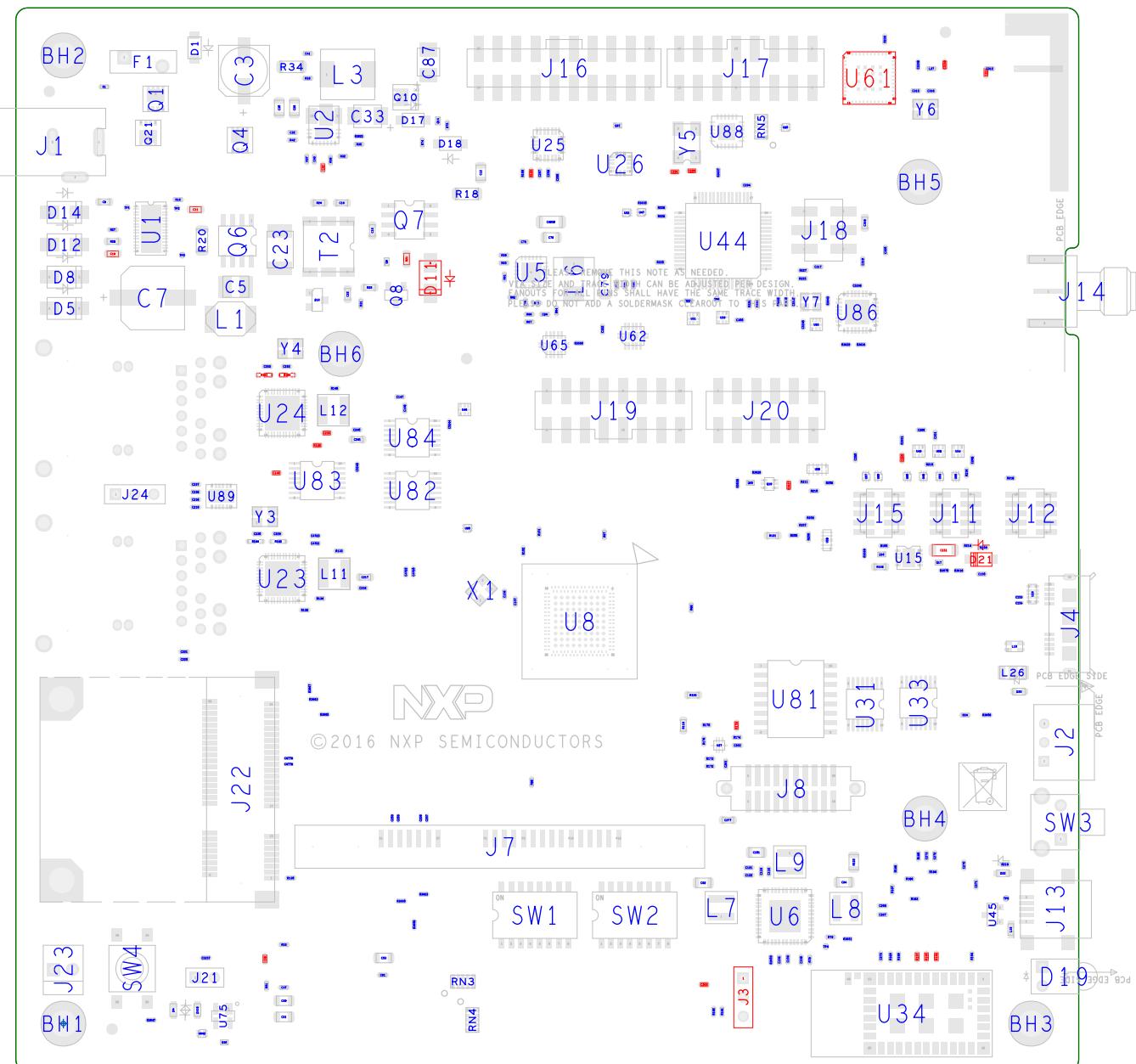
Figure A-1. LS1012ARDB top-side view

A.2   LS1012ARDB bottom-side view

> **NOTE**
>
> For a clear view of the board bottom-side view, please zoom-in on the Figure.
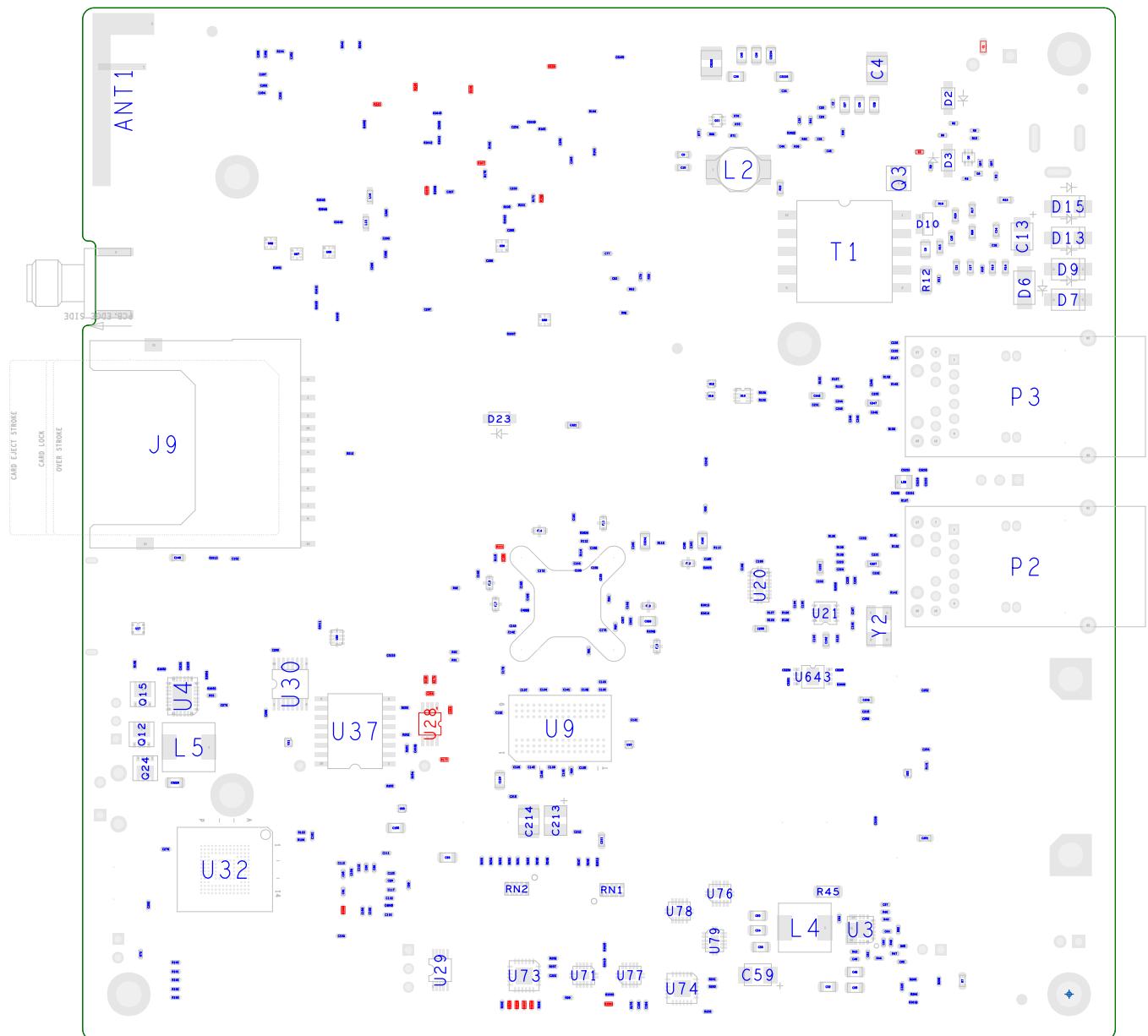
Figure A-2. LS1012ARDB bottom-side view

Appendix B
Revision history

This sections summarizes revisions to this document.

Table B-1. Revision history

Revision	Date	Section	Description
0	06/2016		Initial public release.
1	08/2016	Double data rate (DDR) memory	Updated block diagram
		SGMII port	Updated block diagram
		RGMII port	Updated block diagram
		UART serial ports	Updated block diagram
2	08/2016	LS1012ARDB features Double data rate (DDR) memory QSPI interface QSPI NOR flash memory QSPI device mapping	Updated DDR and QSPI memory sizes to bytes instead of bits.
3	01/2017	Introduction	• Added information about SDIO based WiFi card that is available in Rev D and onwards board kits. • Mentioned about ASK
		LS1012ARDB features	• Removed note: "KW41 is not populated in the current revision of the board, it will available in future revisions." • In Table 1-3 : • Removed "SDIO WiFi" from SDHC2 features. • Updated Clocks row
		LS1012ARDB block diagrams	• Removed note: "KW41 is not populated in the current revision of the board, it will available in future revisions." • Updated Figure 1-1
		LS1012ARDB interface	• Added Figure 1-2 and Figure 1-3 • Updated Figure 1-4 and Figure 1-5
		Power supplies	• Updated Figure 2-1
		Primary power supply	• Added details about "DIP switch SW1[5]"

Table continues on the next page...

Revision	Date	Section	Description
		Power-ON	
		Clocks	• Updated Table 2-7
		SGMII port	• Updated Table 2-11 • Updated Figure 2-6
		RGMII port	• Updated Table 2-12 • Updated Figure 2-7
		USB interface	• Updated the section
		I^{2}C devices and addresses	• Updated "NXP PCA9555" to "NXP PCAL9555AHF"
		SDHC interface	• Updated Figure 2-12 • Added new section, SD Wifi card • Updated Table 2-16
		CMSIS-DAP	• Added note "Only LS1012A debug is supported from CMSIS DAP. KW41 can be debugged only from the JTAG connector, J15."
		Switch configuration	• Updated for Rev D board
		I2C IO expanders	• Updated part no of I2C mux select expander to "PCAL9555AHF" • Updated Table 3-2 • Updated part number of the I2C reset expander to "PCAL9555AHF" • Updated Table 3-3 • Updated par t number of the I2C reset expander to "PCAL9555AHF" • Updated I2C interrupt and GPIO IO-expander
		Using SD WiFi card with LS1012ARDB	• Added new section

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