MPQ4470/4470A

High-Efficiency, Fast-Transient, 5A, 36V Synchronous, Step-Down Converter AEC-Q100 Qualified

The Future of Analog IC Technology®

DESCRIPTION

The MPQ4470/4470A is a fully-integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. It offers a very compact solution to achieve a 5A, continuous-output current over a wide input-supply range with excellent load and line regulation. It also provides fast transient response and good stability for wide input-supply and load range. The MPQ4470/4470A operates at high efficiency over a wide output current load range.

MPQ4470 has full protection features include SCP, OCP, OVP latch, UVP, and thermal shutdown. MPQ4470A has the same protection features to MPQ4470 except has no OVP latch function.

The MPQ4470/4470A requires a minimal number of readily-available, standard, external components, and is available in a space-saving 3mm×4mm, 20-pin, QFN package.

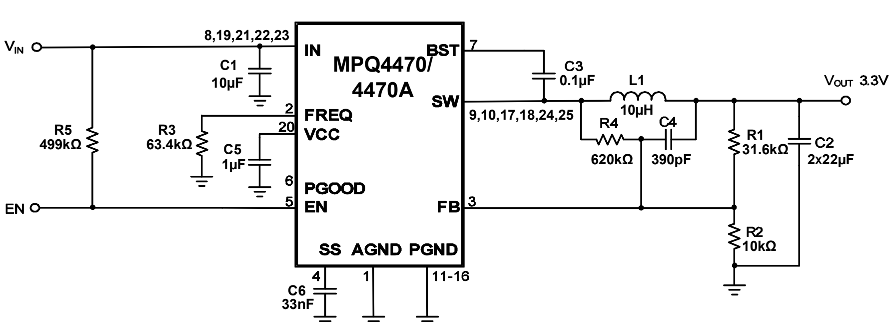
FEATURES

- Wide 4.5V-to-36V Operating Input Range
- Guaranteed 5A, Continuous Output Current
- Internal 40mΩ High-Side, 20mΩ Low-Side Power MOSFETs
- Proprietary Switching-Loss-Reduction Technology
- 1% Reference Voltage
- Programmable Soft-Start Time
- Low Drop-out Mode
- 100kHz-to-1MHz Switching Frequency
- SCP, OCP, OVP Latch (MPQ4470 only), UVP, and Thermal Shutdown
- Output Adjustable from 0.8V to 0.9×V_{IN}
- Available in a 3mm×4mm 20-pin QFN Package
- Available in AEC-Q100 Grade 1

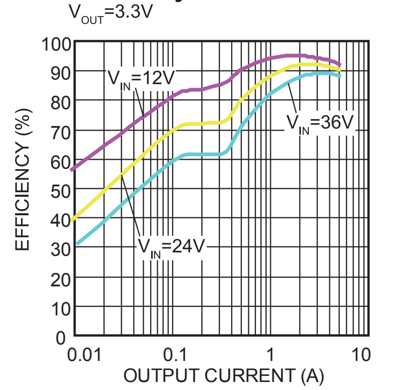
APPLICATIONS

- Notebook Systems and I/O Power
- Automotive Systems
- Networking Systems
- Industrial Supplies
- Optical Communications Systems
- Distributed Power and POL Systems

TYPICAL APPLICATION



Efficiency vs. Load Current
V_{OUT}=3.3V

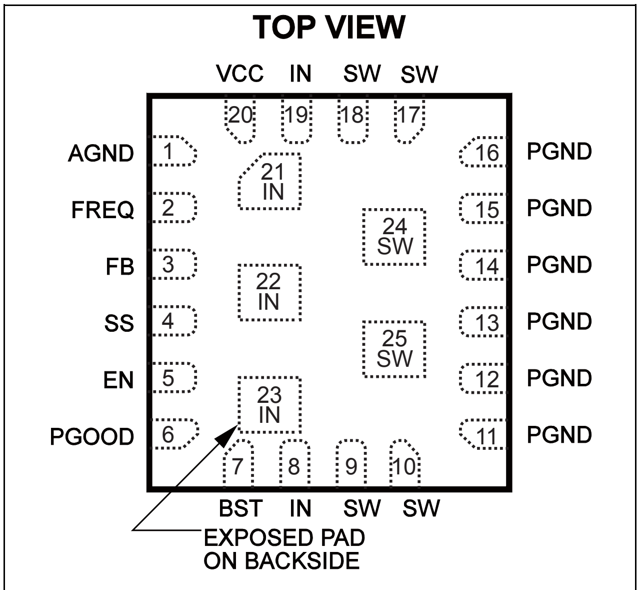


ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ4470GL	QFN20 (3mm×4mm)	4470
MPQ4470AGL	QFN20 (3mm×4mm)	4470A
MPQ4470GL-AEC1	QFN20 (3mm×4mm)	4470
MPQ4470AGL-AEC1	QFN20 (3mm×4mm)	4470A

* For Tape & Reel, add suffix –Z (e.g. MPQ4470/4470AGL–Z)

PACKAGE REFERENCE



QFN20 (3mm×4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 40V
V_{SW} ....-0.3V to V_{IN} + 0.3V
V_{BST} ....V_{SW} + 6V
V_{PGOOD}....................................-0.3V to V_{CC}+0.6V
All Other Pins................................. -0.3V to +6V
EN Sink Current.......................................150µA
Continuous Power Dissipation (T_A = +25°C) (2)
…………………………………… …………….2.6W
Operating Junction Temperature .... 150°C
Lead Temperature .... 260°C
Storage Temperature............... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .... 4.5V to 36V
Output Voltage V_{OUT}...................0.8V to 0.9×V_{IN}
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN20 (3mm×4mm)...............48 ...... 10 ...°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

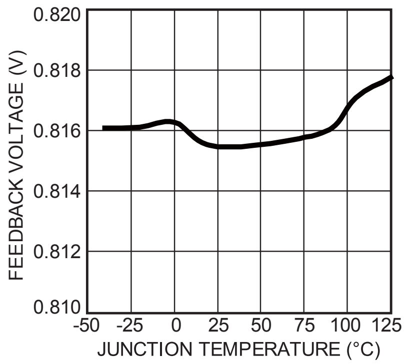
V_{IN} = 24V, V_{EN} = 2V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		10	300	nA
Supply Current (Quiescent)	I_{IN}	V_{FB} = 0.95V		500	600	μA
HS Switch On Resistance	HS_{RDS-ON}			40	65	mΩ
LS Switch On Resistance (5)	LS_{RDS-ON}			20		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V V_{SW} = 0V or 36V		10	400	nA
Current Limit	I_{LIMIT}		6	8	12	A
One-Shot On Time	t_{ON}	V_{IN}=12V, R_{FREQ}=30kΩ	230	280	330	ns
Minimum Off Time(5)	t_{OFF}			100		ns
Fold-back Off Time(5)	t_{FB}	I_{LIM}=1(HIGH), FB>50%V_{REF}		4.8		μs
Fold-back Off Time(5)	t_{FB}	I_{LIM}=1(HIGH), FB<50%V_{REF}		16.8		μs
OCP hold-off time(5)	t_{OC}	I_{LIM}=1(HIGH)		100		μs
Feedback Voltage	V_{FB}	T_J = 25°C	807	815	823	mV
	V_{FB}	T_J = -40°C to 125°C	803		827	mV
Feedback Current	I_{FB}	V_{FB} = 815mV		10	50	nA
Soft Start Charging Current	I_{SS}	V_{SS}=0V	6	8.5	11	μA
Power Good Rising Threshold	$PGOOD_{Vth-Hi}$		0.87	0.9	0.93	V_{FB}
Power Good Falling Threshold	$PGOOD_{Vth-Lo}$		0.82	0.85	0.88	V_{FB}
Power Good Threshold Hysteresis	$PGOOD_{Vth-Hys}$			0.05		V_{FB}
Power Good Rising Delay	t_{PGOOD}		500	700	900	μs
EN Rising Threshold	EN_{Vth-Hi}		1.1	1.25	1.4	V
EN Falling Threshold	EN_{Vth-Lo}		0.73	0.86	0.99	V
EN Threshold Hysteresis	$EN_{Vth-Hys}$			390		mV
EN Input Current	I_{EN}	V_{EN} = 2V		1.5	2	μA
V_{IN} Under-Voltage Lockout Threshold Rising	$INUV_{Vth\_R}$		3.7	4.0	4.3	V
V_{IN} Under-Voltage Lockout Threshold Falling	$INUV_{Vth\_F}$		2.8	3.1	3.4	V
V_{IN} Under-Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			900		mV
V_{CC} Regulator	V_{CC}	I_{CC}=0	4.5	4.85	5.2	V
V_{CC} Load Regulation		I_{CC}=10mA		1	2	%
Vo Over-Voltage Protection Threshold (6)	V_{OVP}		1.15	1.25	1.35	V_{FB}
Thermal Shutdown(5)	T_{SD}			175		°C
Thermal Shutdown Hysteresis(5)	T_{SD-HYS}			45		°C

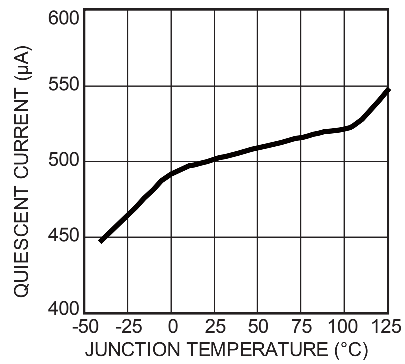
Note:
5) Derived from bench characterization, not tested in production.
6) For MPQ4470 only, MPQ4470A has no OVP function.

TYPICAL CHARACTERISTICS

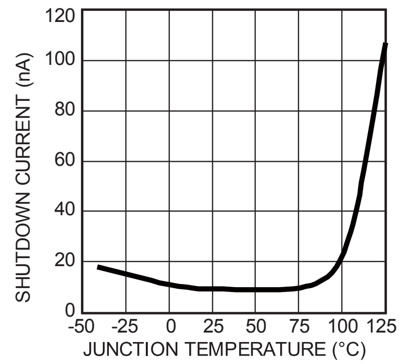
Feedback Voltage vs. Junction Temperature
VIN=24V



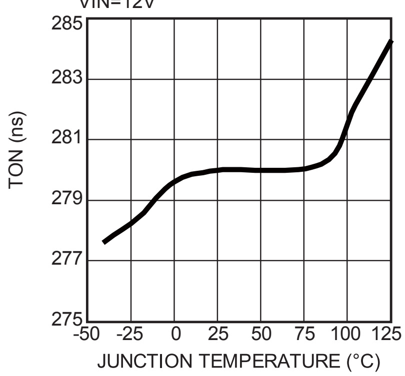
Quiescent Current vs. Junction Temperature
VIN=24V



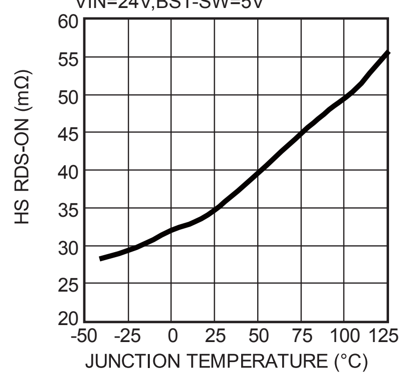
Shutdown Current vs. Junction Temperature
VIN=24V



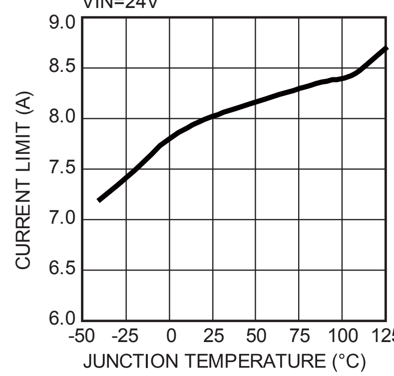
Ton vs. Junction Temperature
VIN=12V



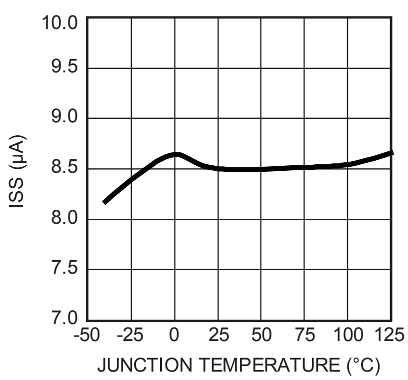
HS R_{DS-ON} vs. Junction Temperature
VIN=24V,BST-SW=5V



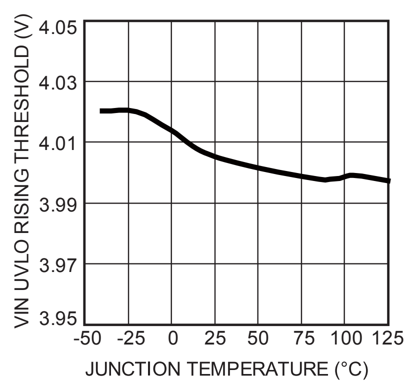
Current Limit vs. Junction Temperature
VIN=24V



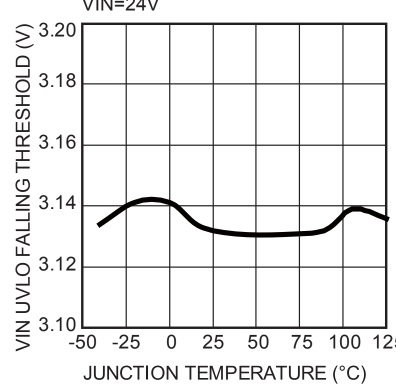
I_{SS} vs. Junction Temperature
VIN=24V



VIN UVLO Rising Threshold vs. Junction Temperature

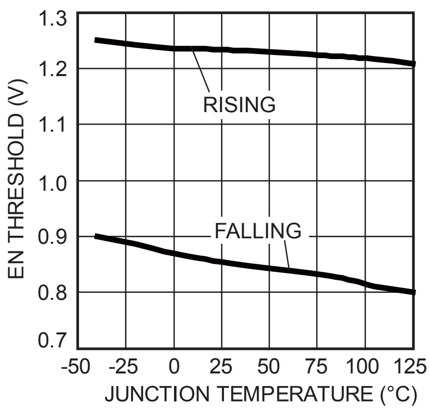


VIN UVLO Falling Threshold vs. Junction Temperature
VIN=24V

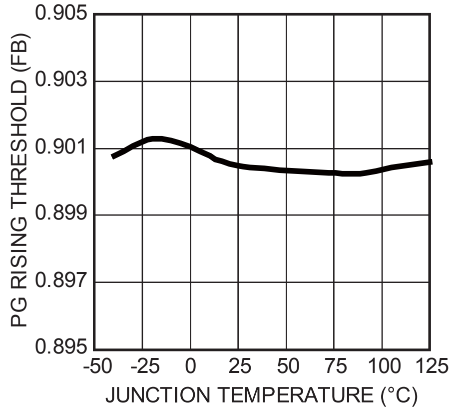


TYPICAL CHARACTERISTICS

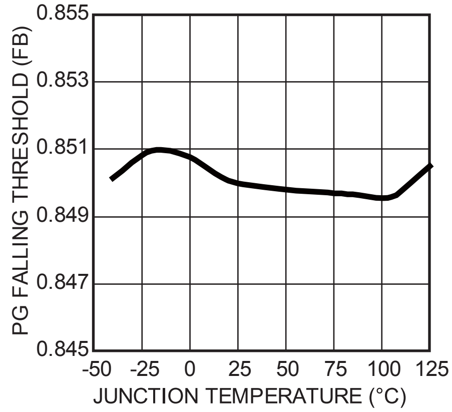
EN Threshold vs. Junction Temperature
VIN=24V



PG Rising Threshold vs. Junction Temperature
VIN=24V



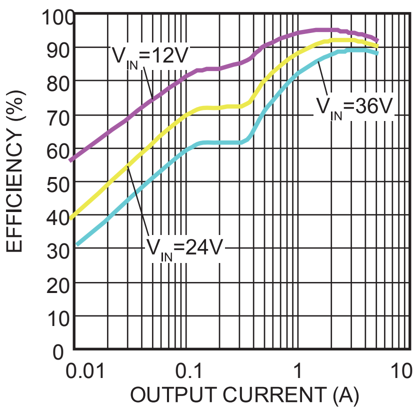
PG Falling Threshold vs. Junction Temperature
VIN=24V



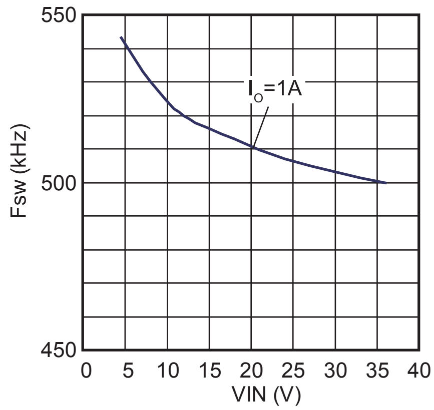
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 3.3V, L = 10µH, R_{FREQ} = 63.4k, T_A = +25°C, unless otherwise noted.

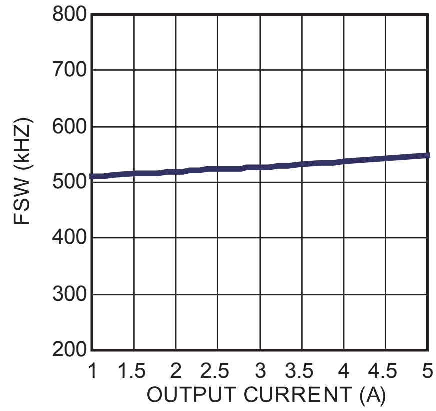
Efficiency vs. Load Current



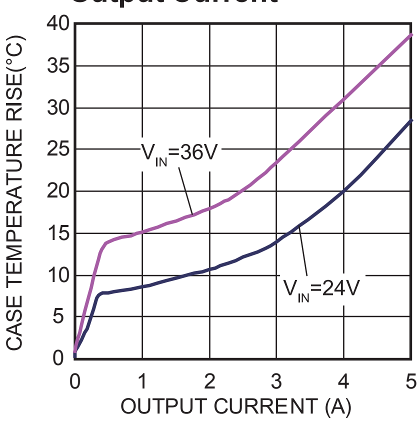
Fsw vs. VIN



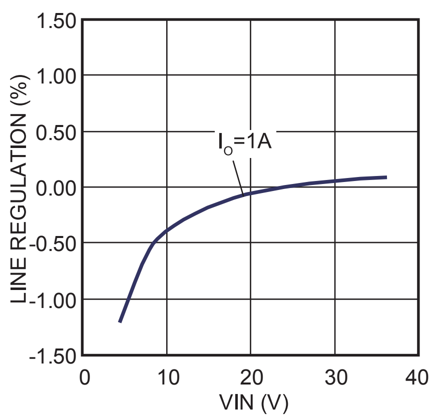
Fsw vs. Output Current



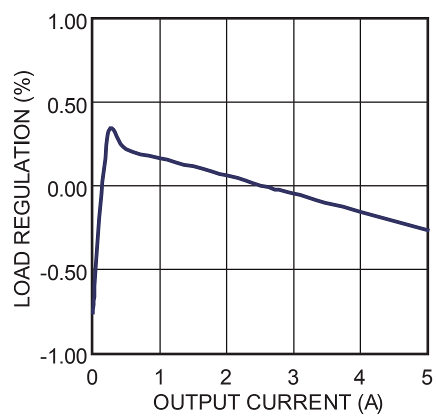
Case Temperature Rise vs. Output Current



Line Regulation



Load Regulation

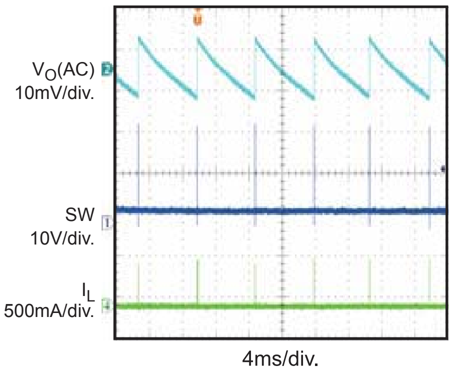


TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

V_{IN} = 24V, V_{OUT} = 3.3V, L = 10µH, R_{FREQ} = 63.4k, T_A = +25°C, unless otherwise noted.

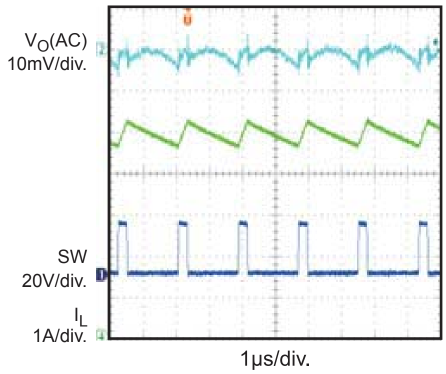
Output Voltage Ripple

I_O = 0A



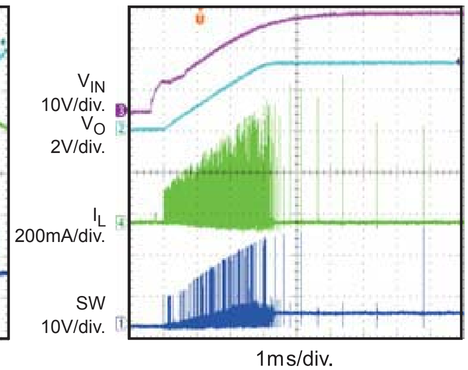
Output Voltage Ripple

I_O = 5A



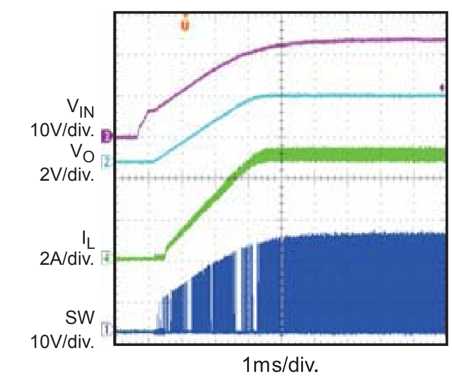
Start-up Through VIN

I_O = 0A



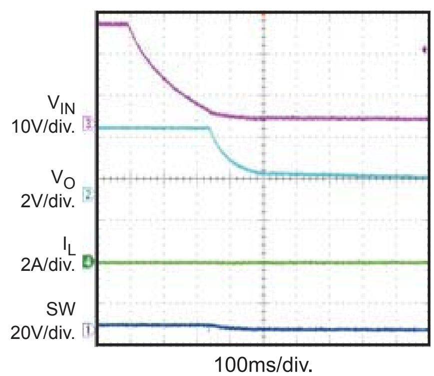
Start-up Through VIN

I_O = 5A



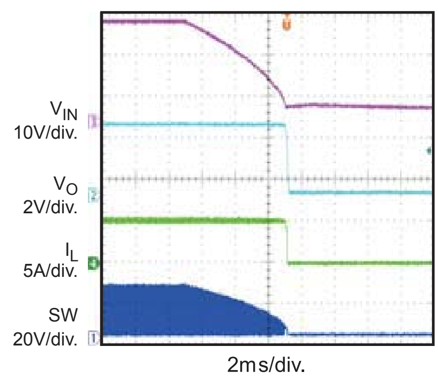
Shutdown Through VIN

I_O = 0A



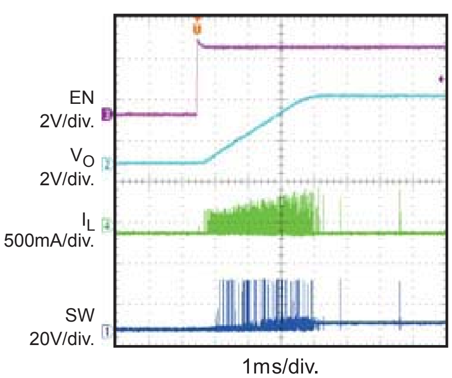
Shutdown Through VIN

I_O = 5A



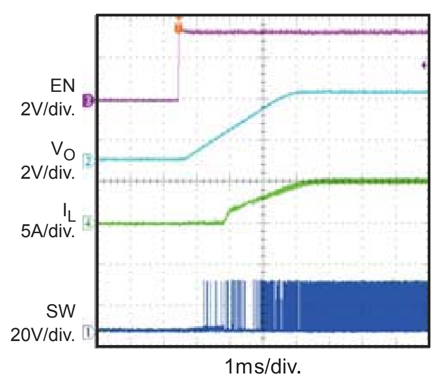
Start-up Through EN

I_O = 0A



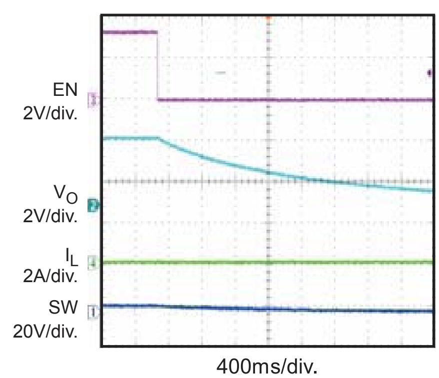
Start-up Through EN

I_O = 5A



Shutdown Through EN

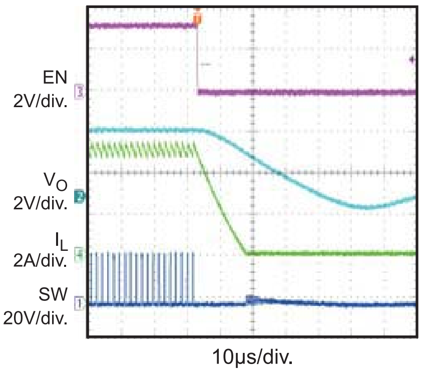
I_O = 0A



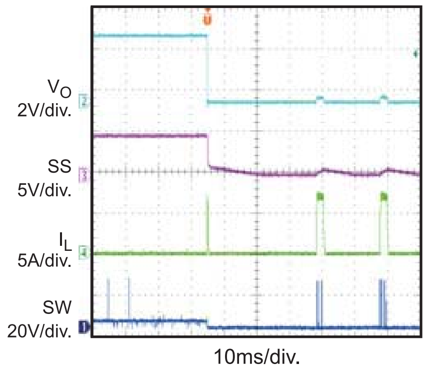
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

V_{IN} = 24V, V_{OUT} = 3.3V, L = 10µH, R_{FREQ} = 63.4k, T_A = +25°C, unless otherwise noted.

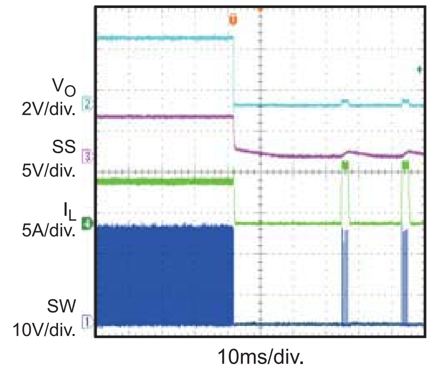
Shutdown Through EN
I_O = 5A



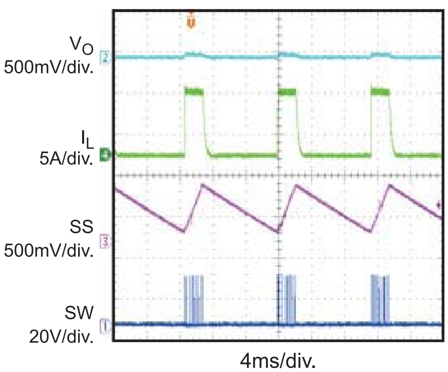
Short Circuit Entry
I_O = 0A



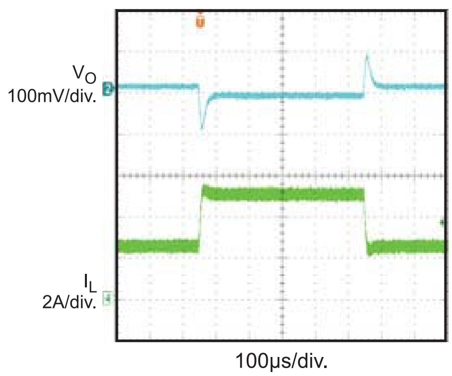
Short Circuit Entry
I_O = 5A



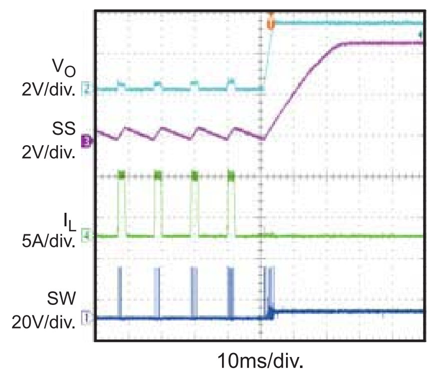
Short Circuit Steady State



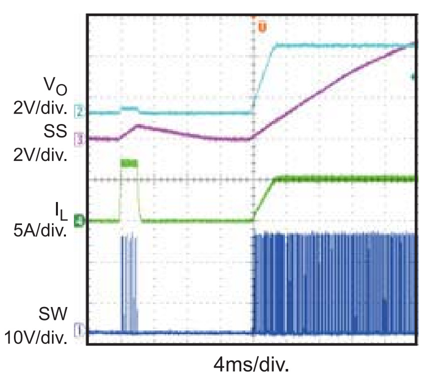
Load Transient
I_O = 2.5A-5A@1.6A/µs



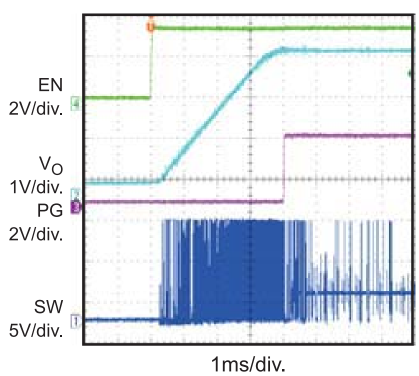
Short Circuit Recovery
I_O = 0A



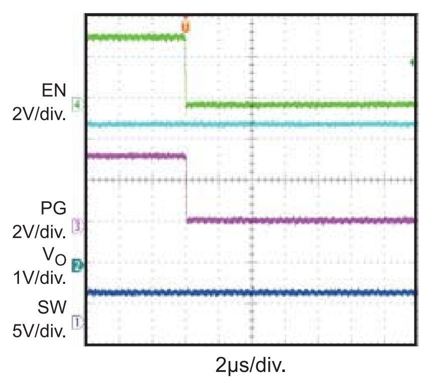
Short Circuit Recovery
I_O = 5A



Power Good Through EN Start-up



Power Good Through EN Shutdown



PIN FUNCTIONS

Pin #	Name	Description
1	AGND	Analog Ground.
2	FREQ	Frequency Set (for CCM). The input voltage and the frequency-set resistor connected to GND determine the ON period.
3	FB	Feedback. The tap of external resistor divider from the output to GND sets the output voltage.
4	SS	Soft-Start. Connect an external capacitor to program the soft-start time for the switch-mode regulator. When the EN pin goes HIGH, an internal current source (8.5μA) charges up the capacitor and the SS voltage slowly and smoothly ramps up from 0 to V_{FB}. When the EN pin goes LOW, the internal current source discharges the capacitor and the SS voltage slowly ramps down.
5	EN	Enable. EN=1 to enable the MPQ4470/4470A. For automatic start-up, connect EN pin to IN with a high ohm resistor. It includes an internal 1MΩ pull-down resistor.
6	PGOOD	Power Good Output. The output of this pin is an open drain and goes HIGH if the output voltage exceeds 90% of the nominal voltage. There is delay of ~700μs from FB ≥ 90% to PGOOD HIGH.
7	BST	Bootstrap. Requires a 0.1μF-to-1μF capacitor connected between SW and BS pins to form a floating supply across the high-side switch driver.
8, 19, Exposed pads 21, 22, 23	IN	Supply Voltage. The MPQ4470/4470A operates from a 4.5V-to-36V input rail. Requires C_{IN} to decouple the input rail. Connect using wide PCB traces and multiple vias.
9, 10, 17, 18, Exposed pads 24, 25	SW	Switch Output. Connect using wide PCB traces and multiple vias.
11-16	PGND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
20	VCC	Internal Bias Supply. Decouple with a 1μF capacitor as close to the pin as possible.

BLOCK DIAGRAM

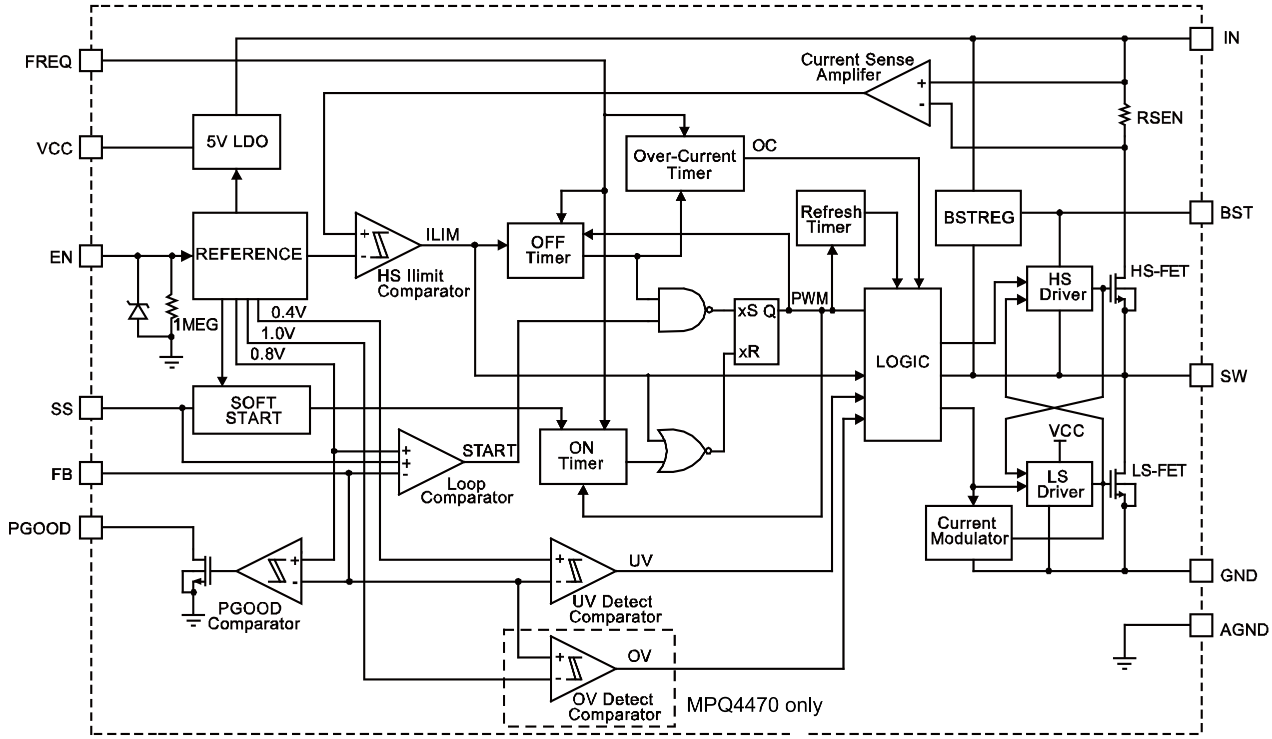


Figure —Functional Block Diagram

OPERATION

PWM Operation

The MPQ4470/4470A is a fully-integrated, synchronous, rectified, step-down, switch-mode converter. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The ON period is determined by the input voltage and the frequency-set resistor as:

$$t_{ON}(ns) = \frac{96 \times R_{FREQ}(k\Omega)}{V_{IN}} + t_{DELAY}(ns) \quad (1)$$

After the ON period elapses, the HS-FET turns OFF. It is turned ON again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns ON when the HS-FET is OFF to minimize conduction loss. A dead short occurs between input and GND if both the HS-FET and the LS-FET turn on at the same time (shoot-through). An internal dead-time (DT) generated between HS-FET OFF and LS-FET ON, or LS-FET OFF and HS-FET ON prevents shoot-through.

Heavy-Load Operation

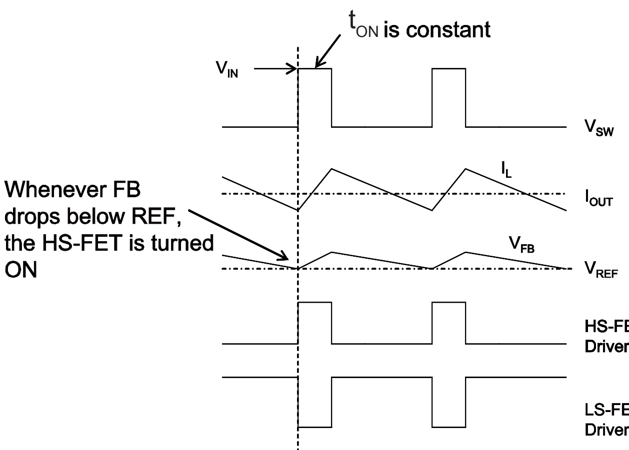


Figure : Heavy-Load Operation

In continuous-conduction mode (CCM), when the output current is HIGH, the HS-FET and LS-FET repeatedly turn ON/OFF as shown in MPS. All Rights Reserved. The inductor current never goes to zero. In CCM, the switching frequency (f_{SW}) is fairly constant.

Light-Load Operation

At light-load or no-load conditions, the output drops very slowly and the MPQ4470/4470A reduces the switching frequency automatically to maintain high efficiency. Figure 3 shows the light-load operation. V_{FB} does not reach V_{REF} as the inductor current approaches zero. The LS-FET driver enters a tri-state (high Z) whenever the inductor current reaches zero. A current modulator takes control of the LS-FET and limits the inductor current to less than -1mA. Hence, the output capacitors discharge slowly to GND through the LS-FET to greatly improve the light-load efficiency. At light loads, the HS-FET does not turn ON as frequently as at heavy loads. This is called skip mode.

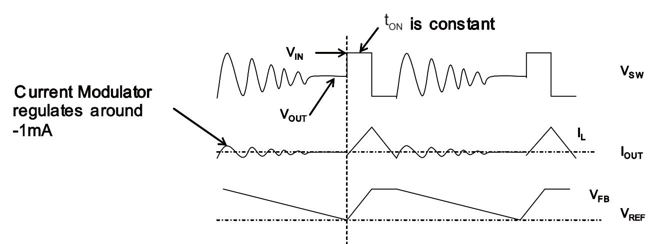


Figure : Light-Load Operation

As the output current increases from light-load condition, the current modulator's regulatory time period becomes shorter. The HS-FET turns ON more frequently, thus increasing the switching frequency increases. The output current reaches its critical level when the current modulator time is zero. The critical output current level is:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (2)$$

It enters PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Switching Frequency

The input voltage is feed-forwarded to the on-time one-shot timer through the resistor, R_{FREQ}. The duty ratio remains at V_{OUT}/V_{IN}. Hence, the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as:

$$F_{SW}(kHz) = \frac{10^6}{[\frac{96 \times R_{FREQ}(k\Omega)}{V_{IN}} + t_{DELAY}(ns)] \times \frac{V_{IN}}{V_{OUT}}} \quad (3)$$

Where t_{DELAY} is the comparator delay (~20ns).

The MPQ4470/4470A is optimized for 100kHz-to-1MHz applications to operate at high switching frequencies with high efficiency. The high-switching frequency allows for smaller LC-filter components to reduce PCB space requirements.

Ramp Compensation

Figure 4 and Figure 5 show jitter occurring in both PWM mode and skip mode. Noise on V_{FB}'s downward slope causes the HS-FET ON time to deviate from its intended position and produces jitter. There is a relationship between system stability and the steepness of the V_{FB} ripple: The slope steepness of the V_{FB} ripple dominates noise immunity. The magnitude of the V_{FB} ripple doesn't affect the noise immunity directly.

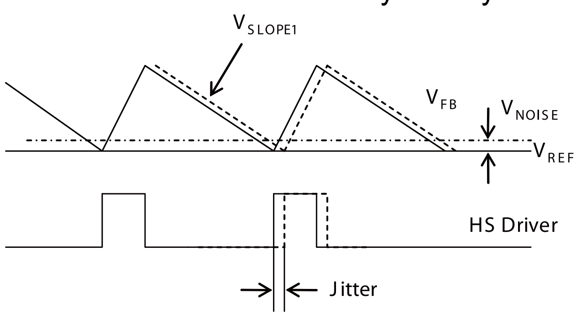


Figure : Jitter in PWM Mode

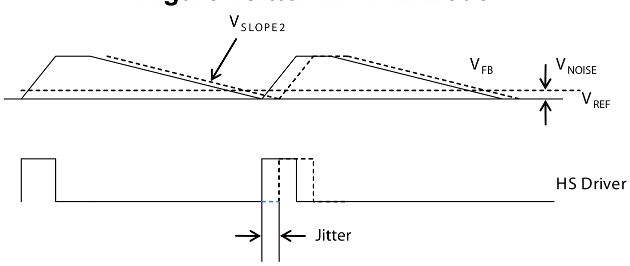


Figure : Jitter in Skip Mode

Ceramic output capacitors lack enough ESR ripple to stabilize the system, and requires an external compensation ramp.

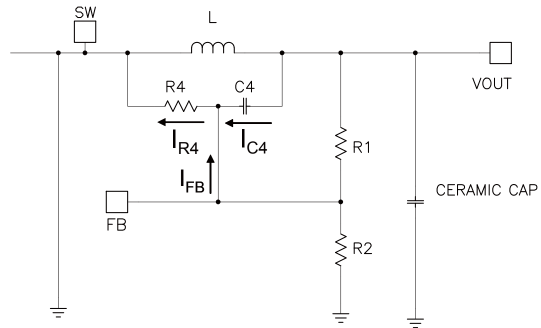


Figure : Simplified Circuit in PWM Mode with External Ramp Compensation

In PWM mode has an equivalent circuit with HS-FET OFF and uses a external ramp compensation circuit (R_4, C_4), shown as a simplified circuit in Figure 6. Derive the external ramp from the inductor-ripple current. Choose C_4, R_1, and R_2 to meet the following condition:

$$\frac{1}{2\pi \times F_{SW} \times C_4} < \frac{1}{5} \times \left(\frac{R_1 \times R_2}{R_1 + R_2} \right) \quad (4)$$

Then:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (5)$$

The V_{FB} downward slope ripple is then estimated as:

$$V_{SLOPE1} = \frac{-V_{OUT}}{R_4 \times C_4} \quad (6)$$

From equation 6, reduce R_4 or C_4 to reduce instability in PWM mode. If C4 cannot be reduced further due to equation 4's limitations, then only reduce R_4. Based on bench experiments, V_{SLOPE1} is around 20V/ms-40V/ms.

In the case of POSCAP or other types of capacitors with higher ESR, an external ramp is not necessary.

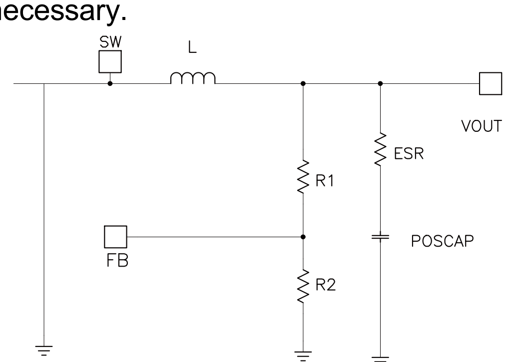


Figure : Simplified Circuit in PWM Mode without External Ramp Compensation

Figure 7 shows an equivalent circuit in PWM mode with the HS-FET OFF and without an external ramp circuit. The ESR ripple dominates the output ripple. The V_{FB} downward slope is:

$$V_{SLOPE1} = \frac{-ESR \times V_{REF}}{L} \quad (7)$$

From equation 7, the V_{FB} downward slope is proportional to ESR/L. Therefore, it's necessary to know the minimum ESR value of the output capacitors without an external ramp. There is also an inductance limit: A smaller inductance leads to more stability. Based on bench experiments, keep V_{SLOPE1} around 15V/ms to 30V/ms.

In skip mode, the external ramp does not affect the downward slope, and V_{FB} ripple's downward slope is the same with or without the external ramp. Figure 8 shows an equivalent circuit with the HS-FET off and the current modulator regulating the LS-FET.

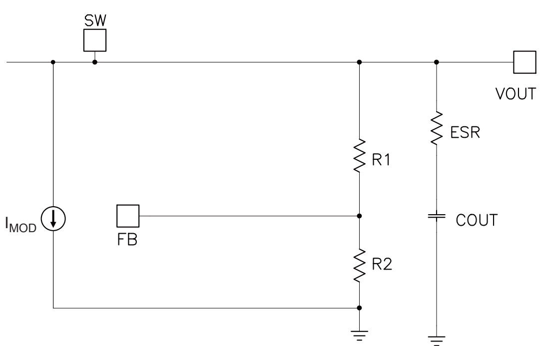


Figure : Simplified Circuit in Skip Mode

The V_{FB} ripple's downward slope is:

$$V_{SLOPE2} = \frac{-V_{REF}}{(R_1 + R_2) \times C_{OUT}} \quad (8)$$

To keep the system stable during light loads, avoid large V_{FB} resistors. Also, keep the V_{SLOPE2} value around 0.4V/ms to 0.8mV/ms. Note that I_{MOD} is excluded from the equation because it does not impact the system's light-load stability.

Enable Control

The MPQ4470/4470A has a dedicated enable-control pin EN. After V_{IN} goes high, drive EN high to turn on the chip, drive EN low to turn the chip off. EN falling threshold is a consistent 0.86V. Its rising threshold is about 390mV higher. When floating, EN pin is internally pulled down to GND to disable the chip.

Internally a zener diode is connected from EN pin to GND pin. The typical clamping voltage of the zener diode is 6.5V. So VIN can be connected to EN through a high ohm resistor if the system doesn't have another logic input acting as enable signal. The resistor needs to be designed to limit the EN sink current less than 150µA. Just note that there is an internal 1M resistor from EN to GND, so the external pull up resistor should be smaller than $\frac{[V_{IN(MIN)} - 1.25V] \times 1M}{1.25V}$ to make sure the part can EN on at the lowest operation VIN.

Soft-Start

The MPQ4470/4470A employs soft start (SS) to ensure a smooth output during power-up. When the EN pin goes HIGH, an internal current source (8.5µA) charges up the SS capacitor (C_{SS}). The C_{SS} voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with V_{SS}. Once V_{SS} reaches the same level as V_{REF}, it continues ramping up while V_{REF} takes over the PWM comparator. At this point, soft-start finishes and the MPQ4470/4470A enters steady-state.

C_{SS} is then:

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (9)$$

If the output capacitors have large capacitance values, avoid setting a short SS or risk hitting the current limit during SS. Select a minimum value of 4.7nF if the output capacitance value exceeds 330µF.

Power Good (PGOOD)

The MPQ4470/4470A has power-good (PGOOD) output. The PGOOD pin is the open drain of a MOSFET. It should connect to V_{CC} or some other voltage source through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns ON so that the PGOOD pin is pulled to GND before SS is ready. After V_{FB} reaches 90%×V_{REF}, the PGOOD pin is pulled HIGH after a delay; typically 700µs.

When the FB voltage drops to 85%×V_{REF}, the PGOOD pin is pulled LOW.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPQ4470/4470A has cycle-by-cycle over-current limit control. The inductor current is monitored during the ON state. Once the inductor current exceeds the current limit, the HS-FET turns OFF. At the same time, the OCP timer starts. The OCP timer is set at 100µs. Hitting the current limit during each cycle during this 100µs time frame will trigger hiccup SCP.

If a short circuit occurs, the MPQ4470/4470A will immediately hit its current limit and V_{FB} will drop below 50%×V_{REF} (0.815V). The device considers this an output dead short and will trigger hiccup SCP immediately.

Over/Under-Voltage Protection (OVP/UVP)

The MPQ4470 monitors the output voltage through the tap of a resistor divider to the FB pin to detect output over-voltage conditions. A V_{FB} that exceeds 125%×V_{REF} (0.815V) triggers OVP latch-off. Once OVP triggers, the LS-FET turns on to discharge V_O until the inductor current drops to zero while the HS-FET remains off. The MPQ4470 needs to power cycle to restart. Note that MPQ4470A has no this OVP function.

The MPQ4470/4470A also monitors FB pin voltage to detect output under-voltage condition. A V_{FB} drop below 50% ×V_{REF} triggers UVP as well as a current-limit that triggers SCP.

UVLO Protection

The MPQ4470/4470A has under-voltage lock-out protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MPQ4470/4470A will be powered up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor power the floating-power-MOSFET driver. A dedicated internal regulator charges and regulates the bootstrap capacitor voltage to ~5V. When the voltage between the BST and SW nodes drops below regulation, a PMOS pass transistor connected from VIN to BST turns on. The charging current path is from VIN, BST and then to SW. The external circuit should provide enough voltage headroom to facilitate charging.

As long as V_{IN} is significantly higher than SW, the bootstrap capacitor remains charged. When the HS-FET is ON, $V_{IN}≈V_{SW}$ so the bootstrap capacitor cannot charge.

When the LS-FET is ON, $V_{IN}−V_{SW}$ reaches its maximum for fast charging. When there is no inductor current, $V_{SW}=V_{OUT}$ so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

At higher duty cycles, the bootstrap-charging time is shorter so the bootstrap capacitor may not charge sufficiently. In case the internal circuit has insufficient voltage and time to charge the bootstrap capacitor, the bootstrap capacitor voltage will drop low. When $V_{BST}−V_{SW}$ drops below 2.3V, the HS-FET turns OFF. A UVLO circuit allows the LS-FET to conduct and refresh the charge on the bootstrap capacitor. Once bootstrap capacitor voltage is charged, the HS-FET can turn on again and the part resumes normal switching. With this bootstrap refreshing function, MPQ4470/4470A is able to work on the low drop-out mode.

Thermal Shutdown

The MPQ4470/4470A uses thermal shutdown. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 175°C), the converter shuts off. This is a non-latched protection. There is about 45°C hysteresis. Once the junction temperature drops to about 130°C, it initiates a SS.

APPLICATION INFORMATION

Setting the Output Voltage

A resistor divider from the output voltage to the FB pin set V_{OUT}.

Without an external ramp employed, the feedback resistors (R_1 and R_2) set the output voltage. To determine the values for the resistors, first, choose R_2 (typically 5kΩ-40kΩ). Then R_1 is:

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (10)$$

When using a low-ESR ceramic capacitor on the output, add an external voltage ramp to the FB pin through R_4 and C_4. The ramp voltage (V_{RAMP}) affects output voltage. Calculate V_{RAMP} as per equation 18. Choose R_2 between 5kΩ and 40kΩ. Determine R_1 as:

$$R_1 = \left(\frac{V_{REF} + \frac{1}{2}V_{RAMP}}{R_2 \times (V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})} - \frac{1}{R_4} \right)^{-1} \quad (11)$$

Using equation 11 to calculate the output voltage can be complicated. Furthermore, as V_{RAMP} changes due to changes in V_{OUT} and V_{IN}, V_{FB} also varies. To improve the output voltage accuracy and simplify the R_2 calculation from equation 11, add a DC-blocking capacitor (C_{DC}). Figure 9 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. Equation 10 can then estimate R_1)

Select a C_{DC} value between 1μF and 4.7μF to improve DC-blocking performance.

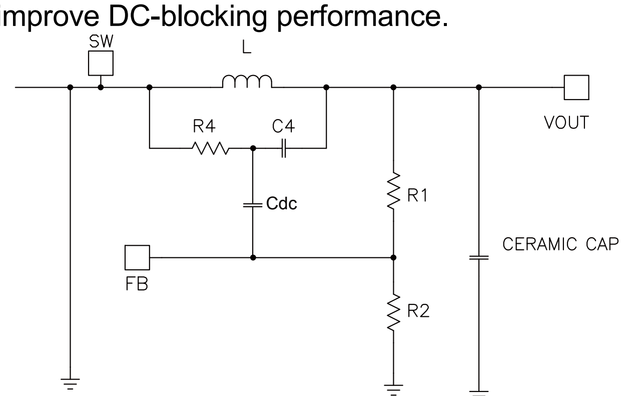


Figure : Simplified Circuit with External Ramp Compensation and DC Blocking Capacitor

Input Capacitor

The input current to the step-down converter is discontinuous, and Therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance. Be sure to place the input capacitors as close to the IN pin as possible.

The capacitance varies significantly with temperature. Capacitors with X5R and X7R ceramic dielectrics are are fairly stable over temperature fluctuations.

The capacitors must also have a ripple-current rating greater than the converter's maximum input-ripple current. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (12)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (13)$$

For simplification, choose an input capacitor whose RMS current rating is greater than half of the maximum load current.The input capacitance value determines the input voltage ripple of the converter. If there is an input-voltage-ripple requirement in the system design, choose an input capacitor that meets the specification

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (15)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic or POSCAP capacitors. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (16)$$

Where R_{ESR} is the equivalent series resistance of the output capacitor.

For ceramic capacitors, capacitance dominates the impedance at the switching frequency, can is the primary cause of the output-voltage ripple. For simplification, estimate the output voltage ripple as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (17)$$

The output voltage ripple caused by ESR is very small and therefore requires an external ramp to stabilize the system. The voltage ramp is ~30mV. The external ramp can be generated through R_4 and C_4 using the following equation:

$$V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{R4 \times C4} \quad (18)$$

Select C_4 to meet the following condition:

$$\frac{1}{2\pi \times F_{SW} \times C4} < \frac{1}{5} \times (\frac{R1 \times R2}{R1 + R2}) \quad (19)$$

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value of 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (20)$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switching input voltage. A larger inductance will result in less ripple current and a lower output ripple voltage. However, a larger inductance resultsin a larger inductor, which will physically larger, and have a higher series resistance and/or lower saturation current. A good rule for determining the inductor value is to allow the peak-to-peak ripple current in the inductor to be approximately 30% to 40% of the maximum switch current limit. Ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (21)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (22)$$

Typical Design Parameter Tables

The following tables include recommended component values for typical output voltages (3.3V, 5V) and switching frequencies (300kHz, 500kHz, and 700kHz). Refer to Tables 1 through 3 for design cases without external ramp compensation, and Tables 4 through 6 for design cases with external ramp compensation. An external ramp is not needed when using high-ESR capacitors, such as electrolytic or POSCAPs. An external ramp is needed when using low-ESR capacitors, such as ceramic capacitors. For cases not listed in this datasheet, an Excel spreadsheet available through your local sales representative can calculate approximate component values.

Table 1—300kHz, 24V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R_{FREQ} (kΩ)
3.3	10	30.1	10	110
5	10	51.1	10	169

Table 2—500kHz, 24V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R_{FREQ} (kΩ)
3.3	10	30.1	10	63.4
5	10	51.1	10	100

Table 3—700kHz, 24V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R_{FREQ} (kΩ)
3.3	10	30.1	10	44.2
5	10	51.1	10	69.8

Table 4—300kHz, 24V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R_{FREQ} (kΩ)
3.3	10	30.9	10	953	390	110
5	10	53.6	10	845	560	169

Table 5—500kHz, 24V_{IN}

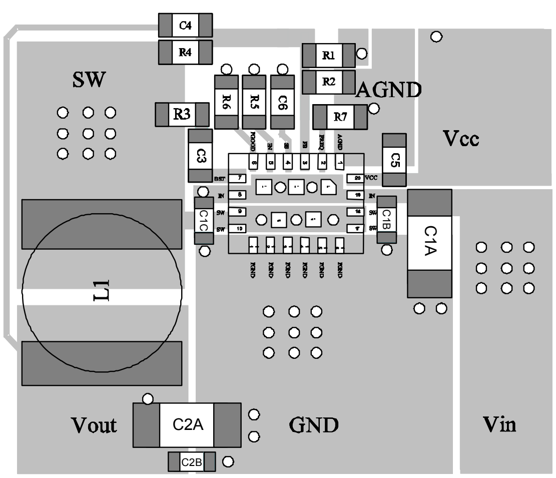
V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R_{FREQ} (kΩ)
3.3	10	31.6	10	620	390	63.4
5	10	53.6	10	845	390	100

Table 6—700kHz, 24V_{IN}

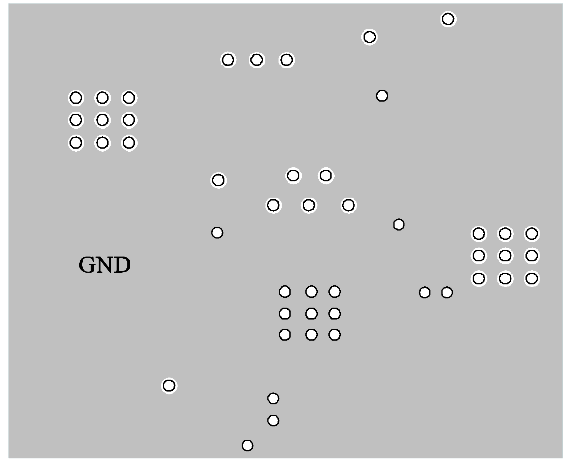
V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R_{FREQ} (kΩ)
3.3	10	31.6	10	560	390	44.2
5	10	54.9	10	620	390	69.8

LAYOUT RECOMMENDATION

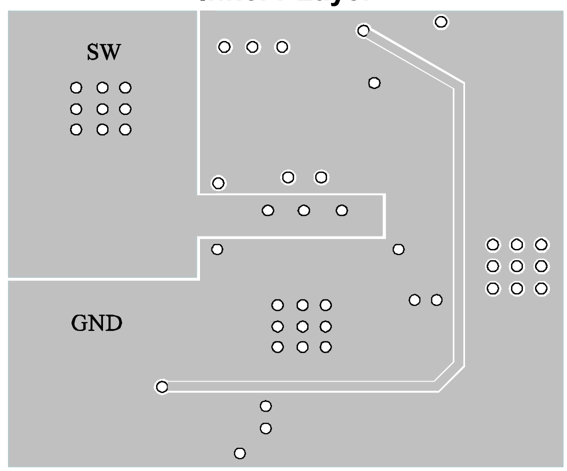
1. Place high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place input capacitors on both VIN sides (PIN8 and PIN19) and as close to the IN and GND pins as possible.
3. Place the decoupling capacitor as close to the VCC and GND pins as possible.
4. Keep the switching node SW short and away from the feedback network.
5. Place the external feedback resistors next to the FB pin. Do not place vias on the FB trace.
6. Keep the BST voltage path (BST, C3, and SW) as short as possible.
7. Connect the bottom IN and SW pads to a large copper area to achieve better thermal performance.
8. A Four-layer layout is strongly recommended to achieve better thermal performance.



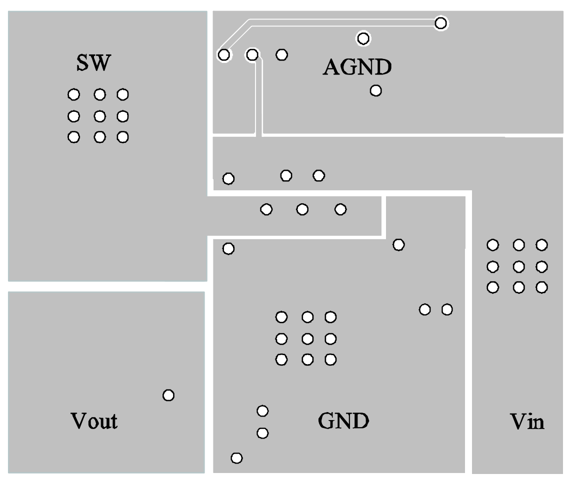
Top Layer



Inner1 Layer



Inner2 Layer



Bottom Layer

Figure : PCB Layout

TYPICAL APPLICATION CIRCUITS

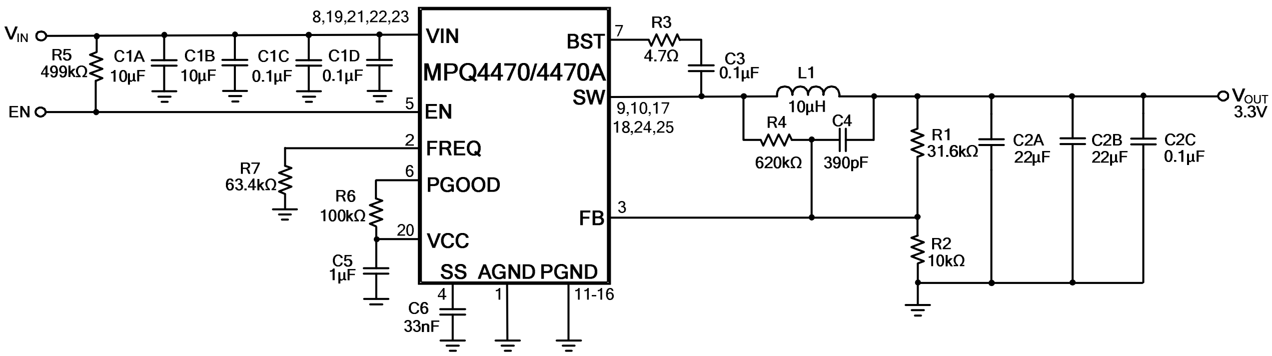
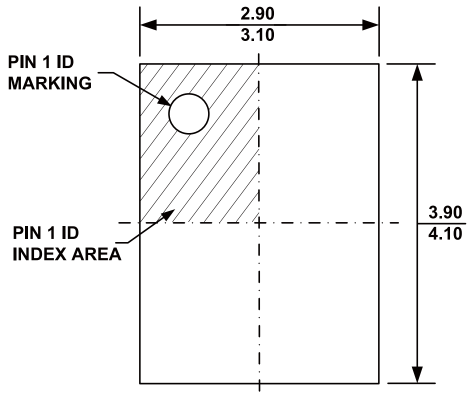


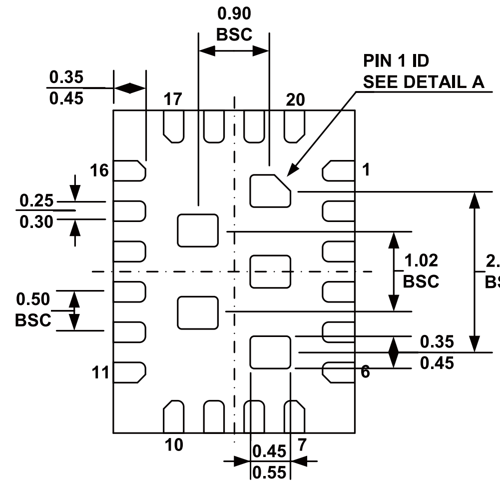
Figure : Typical Application Circuit, 3.3V-Output

PACKAGE INFORMATION

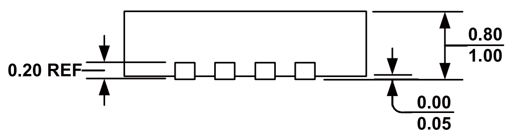
3mm × 4mm QFN20



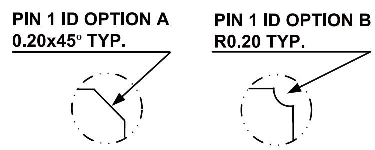
TOP VIEW



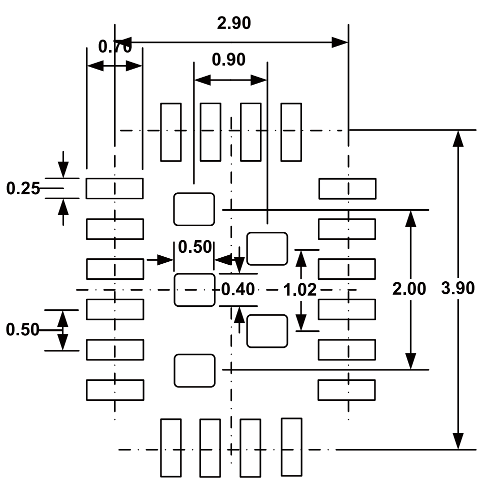
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.