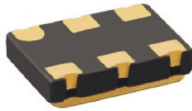


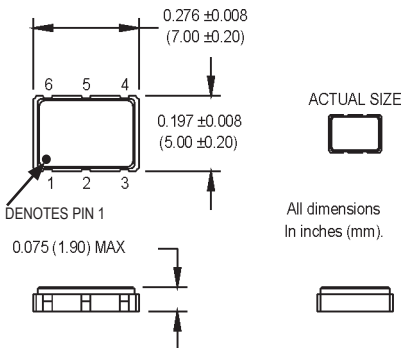
# UVC Series

## 5x7 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillators



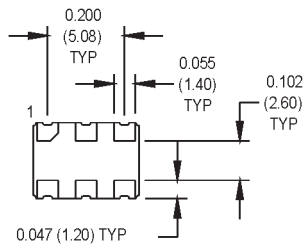
Ordering Information		UVC	1	8	R	L	N	00.0000 MHz
Product Series								
Temperature Range								
1: 0°C to +70°C	2: -40°C to +85°C							
6: -20°C to +70°C	7: -0°C to +85°C							
8: 0°C to +50°C								
Stability								
3: ±100 ppm	4: ±50 ppm							
6: ±25 ppm	8: ±20 ppm							
Output Type								
R: Complementary Enable	Z: Complementary w/o Enable							
Symmetry/Output Logic Type								
L: 45/55% LVDS	P: 45/55% PECL							
H: 40/60% LVDS	Q: 40/60% PECL							
Package/Lead Configurations								
N: Leadless Ceramic (6 pads)								
Frequency (customer specified)								

M2022Sxxx - Contact factory for datasheet.

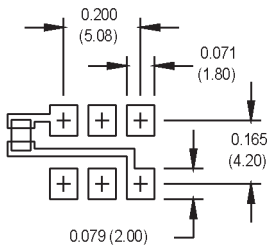


ACTUAL SIZE

All dimensions in inches (mm).



### SUGGESTED SOLDER PAD LAYOUT



### Pad Connections

Pad	Function
1	Enable/Disable for "R" Output Type or N/C for "Z" Output Type
2	N/C
3	Ground
4	Output Q
5	Complementary Output $\bar{Q}$
6	+ Vdd

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	0.75		800	MHz		
Operating Temperature	T <sub>A</sub>	(See ordering information)					
Storage Temperature	T <sub>S</sub>	-55		+125	°C		
Frequency Stability	ΔF/F	(See ordering information)					
Aging						See Note 1	
1st Year Thereafter (per year)		-3		+3	ppm		
		-1		+1	ppm		
Input Voltage	V <sub>CC</sub>	3.135	3.3	3.465	V		
PECL Input Current	I <sub>CC</sub>			70	mA	0.75 to 24 MHz	
				100	mA	24 to 96 MHz	
				110	mA	96 to 800 MHz	
LVDS Input Current	I <sub>CC</sub>			30	mA	0.75 to 24 MHz	
				60	mA	24 to 96 MHz	
				60	mA	96 to 800 MHz	
Output Type						PECL/LVDS	
Load		50 Ohms to V <sub>CC</sub> - 2 VCD 100 Ohm differential load				See Note 2 PECL Waveform LVDS Waveform	
Symmetry (Duty Cycle)		(See ordering information)					@ 50% of waveform
Output Skew				200	ps	PECL	
Differential Voltage	V <sub>OD</sub>	250	350	450	mV	LVDS	
Logic "1" Level	V <sub>OH</sub>	V <sub>CC</sub> - 1.02			V	PECL	
Logic "0" Level	V <sub>OL</sub>			V <sub>CC</sub> - 1.63	V	PECL	
Rise/Fall Time	T <sub>r</sub> /T <sub>f</sub>		0.35	0.55	ns	@ 20/80% LVPECL	
			0.50	1.0	ns	@ 20/80% LVDS	
Enable Function		80% V <sub>CC</sub> min or N/C: output active 20% V <sub>CC</sub> max: output disables to high-Z				Output Option R	
Start up Time				10	ms		
Phase Jitter (Typical)	φ <sub>J</sub>		3	5	ps RMS	Integrated 12 kHz - 20 MHz	
Mechanical Shock		MIL-STD-202, Method 213, C (100 g's)					
Vibration		MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
Thermal Cycle		MIL-STD-883, Method 1010, B (-55°C to +125°C, 15 min dwell, 10 cycles)					
Hermeticity		MIL-STD-202, Method 112					
Solderability		Per EIAJ-STD-002					
Max Soldering Conditions		See solder profile, Figure 1					

1. Inclusive of initial tolerance, deviation over temperature, shock, vibration, voltage and aging.
2. PECL load - see Load Circuit Diagram #5. LVDS load - see load circuit diagram #9.

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# MtronPTI Lead Free Solder Profile



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