AMMP-6120
8-24 GHz x2 Frequency Multiplier

AVAGO TECHNOLOGIES

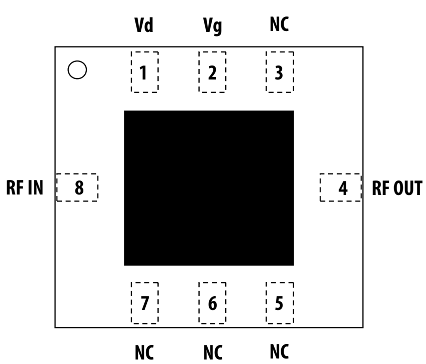
Data Sheet

Description

Avago Technologies' AMMP-6120 is an easy-to-use integrated frequency multiplier (x2) in a surface mount package designed for commercial communication systems. The MMIC takes a 4 to 12 GHz input signal and doubles it to 8 to 24 GHz. It has integrated amplification, matching, harmonic suppression, and bias networks. The input/output are matched to 50 Ω and fully DC blocked. The MMIC is fabricated using PHEMT technology.

The backside of the package is both RF and DC ground. This helps simplify the assembly process and reduces assembly related performance variations and costs. The surface mount package allows elimination of "chip & wire" assembly for lower cost. This MMIC is a cost effective alternative to hybrid (discrete-FET), passive, and diode doublers that require complex tuning and assembly processes.

Package Diagram



RoHS-Exemption

Please refer to hazardous substances table on page 7.

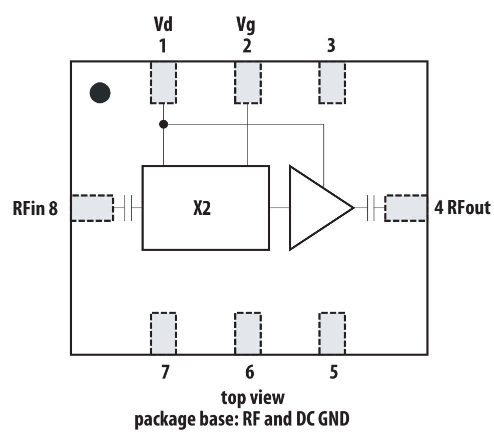
Features

- 5x5mm Surface Mount Package
- Frequency Range : 8-24 GHz output (Useable to 26 GHz)
- Broad input power range: -11 to +5 dBm
- Output Power : +16 to +18 dBm
- Harmonic Suppression : 20 dBc (Fundamental)
- DC requirements : -1.4V and 5V, 112 mA @ Pin= +3dBm

Applications

- Microwave Radio systems
- Satellite VSAT and DBS systems
- 802.16 & 802.20 WiMax BWA systems
- WLL and MMDS loops

Functional Block Diagram



Pin	Function
1	Vd
2	Vg
3	
4	RF Out
5	
6	
7	
8	RF In

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A) = 40V
ESD Human Body Model (Class 1A) = 250V
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

Note: MSL Rating = Level 2A

Electrical Specifications

1. Small/Large -signal data measured in a fully de-embedded test fixture form TA = 25°C.
2. Pre-assembly into package performance verified 100% on-wafer.
3. This final package part performance is verified by a functional test correlated to actual performance at one or more frequencies.
4. Specifications are derived from measurements in a 50 Ω test environment. Aspects of the amplifier performance may be improved over a more narrow bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.

Table 1. RF Electrical Characteristics

TA=25°C, Vd=50V, Vg=-1.4V, Idq=85mA, Zin=Zout=50 Ω

Parameter	Min	Typ.	Max	Unit
Output Power, Pout	13	16		dBm
Input Power at 1dB Gain Compression, IP-1dB		2		dBm
Input Return Loss, RLin		-15		dB
Output Return Loss, RLout		-10		dB
Fundamental Suppresion, Sup	18	25		dBc
3rd Harmonic Suppression, Sup3		25		dBc
4th Harmonic Suppression, Sup4		35		dBc
Single Side Band Phase Noise, SSBPN (@100kHz offset, fout=15.6GHz)		-140		dBc

Table 2. Recommended Operating Range

1. Ambient operational temperature TA = 25°C unless otherwise noted.
2. Channel-to-backside Thermal Resistance (Tchannel (Tc) = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temperature (Tb) = 25°C calculated from measured data.

Description	Min.	Typical	Max.	Unit	Comments
Drain Supply Current, Id		85	110	mA	Vd = 5V, Under any RF power drive and temperature
Gate Current, Ig		9		uA	

Table 3. Thermal Properties

Parameter	Test Conditions	Value
Thermal Resistance, θch-b	Channel-to-backside Thermal Resistance Tchannel(Tc)=34°C Thermal Resistance at backside temperature Tb=25°C	θch-b = 34 °C/W

Absolute Minimum and Maximum Ratings

Table 4. Minimum and Maximum Ratings

Description	Min.	Max.	Unit	Comments
Drain Supply Voltage, Vd		7	V	
Gate Supply Voltage, Vg	-3.0	+0.5	V	
Drain Current, Idq		120	mA	
CW Input Power, Pin		15	dBm	
Channel Temperature, Tch		+150	°C	
Storage Temperature , Tstg	-65	+150	°C	
Maximum Assembly Temperature, Tmax		+300	°C	60 second maximum

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.

AMMP-6120 Typical Performances

(T_A = 25°C, Z_{in} = Z_{out} = 50 Ω, Vd=5V, Vg=-1.4V)

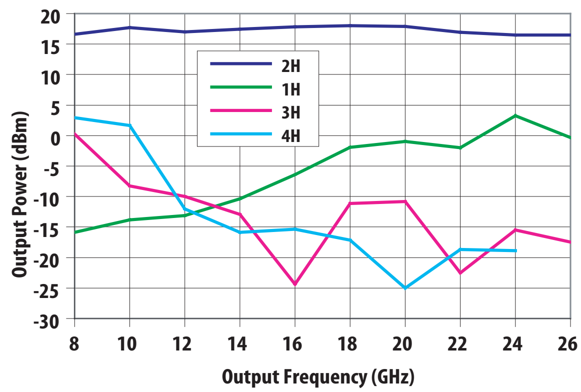


Figure 1. Output Power vs. Output Freq. @ Pin=+3dBm

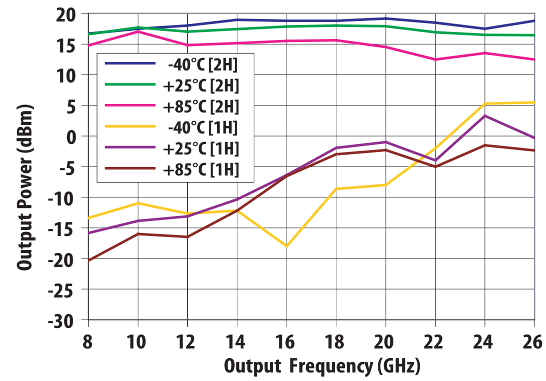


Figure 2. Output Power vs. Output Freq. over temp @ Pin=+3dBm

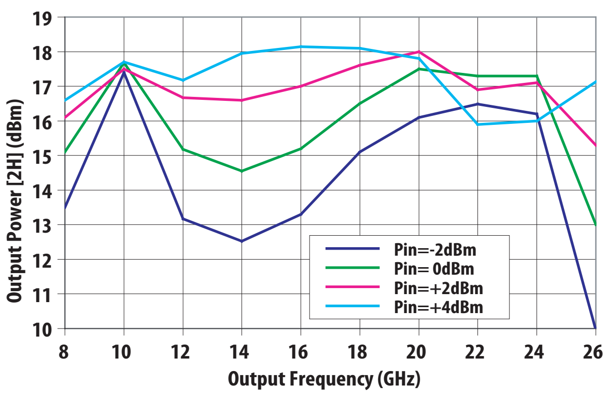


Figure 3. Output Power [2H] vs. Output Freq. at variable Pin

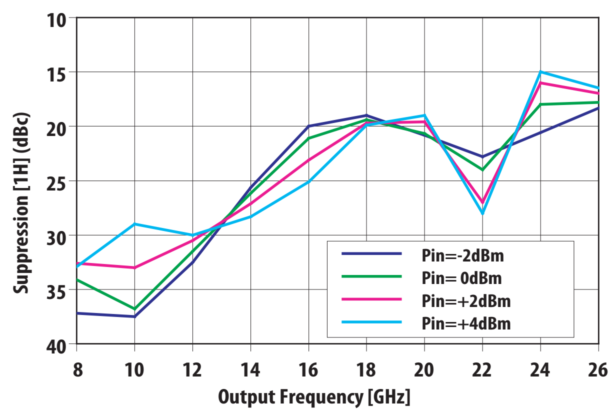


Figure 4. Fundamental Suppression at variable Pin

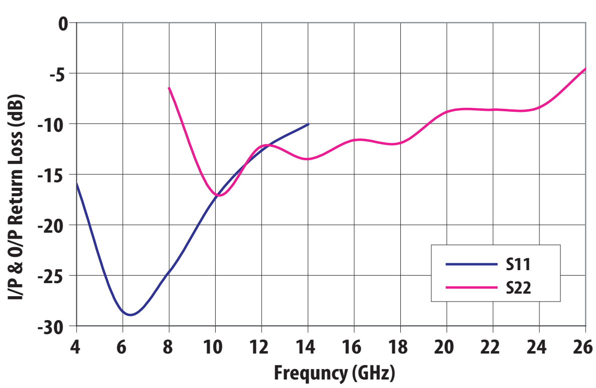


Figure 5. Input and Output Return Loss

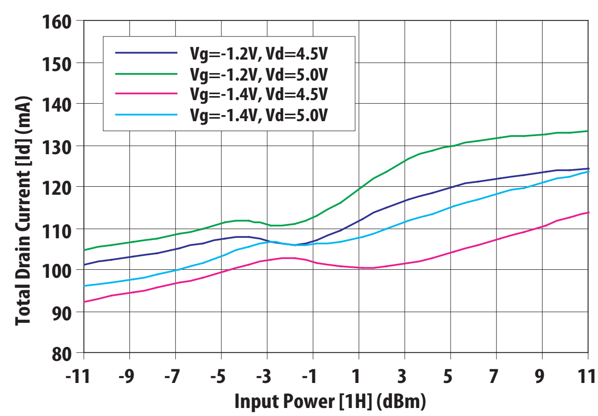


Figure 6. Variation of total drain current with input power

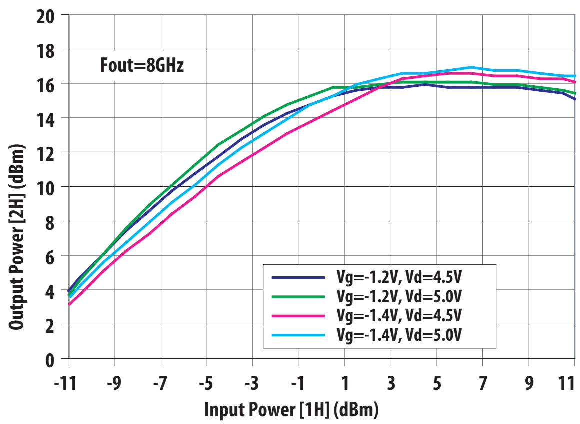


Figure 7. 2H Output Power Vs Input Power @ Fout=8GHz

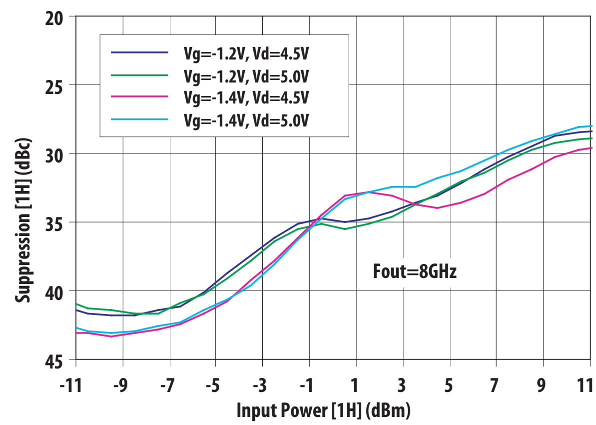


Figure 8. Fundamental Supp. Vs Input Power @ Fout=8GHz

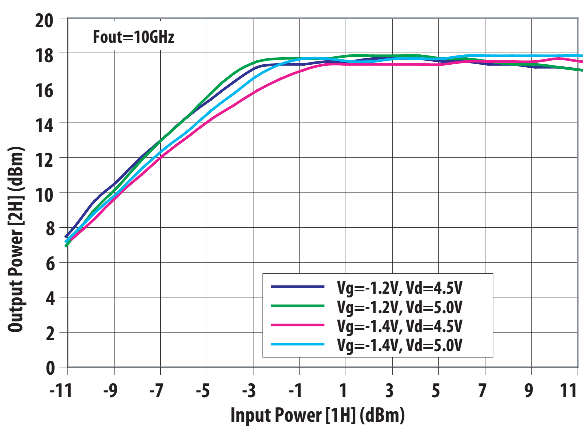


Figure 9. 2H Output Power Vs Input Power @ Fout=10GHz

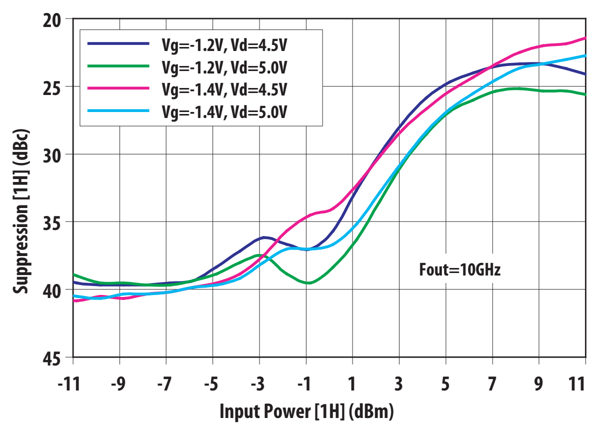


Figure 10. Fundamental Supp. Vs Input Power @ Fout=10GHz

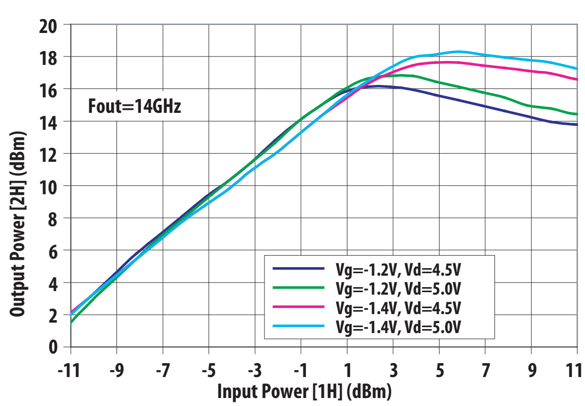


Figure 11. 2H Output Power Vs Input Power @ Fout=14GHz

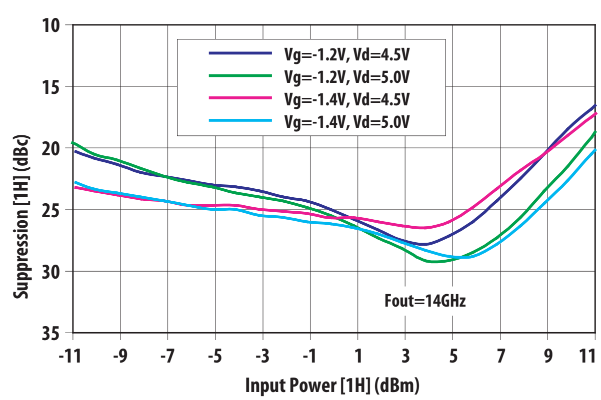


Figure 12. Fundamental Supp. Vs Input Power @ Fout=14GHz

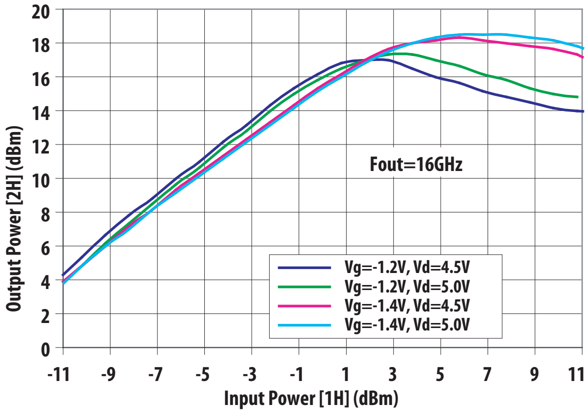


Figure 13. 2H Output Power Vs Input Power @ Fout=16GHz

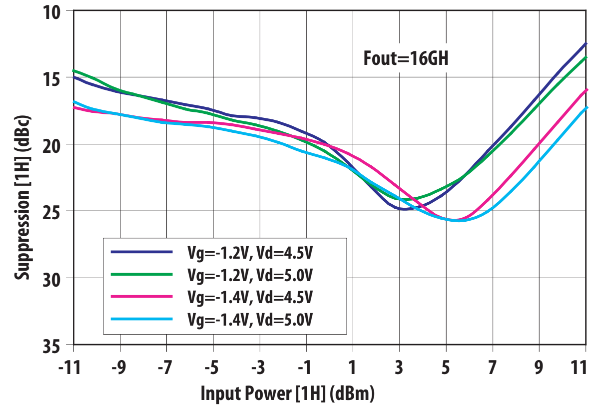


Figure 14. Fundamental Supp. Vs Input Power @ Fout=16GHz

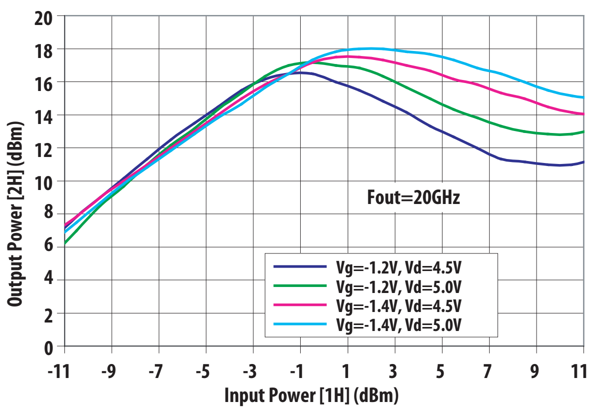


Figure 15. 2H Output Power Vs Input Power @ Fout=20GHz

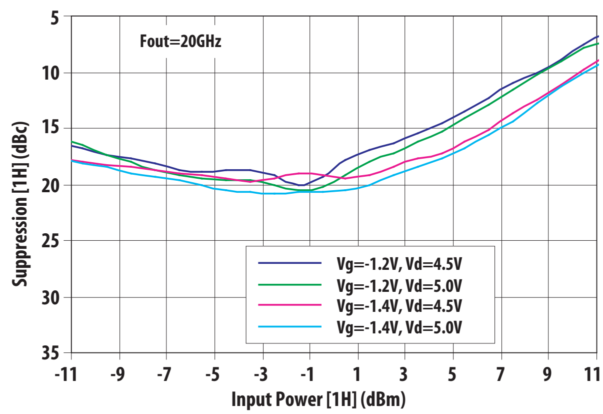


Figure 16. Fundamental Supp. Vs Input Power @ Fout=20GHz

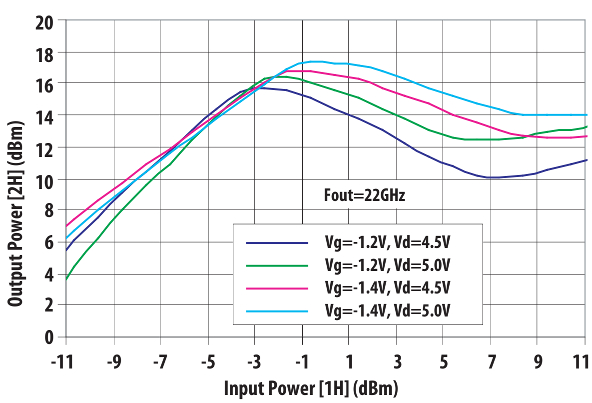


Figure 17. 2H Output Power Vs Input Power @ Fout=22GHz

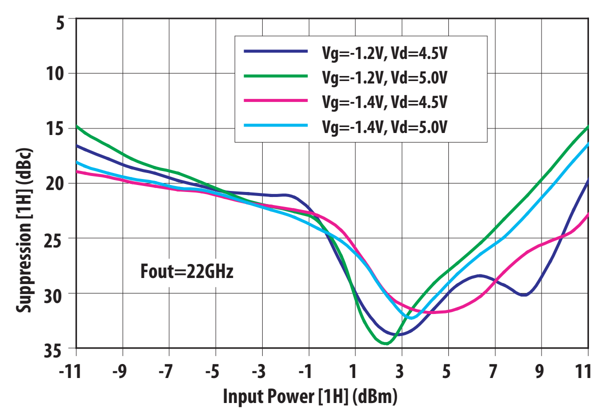


Figure 18. Fundamental Supp. Vs Input Power @ Fout=22GHz

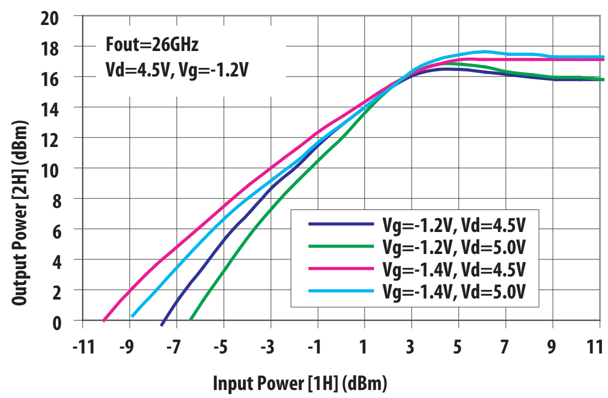


Figure 19 . 2H Output Power Vs Input Power @ Fout=26GHz

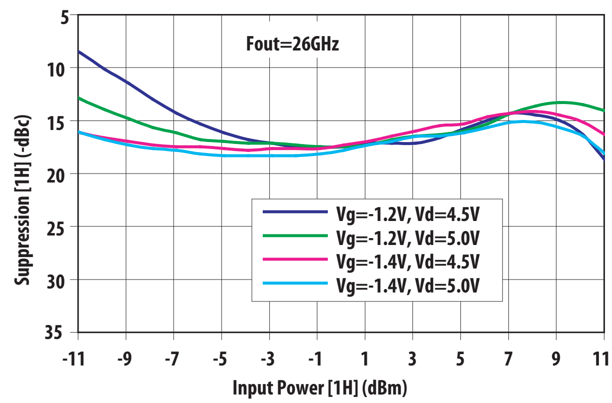


Figure 20 . Fundamental Supp. Vs Input Power @ Fout=26GHz

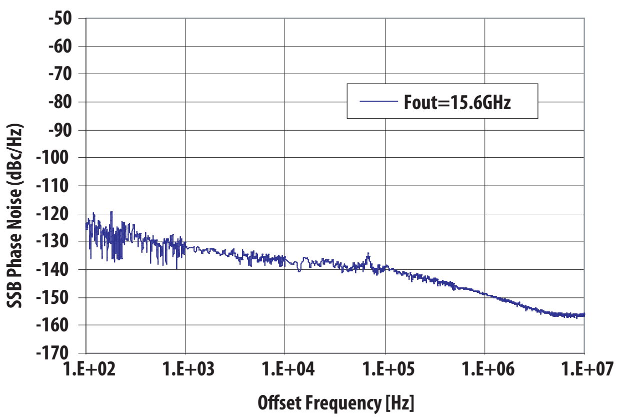


Figure 21. SSB Phase Noise of frequency doubler
(Pin=+2dBm, fout=15.6GHz)

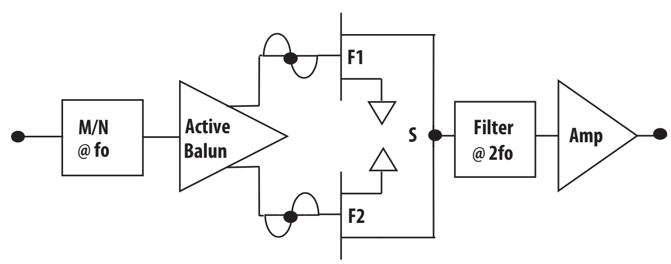


Figure 22. Top Level Schematic of Frequency doubler

Biasing and Operation

The frequency doubler MMIC consists of a balun. The outputs of this balun feed the gates of balanced FETs and the drains are connected to form the single-ended output. This results in fundamental frequency & odd harmonics cancellation. The even harmonic drain currents are in phase and thus add in phase. The input matching network (M/N) is designed to provide good match at fundamental frequencies and produces high impedance mismatch to higher harmonics.

The AMMP-6120 is biased with a single positive drain supply Vdd and a single negative gate supply using separate bypass capacitors. It is normally biased with the drain supply connected to Vd and the gate supply connected to Vg. For most applications it is recommended to use a Vg =-1.2V to -1.4V and Vd=4.5V to 5.0V.

The RF input and output ports are AC coupled thus no DC voltage is present at either port. The ground connection is made via the package base."

The AMMP-6120 performance changes with Drain Voltage (Vd) and Gate bias (Vg) as shown in the previous graphs. Improvements in output power or fundamental suppression performance are possible by optimizing the Vg from -1.2V to -1.4V and/or Vd from 4.5 to 5.0V.

A simplified schematic of the frequency multiplier is shown in figure 22. The active balun circuit and the output amplifier of the circuit are self biased. The Vg negative bias (below pinch off) is only applied to FETs 'F1' and 'F2'. FETs 'F1' and 'F2' have no significant contribution to total drain current therefore Vg cannot be used to set drain current. It should only be used to optimize the output power and fundamental & higher harmonics suppression of the doubler.

Refer to the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Typical Scattering Parameters

Please refer to <http://www.avagotech.com> for typical scattering parameters data.

Package Dimension, PCB Layout and Tape and Reel information

Please refer to Avago Technologies Application Note 5520, AMxP-xxxx production Assembly Process (Land Pattern A).

AMMP-6120 Part Number Ordering Information

Part Number	Devices Per Container	Container
AMMP-6120-BLK	10	Antistatic bag
AMMP-6120-TR1	100	7″ Reel
AMMP-6120-TR2	500	7″ Reel

Names and Contents of the Toxic and Hazardous Substances or Elements in the Products
产品中有毒有害物质或元素的名称及含量

Part Name 部件名称	Toxic and Hazardous Substances or Elements 有毒有害物质或元素					
	Lead (Pb) 铅 (Pb)	Mercury (Hg) 汞（Hg）	Cadmium (Cd) 镉（Cd）	Hexavalent (Cr(VI)) 六价铬（Cr(VI)）	Polybrominated biphenyl (PBB) 多溴联苯（PBB）	Polybrominated diphenylether (PBDE) 多溴二苯醚（PBDE）
100pF capacitor	×	○	○	○	○	○

○: indicates that the content of the toxic and hazardous substance in all the homogeneous materials of the part is below the concentration limit requirement as described in SJ/T 11363-2006.
×: indicates that the content of the toxic and hazardous substance in at least one homogeneous material of the part exceeds the concentration limit requirement as described in SJ/T 11363-2006.
(The enterprise may further explain the technical reasons for the "x" indicated portion in the table in accordance with the actual situations.)

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。
×：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。
（企业可在此处，根据实际情况对上表中打"×" 的技术原因进行进一步说明。）

Note: EU RoHS compliant under exemption clause of "lead in electronic ceramic parts (e.g. piezoelectronic devices)"

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