SY89855U

Precision Low Power Differential LVPECL 4:1 MUX with 1:2 Fanout and Internal Termination

General Description

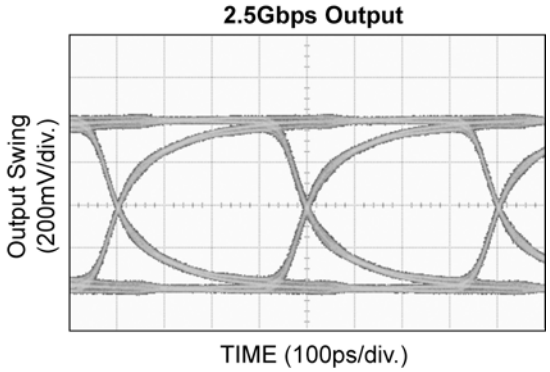
The SY89855U is a 2.5V/3.3V precision, high-speed, 4:1 differential multiplexer with 100K LVPECL (800mV) compatible outputs, capable of handling clocks up to 2.5GHz and data streams up to 2.5Gbps. In addition, a 1:2 fanout buffer provides two copies of the selected inputs.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The result is a clean, stub-free, low-jitter interface solution. The outputs are 800mV LVPECL, (100K temperature compensated) with fast rise/fall times guaranteed to be less than 180ps.

The SY89855U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require higher performance, consider the SY58029U. The SY89855U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

Typical Performance



Precision Edge®

Features

- Select 1 of 4 differential inputs
- Provides two copies of the selected input
- Low power 260mW (V_{CC} = 2.5V)
- Guaranteed AC performance over temperature and voltage:
  - DC-to->2.5Gbps data rate throughput
  - <410ps In-to-Q t_{pd}
  - <180ps t_r / t_f times
- Ultra low-jitter design:
  - <10ps$_{PP}$ total jitter (clock)
  - <1ps$_{RMS}$ random jitter
  - <10ps$_{PP}$ deterministic jitter
  - <0.7ps$_{RMS}$ crosstalk-induced jitter
- Unique, patent-pending input design minimizes crosstalk
- Accepts an input signal as low as 100mV
- Unique patented input termination and VT pin accepts DC- and AC-coupled inputs (CML, LVPECL, LVDS)
- 800mV 100K LVPECL output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to +85°C temperature range
- Available in 32-pin (5mm x 5mm) QFN package

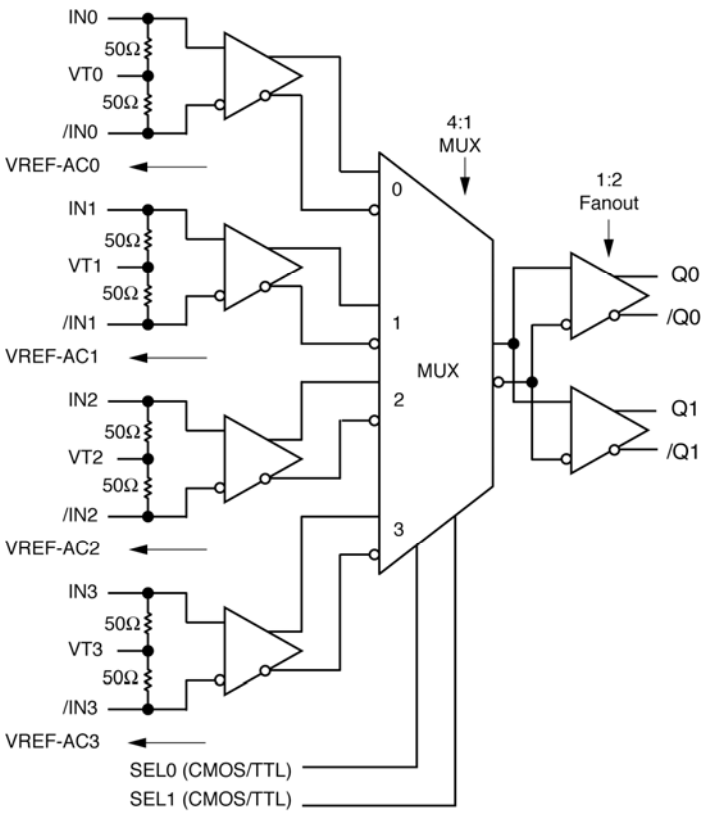
Applications

- Redundant clock and/or data distribution
- All SONET/OC-3 to OC-48 clock/data distribution
- Loopback
- All Fibre Channel applications
- All GigE applications

Markets

- LAN/WAN communication
- Enterprise servers
- ATE
- Test and measurement

Functional Block Diagram



Truth Table

SEL1	SEL0	Q
0	0	IN0 Input Select
0	1	IN1 Input Select
1	0	IN2 Input Select
1	1	IN3 Input Select

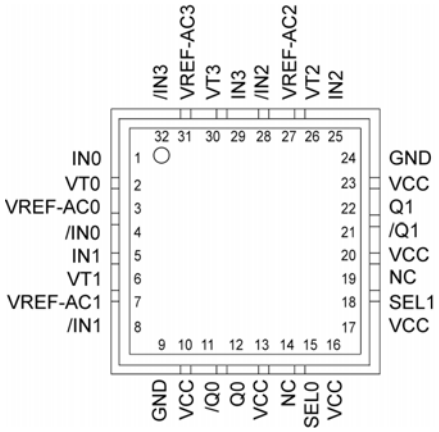
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89855UMG	QFN-32	Industrial	SY89855U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89855UMGTR[2]	QFN-32	Industrial	SY89855U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25ºC, DC Electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1, 4 5, 8 25, 28 29, 32	IN0, /IN0, IN1, /IN1, IN2, /IN2, IN3, /IN3	Differential Input: Each pair accepts AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. If an input is not used, connect one end of the differential pairs to ground through a 1kΩ resistor, and leave the other end to VCC through an 825Ω resistor. Unused VT and VREF-AC pins may also be left floating. Please refer to the “Input Interface Applications” section for more details.
2, 6 26, 30	VT0, VT1 VT2, VT3	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pin provides a center-tap to the termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
15, 18	SEL0, SEL1	This Single-Ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. Input logic threshold is V_{CC}/2. See “Truth Table” for select control.
14, 19	NC	Not connected.
10, 13, 16 17, 20, 23	VCC	Positive Power Supply: Bypass with 0.1µF||0.01µF low ESR capacitors placed as close as possible to each VCC pin.
11, 12 21, 22	/Q0, Q0 /Q1, Q1	Differential Outputs: These 100K-compatible (internally temperature compensated) LVPECL output pairs are copies of the selected input. Unused output pins may be left floating. See “Output Interface” for terminating guidelines.
9, 24	GND, Exposed Pad	Ground: Ground pins and exposed pad must be connected to the most negative potential of the chip.
3 7 27 31	VREF-AC0, VREF-AC1, VREF-AC2, VREF-AC3	Reference Voltage: This reference output is equivalent to V_{CC}–1.2V. It is used for AC-coupled inputs. When interfacing to AC input signals, connect VREF-AC directly to the VT pin and bypass with a 0.01µF low ESR capacitor to VCC. See “Input Interface Applications” section. Maximum sink/source current is ± 1.5mA.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous ..... ±50mA
  Surge ..... ±100mA
Termination Current
  Source or Sink Current on V_T ..... ±100mA
Input Current
  Source or Sink Current on IN, /IN ..... ±50mA
Current (V_{REF-AC})
  Source or Sink Current on V_{REF-AC} ..... ±2mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
  QFN (θ_{JA})
    Still-Air ..... 35°C/W
    500lfpm ..... 28°C/W
  QFN (ψ_{JB})
    Junction-to-Board ..... 16°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V V_{CC} = 3.3V	2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		65	85	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN, /IN-to-V_T)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)	Note 5	V_{CC}– 1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}– 0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN - /IN|	See Figure 1b.	0.2			V
V_{T_IN}	Maximum Input Voltage (IN-to-V_T)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}– 1.3	V_{CC}– 1.2	V_{CC}– 1.1	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still-air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IH} (min) not lower than 1.2V.

LVPECL Output DC Electrical Characteristics[5]

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage (Q, /Q)		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output Low Voltage (Q, /Q)		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 1a.	400	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing (Q, /Q)	See Figure 1b.	800	1600		mV

LVTTL/CMOS DC Electrical Characteristics[5]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC}			75	µA
I_{IL}	Input Low Current	V_{IN} = 0.5V	–300			µA

Notes:

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[6]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

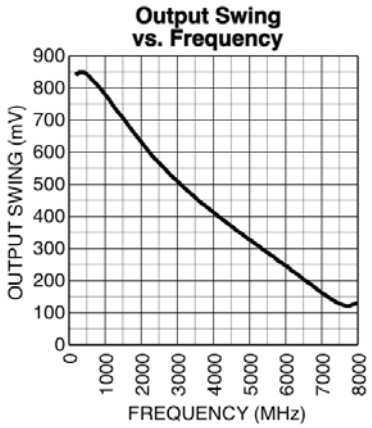
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	2.5			Gbps
		Clock, V_{OUT} > 400mV	2.5			GHz
t_{pd}	Propagation Delay					
	IN-to-Q	V_{IN} > 100mV	210	300	410	ps
	SEL-to-Q		100	300	500	ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			234		fs/°C
t_{SKEW}	Output-to-Output	Note 7		9	20	ps
	Part-to-Part	Note 8			150	ps
t_{JITTER}	Data					
	Random Jitter (RJ)	Note 9			1	ps_{RMS}
	Deterministic Jitter (DJ)	Note 10			10	ps_{PP}
	Clock					
	Cycle-to-Cycle Jitter	Note 11			1	ps_{RMS}
	Total Jitter (TJ)	Note 12			10	ps_{PP}
	Crosstalk-induced Jitter (Adjacent Channel)	Note 13			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	50	100	180	ps

Notes:

6. High frequency AC electricals are guaranteed by design and characterization.
7. Output-to-output skew is measured between outputs under identical input conditions.
8. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
9. Random jitter is measured with a K28.7 character pattern, measured at <f_{MAX}.
10. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}-1 PRBS pattern.
11. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
12. Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
13. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

Typical Operating Characteristics

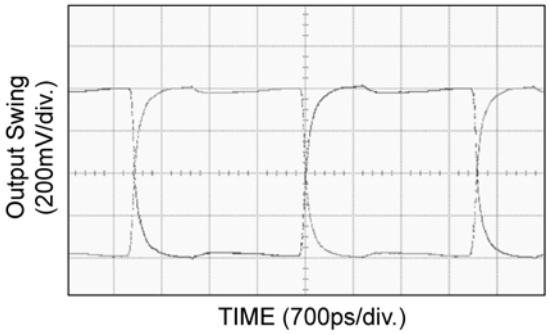
V_{CC} = 2.5V, GND = 0, V_{IN} = 100mV; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.



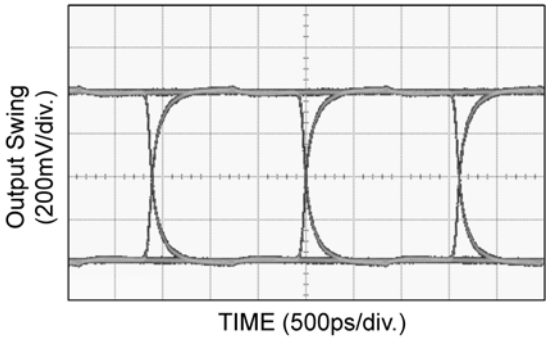
Functional Characteristics

V_{CC} = 3.3V ±10%; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

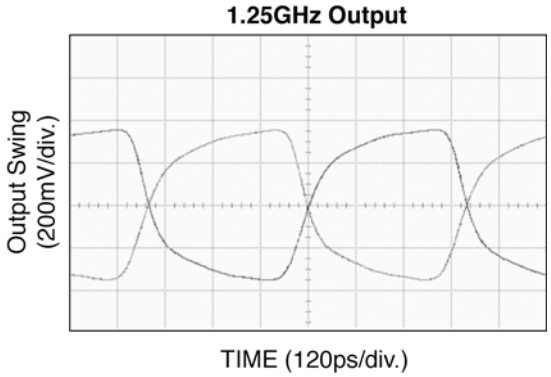
200MHz Output



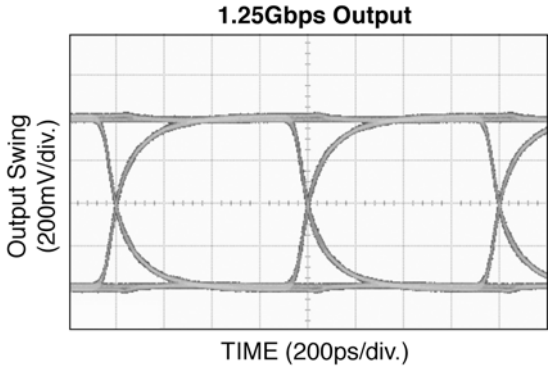
622Mbps Output



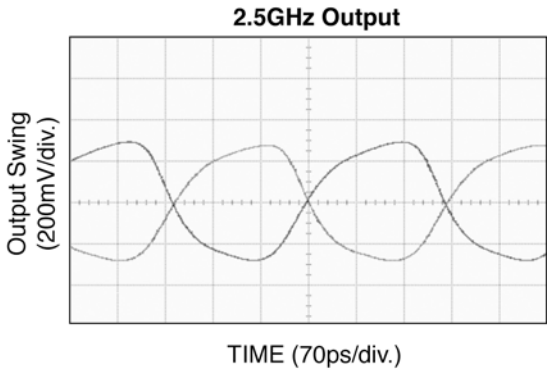
1.25GHz Output



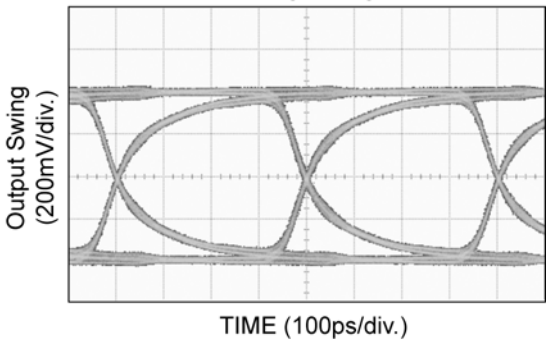
1.25Gbps Output



2.5GHz Output



2.5Gbps Output



Single-Ended and Differential Swings

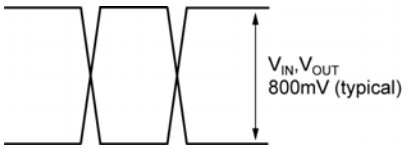


Figure 1a. Single-Ended Voltage Swing

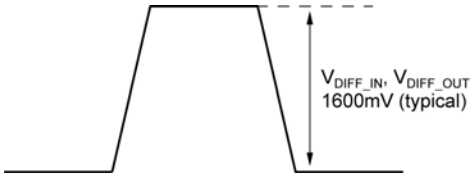
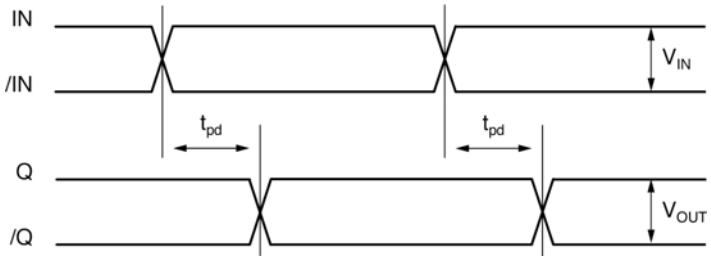
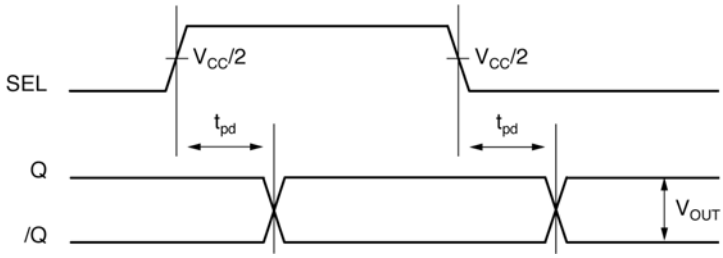


Figure 1b. Differential Voltage Swing

Timing Diagram



IN-to-Q Timing Diagram



SEL-to-Q Timing Diagram

Input and Output Stages

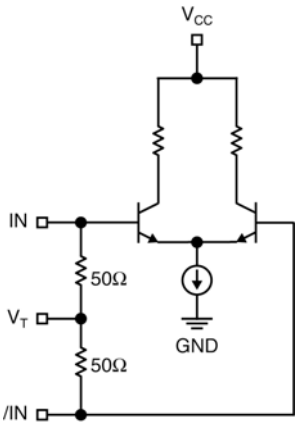


Figure 2a. Simplified Differential Input Stage

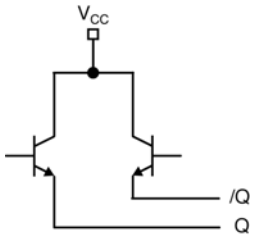


Figure 2b. PECL Output Stage

Input Interface Applications

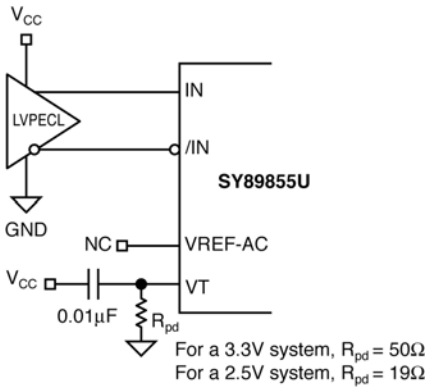


Figure 3a. LVPECL Interface (DC-Coupled)

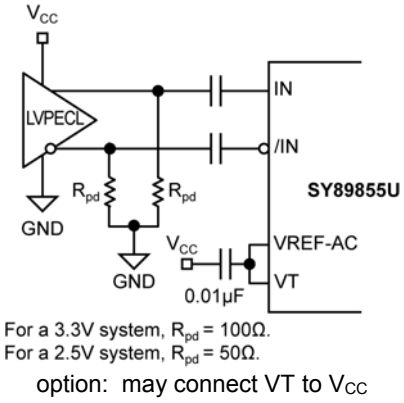


Figure 3b. LVPECL Interface (AC-Coupled)

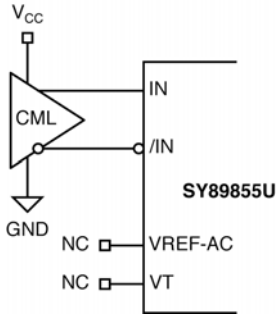


Figure 3c. CML Interface (DC-Coupled)

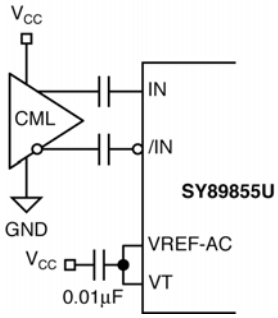


Figure 3d. CML Interface (AC-Coupled)

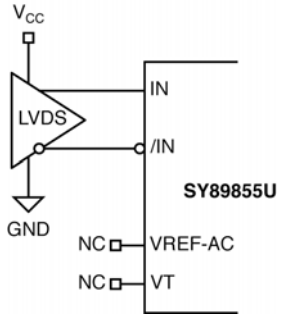
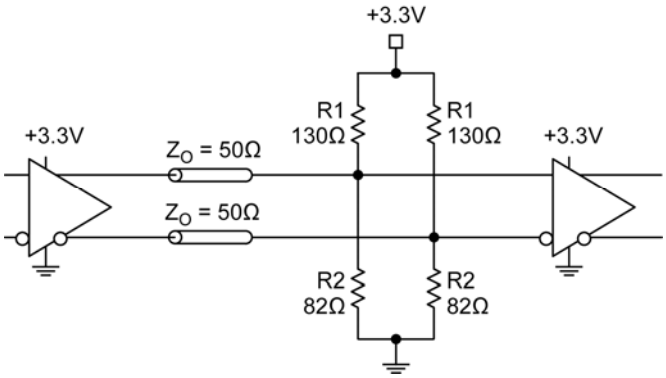


Figure 3e. LVDS Interface

Output Interface Applications

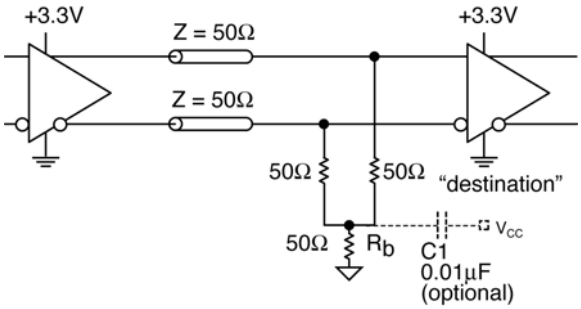
LVPECL has high input impedance, very low output (open emitter) impedance, and small signal swing, which result in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are different techniques for terminating LVPECL outputs: parallel termination thevenin-equivalent, parallel termination (3-resistor), and AC-coupled termination. Unused output pairs may be left floating; however, single-ended outputs must be terminated or balanced.



Note:

For a 2.5V system, R1 = 250Ω, R2 = 62.5Ω.

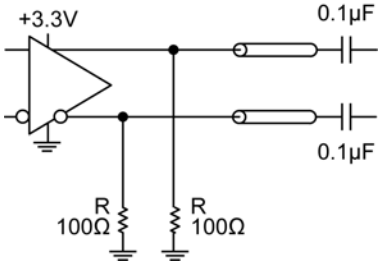
Figure 4a. Parallel Thevenin-Equivalent Termination



Note:

1. For a 2.5V system, Rb = 19Ω.

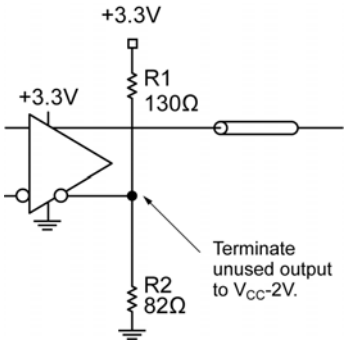
Figure 4b. Parallel Termination (3-Resistor)



Note:

For a 2.5V system, R = 50Ω.

Figure 4c. AC-Coupled Termination



Note:

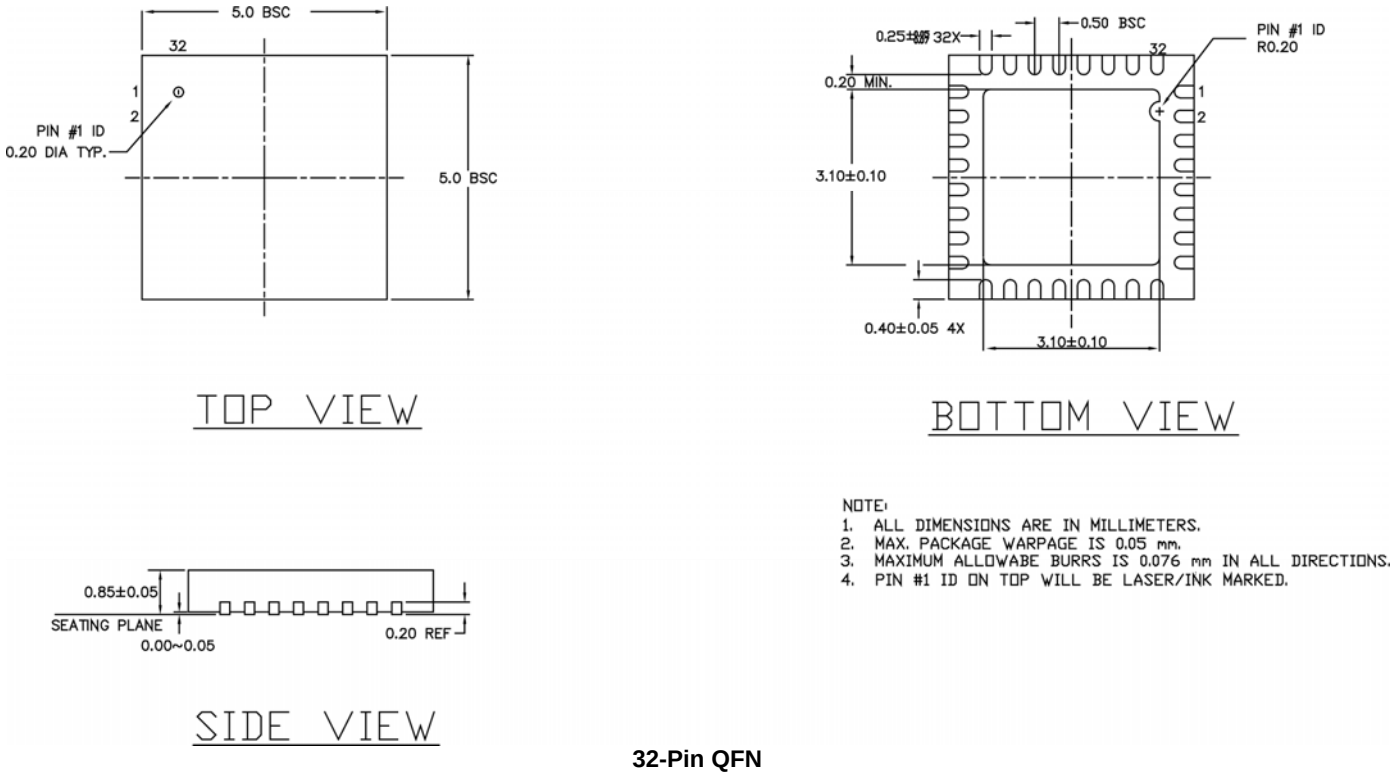
For a 2.5V system, R1 = 250Ω, R2 = 62.5 Ω.

Figure 4d. Parallel Thevenin-Equivalent Termination

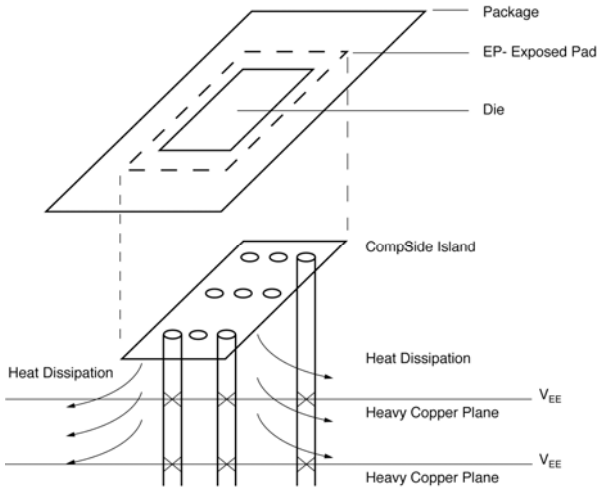
Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY58029U	Ultra Precision Differential LVPECL 4 :1 MUX with 1 :2 Fanout Internal Termination	www.micrel.com/product-info/products/sy58029u.shtml.
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



32-Pin QFN



PCB Thermal Consideration for 32-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Packages Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packed before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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