



## SY88309BL

### 3.3V, 3.2Gbps PECL Limiting Post Amplifier with Wide Signal-Detect Range

#### General Description

The SY88309BL low-power limiting post amplifiers are designed for use in fiber-optic receivers. These devices connect to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88309BL quantizes these signals and output PECL-level waveforms.

The SY88309BL operates from a single +3.3V power supply, over temperatures ranging from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . With their wide bandwidth and high gain, signals with data rates up to 3.2Gbps, and as small as 10mVpp, can be amplified to drive devices with CML or PECL inputs.

It generates a Signal Detect (SD) open-collector TTL output. The SD function is optimized to detect a larger and wider input range, as shown in the characteristic curve on page 6. A programmable signal-detect level set pin ( $\text{SD}_{\text{LVL}}$ ) sets the sensitivity of the input amplitude detection.

SD asserts high if the input amplitude rises above the threshold sets by  $\text{SD}_{\text{LVL}}$  and de-asserts low otherwise. The SD output can be fed back to the EN input to maintain stability. Typically, 3.5dB LOS/SD hysteresis is provided to prevent chattering.

Datasheet and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

#### Features

- Signal Detect circuit optimized to detect a larger and wider input range ( $20\text{mV}_{\text{PP}}-140\text{mV}_{\text{PP}}$ )
- Chatter-free Open-Collector TTL Signal-Detect (SD)
- Single 3.3V power supply
- 155Mbps to 3.2Gbps operation
- Low-noise PECL data outputs
- Programmable SD level set ( $\text{SD}_{\text{LVL}}$ )
- Available in a tiny 10-pin EPAD-MSOP and 16-pin QFN package

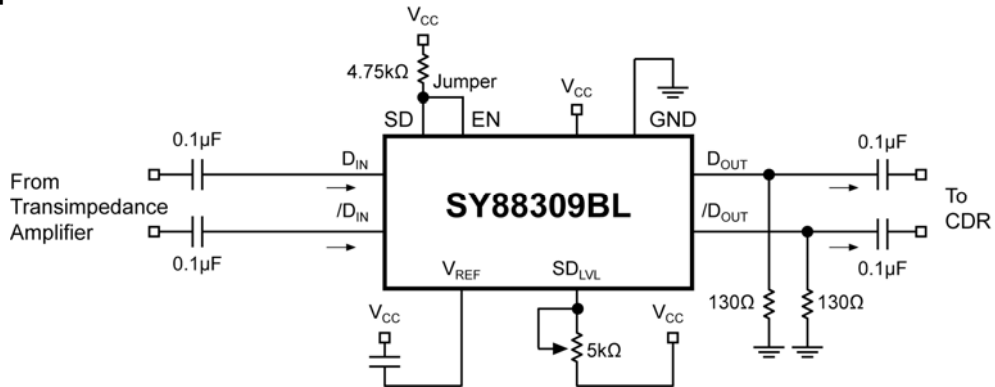
#### Applications

- PON
- Gigabit Ethernet
- 1X and 2X Fibre Channel
- SONET/SDH:OC-3/12/24/48 – STM 1/4/8/16
- High-gain line driver and line receiver

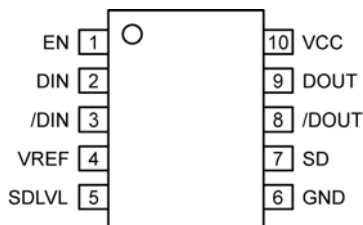
#### Markets

- FTTX
- Optical transceivers
- Datacom/Telecom
- Low-gain TIA interface
- Long-reach FOM

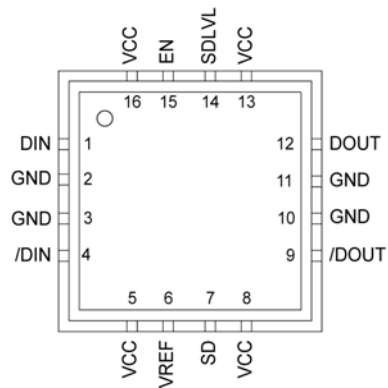
### Typical Application



### Pin Configuration



10-Pin EPAD-MSOP (K10-2)



16-Pin QFN

### Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88309BLEY	K10-2	Industrial	309B with Pb-Free bar line indicator	Matte-Sn Pb-free
SY88309BLEYTR <sup>(1)</sup>	K10-2	Industrial	309B with Pb-Free bar line indicator	Matte-Sn Pb-free
SY88309BLMG	QFN-16	Industrial	309B with Pb-Free bar line indicator	NiPdAu Pb-free
SY88309BLMGTR <sup>(1)</sup>	QFN-16	Industrial	309B with Pb-Free bar line indicator	NiPdAu Pb-free

**Note:**

- 1. Tape and Reel.

## Pin Description

Pin Number (MSOP)	Pin Number (QFN)	Pin Name	Type	Pin Function
1	15	EN	TTL Input: Default is high.	Enable: De-asserts true data output when LOW.
2	1	DIN	Data Input	True data input with 50Ω termination to V <sub>REF</sub> .
3	4	/DIN	Data Input	Complementary data input with 50Ω termination to V <sub>REF</sub> .
4	6	VREF		Reference Voltage: Placing a capacitor here to V <sub>CC</sub> helps stabilize SD <sub>LVL</sub> .
5	14	SDLVL	Input	Signal-detect Level Set: A resistor from this pin to V <sub>CC</sub> sets the threshold for the data input amplitude at which the SD output will be asserted.
6 Exposed Pad	2, 3, 10, 11 Exposed Pad	GND	Ground	Device ground. Exposed pad must be connected to PCB ground plane.
7	7	SD	Open Collector TTL Output	Signal-detect: Asserts high when the data input amplitude rises above the threshold sets by SD <sub>LVL</sub> . For proper operation, install an external 4.75kΩ pull-up resistor at this output.
8	9	/DOUT	PECL Output	Complementary data output.
9	12	DOUT	PECL Output	True data output.
10	5, 8, 13, 16	VCC	Power supply	Positive power supply.

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{CC}$ )	0V to +4.0V
Input Voltage (DIN, /DIN)	0 to $V_{CC}$
Output Current ( $I_{OUT}$ )	
Continuous	$\pm 50$ mA
Surge	$\pm 100$ mA
/EN Voltage	0 to $V_{CC}$
$V_{REF}$ Current	-800 $\mu$ A to +500 $\mu$ A
Voltage	$V_{REF}$ to $V_{CC}$
Lead Temperature (soldering, 20sec.)	260°C
Storage Temperature ( $T_s$ )	-65°C to +150°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{CC}$ )	+3.0V to +3.6V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Junction Temperature ( $T_J$ )	-40°C to +125°C
Junction Thermal Resistance <sup>(3)</sup>	
EPAD-MSOP	
$\theta_{JA}$ (Still-Air)	38°C/W
$\Psi_{JB}$	22°C/W
QFN	
$\theta_{JA}$ (Still-Air)	61°C/W
$\Psi_{JB}$	38°C/W

**DC Electrical Characteristics**

$V_{CC} = 3.0V$  to  $3.6V$ ;  $R_L = 50\Omega$  to  $V_{CC}-2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{CC}$	Power Supply Current	No output load		38	60	mA
$V_{SDLVL}$	$SD_{LVL}$ Voltage		$V_{REF}$		$V_{CC}$	V
$V_{OH}$	PECL Output HIGH Voltage		$V_{CC}-1.085$	$V_{CC}-0.955$	$V_{CC}-0.880$	V
$V_{OL}$	PECL Output LOW Voltage		$V_{CC}-1.830$	$V_{CC}-1.705$	$V_{CC}-1.555$	V
$V_{OFFSET}$	Differential Output Offset				$\pm 160$	mV
$V_{REF}$	Reference Voltage		$V_{CC}-1.48$	$V_{CC}-1.32$	$V_{CC}-1.16$	V
$Z_I$	Single-Ended Input Impedance		40	50	60	$\Omega$

**TTL DC Electrical Characteristics**

$V_{CC} = 3.0V$  to  $3.6V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ .

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	EN Input HIGH Voltage		2.0			V
$V_{IL}$	EN Input LOW Voltage				0.8	V
$I_{IH}$	EN Input HIGH Current	$V_{IN} = 2.7V$ $V_{IN} = V_{CC}$			20 100	$\mu$ A $\mu$ A
$I_{IL}$	EN Input LOW Current	$V_{IN} = 0.5V$	-300			$\mu$ A
$I_{OH}$	SD Output Leakage	$V_{OH} = 3.6V$			100	$\mu$ A
$V_{OL}$	SD Output LOW Level	$I_{OL} = +4mA$			0.5	V

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes the use of a 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.

## AC Electrical Characteristics

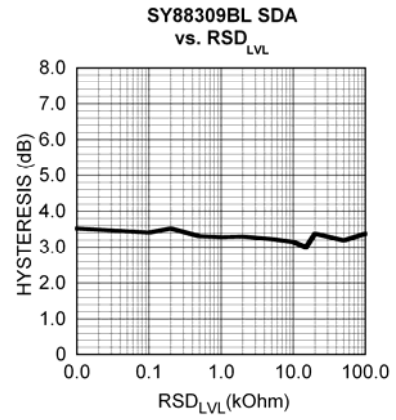
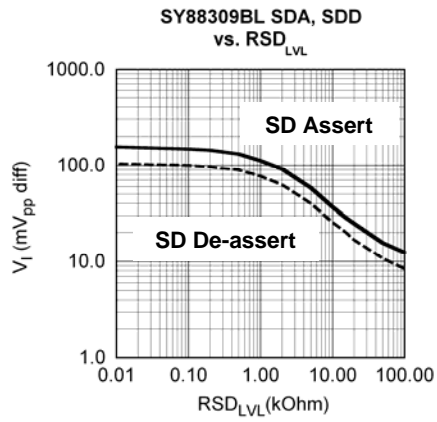
$V_{CC} = 3.0V$  to  $3.6V$ ;  $R_L = 50\Omega$  to  $V_{CC}-2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; typical values at  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ .

Symbol	Parameter	Condition	Min	Typ	Max	Units
$t_r, t_f$	Output Rise/Fall Time (20% to 80%)	Note 4			150	ps
$t_{JITTER}$	Deterministic Random	Note 5 Note 6		15 5		ps <sub>PP</sub> ps <sub>RMS</sub>
$V_{ID}$	Differential Input Voltage Swing	Figure 1	5		1800	mV <sub>PP</sub>
$V_{OD}$	Differential Output Voltage Swing	$V_{ID} \geq 12mV_{PP}$ , Figure 1		1500		mV <sub>PP</sub>
$T_{OFF}$	SD Assert Time			2	10	μs
$T_{ON}$	SD De-assert Time			2	10	μs
$SD_{AL}$	Low SD Assert Level	$R_{SDLVL} = 15k\Omega$ , Note 8		27		mV <sub>PP</sub>
$SD_{DL}$	Low SD De-assert Level	$R_{SDLVL} = 15k\Omega$ , Note 8		18		mV <sub>PP</sub>
$HYS_L$	Low SD/LOS Hysteresis	$R_{SDLVL} = 15k\Omega$ , Note 7		3.4		dB
$SD_{AM}$	Medium SD Assert Level	$R_{SDLVL} = 5k\Omega$ , Note 8		53	80	mV <sub>PP</sub>
$SD_{DM}$	Medium SD De-assert Level	$R_{SDLVL} = 5k\Omega$ , Note 8	21	36		mV <sub>PP</sub>
$HYS_M$	Medium SD/LOS Hysteresis	$R_{SDLVL} = 5k\Omega$ , Note 7	2	3.5	6	dB
$SD_{AH}$	High SD Assert Level	$R_{SDLVL} = 100\Omega$ , Note 8		137	200	mV <sub>PP</sub>
$SD_{DH}$	High SD De-assert Level	$R_{SDLVL} = 100\Omega$ , Note 8	70	94		mV <sub>PP</sub>
$HYS_H$	High SD/LOS Hysteresis	$R_{SDLVL} = 100\Omega$ , Note 7	2	3.5	6	dB
$B_{-3dB}$	3dB Bandwidth			1.8		GHz
$A_{V(Diff)}$	Differential Voltage Gain			42		dB
$S_{21}$	Single-ended Small-Signal Gain		30	36		dB

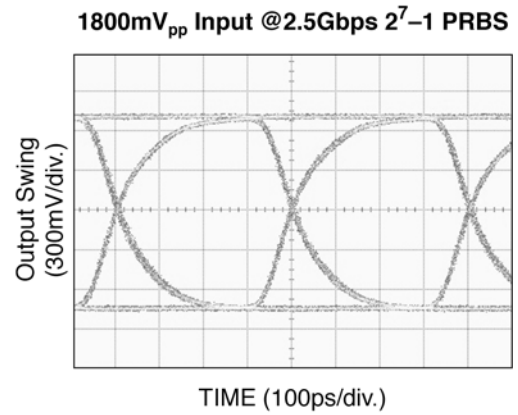
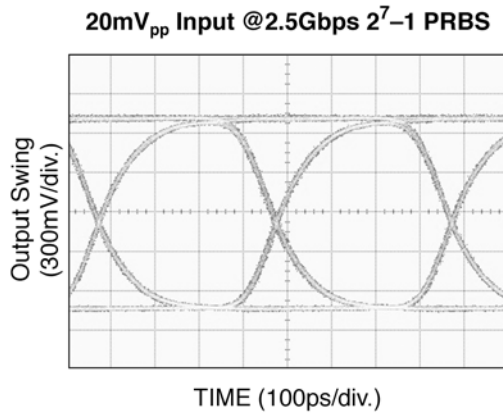
### Notes:

- Amplifier in limiting mode. Input is a 200MHz, 100mVpp square wave.
- Deterministic jitter measured using 3.2Gbps K28.5 pattern,  $V_{ID} = 10mV_{PP}$ .
- Random jitter measured using 3.2Gbps K28.7 pattern,  $V_{ID} = 10mV_{PP}$ .
- This specification defines electrical hysteresis as  $20\log$  (LOS De-assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2, depending upon the level of received optical power and ROSA characteristics. Based upon that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-6dB, shown in the AC characteristics table, will be 1dB-3dB Optical Hysteresis.
- See "Typical Operating Characteristics" for a graph showing how to choose a particular  $R_{SDLVL}$  for a particular SD assert and its associated de-assert amplitude.

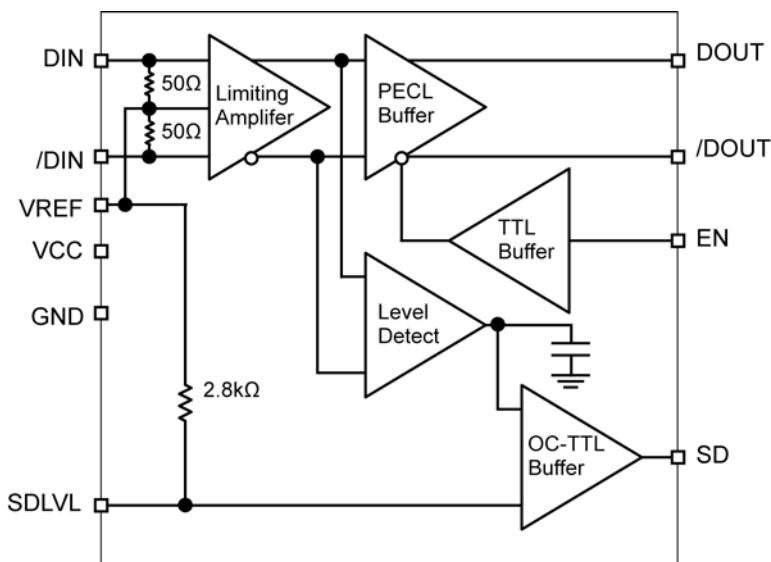
## Typical Operating Characteristics



## Functional Characteristics



## Functional Block Diagram



### Detailed Description

The SY88309BL low-power limiting post amplifiers operate from a single +3.3V power supply, over temperatures from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Signals with data rates up to 3.2Gbps and as small as 10mVpp can be amplified. Figure 1 shows the allowed input voltage swing. The SY88309BL generates an SD output allowing feedback to EN for output stability.  $\text{SD}_{\text{LVL}}$  sets the sensitivity of the input amplitude detection.

#### Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier allows signals as small as 10mVpp to be amplified. The input amplifier also allows input signals as large as 1800mVpp. Input signals below 12mVpp are linearly amplified with a typical 42dB differential voltage gain. Since it is a limiting amplifier, these devices output typically 1500mVpp voltage-limited waveforms for input signals greater than 12mVpp. Applications requiring the SY88309BL to operate with strong signals should have the upstream TIA placed as close as possible to the devices' input pins. This ensures the best performance of the device.

#### Output Buffer

The SY88309BL PECL output buffers are designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to  $V_{\text{CC}}-2\text{V}$  for each output pin provides this. Figure 3 shows a simplified schematic of the output

stage.

#### Signal Detect

The SY88309BL generates a chatter-free SD open-collector TTL output, as shown in Figure 4. SD asserts high if the input amplitude rises above the threshold sets by  $\text{SD}_{\text{LVL}}$  and de-asserts low otherwise. The SD output can be fed back to the EN input to maintain stability

#### Signal-Detect Level Set

Programmable SD level set pin ( $\text{SD}_{\text{LVL}}$ ) sets the threshold of the input amplitude detection. Connecting an external resistor between  $V_{\text{CC}}$  and  $\text{SD}_{\text{LVL}}$  set the voltage at  $\text{SD}_{\text{LVL}}$ . This voltage ranges from  $V_{\text{CC}}$  to  $V_{\text{REF}}$ . The external resistor creates a voltage divider between  $V_{\text{CC}}$  and  $V_{\text{REF}}$ , as shown in Figure 5.

#### Hysteresis

The SY88309BL typically provide 3.5dB SD electrical hysteresis. By definition, a power ratio measured in dB is  $10\log(\text{power ratio})$ . Power is calculated as  $V_{\text{IN}}^2/R$  for an electrical signal. Hence, the same ratio can be stated as  $20\log(\text{voltage ratio})$ . While in linear mode, the electrical voltage input changes linearly with the optical power and therefore, the ratios change linearly. Thus, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. Since the SY88309BL are electrical devices, this data sheet refers to hysteresis in electrical terms. With 3.5dB SD hysteresis, a voltage factor of 1.5 is required to assert or de-assert SD.

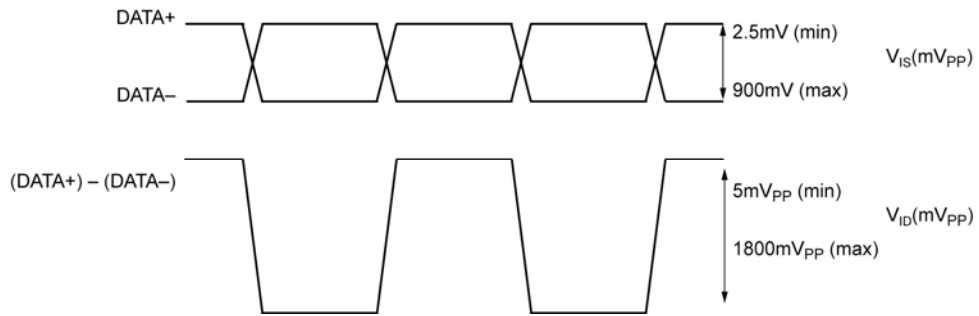


Figure 1.  $V_{IS}$  and  $V_{ID}$

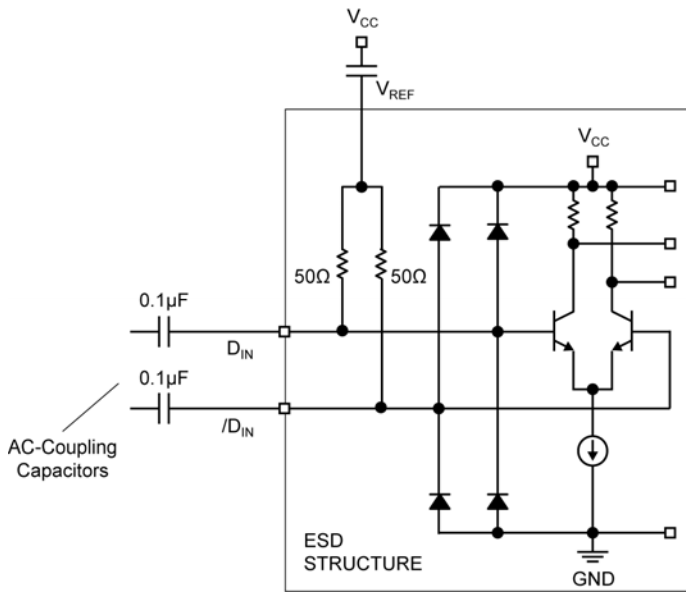


Figure 2. Input Structure

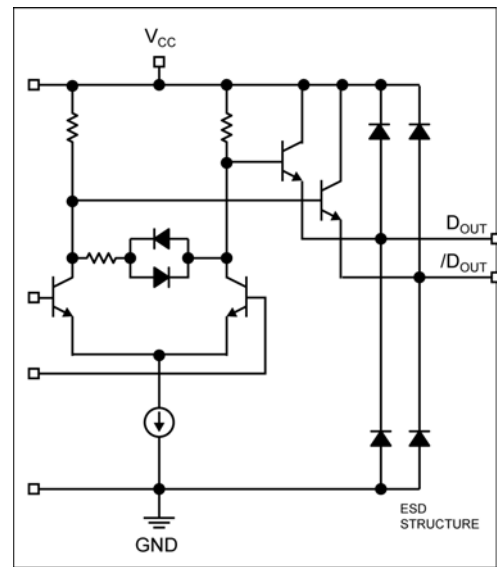


Figure 3. Output Structure

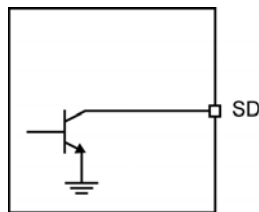


Figure 4. SD Output Structure

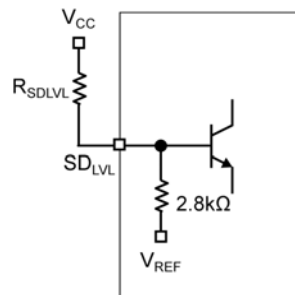
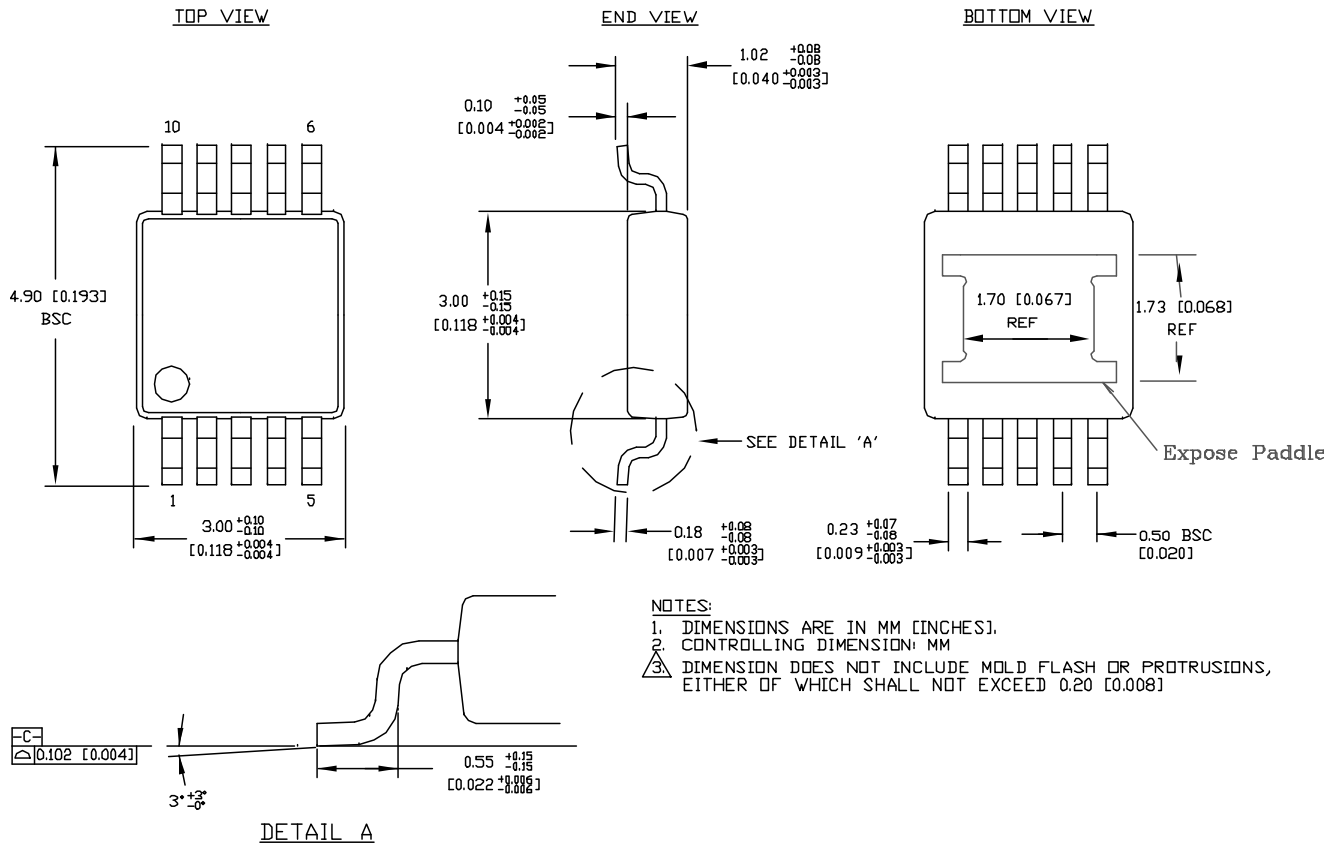


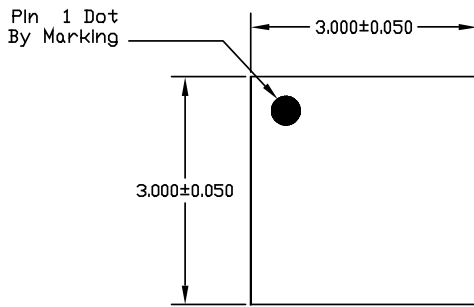
Figure 5.  $SD_{LVL}$  Setting Circuit



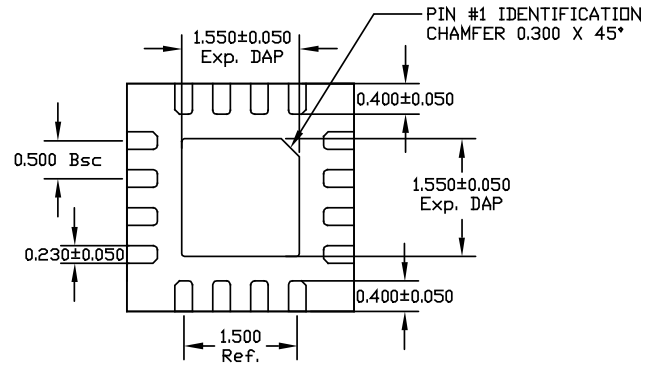
**Package Information**



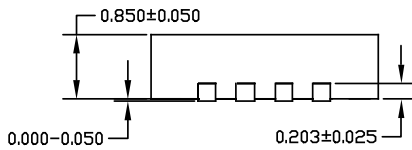
**10-Pin EPAD-MSOP (K10-2)**



TOP VIEW



BOTTOM VIEW

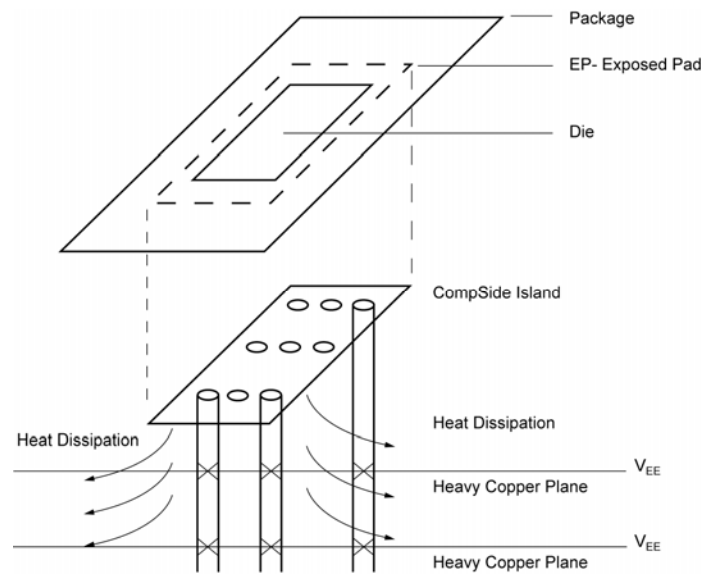


SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

16-Pin QFN



**PCB Thermal Consideration for 16-Pin QFN Package  
(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management, solder void has to be less than 50% of the epad area.

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**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**  
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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