

QUINT DIFFERENTIAL LINE RECEIVER

FEATURES

- 450ps max. Propagation Delay
- Extended 100E VEE range of -4.2V to -5.5V
- VBB output for single-ended reception
- Fully compatible with industry standard 10KH, 100K I/O levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E116
- Available in 28-pin PLCC package

BLOCK DIAGRAM





DESCRIPTION

The SY10/100E116 are quint differential line receivers designed for use in new, high-performance ECL systems. These devices have emitter-follower outputs and an internally generated reference supply (VBB) for single-ended reception.

Active current sources combined with Micrel's ASSET[™] technology provide the receivers with excellent common mode noise rejection.

The receiver design features clamp circuitry to cause a defined output state if both the inverting and non-inverting inputs are left open; in this case the Q output goes LOW, while the \overline{Q} output goes HIGH.

If both inverting and non-inverting inputs are at equal potential, the receiver does *not* go to a defined state, but rather shares current in normal differential amplifier fashion, producing output voltage levels midway between HIGH and LOW.

The VBB output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using VBB for this purpose, it is recommended that VBB is decoupled to VCC via a 0.01 μF capacitor.

For higher bandwidth, please refer to the SY10/100E416 device.

PIN NAMES

Pin	Function						
D0, \overline{D} 0-D4, \overline{D} 4	Differential Input Pairs						
Q0, \overline{Q} 0-Q4, \overline{Q} 4	Differential Output Pairs						
VBB	Reference Voltage Output						
Vcco	Vcc to Output						

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E116JI	J28-1	Industrial	SY10E116JI	Sn-Pb
SY10E116JITR ⁽²⁾	J28-1	Industrial	SY10E116JI	Sn-Pb
SY100E116JI	J28-1	Industrial	SY100E116JI	Sn-Pb
SY100E116JITR ⁽²⁾	J28-1	Industrial	SY100E116JI	Sn-Pb
SY10E116JC	J28-1	Commercial	SY10E116JC	Sn-Pb
SY10E116JCTR ⁽²⁾	J28-1	Commercial	SY10E116JC	Sn-Pb
SY100E116JC	J28-1	Commercial	SY100E116JC	Sn-Pb
SY100E116JCTR ⁽²⁾	J28-1	Commercial	SY100E116JC	Sn-Pb
SY10E116JY ⁽³⁾	J28-1	Industrial	SY10E116JY with Pb-Free bar-line indicator	Matte-Sn
SY10E116JYTR ^(2, 3)	J28-1	Industrial	SY10E116JY with Pb-Free bar-line indicator	Matte-Sn
SY100E116JY ⁽³⁾	J28-1	Industrial	SY100E116JY with Pb-Free bar-line indicator	Matte-Sn
SY100E116JYTR ^(2, 3)	J28-1	Industrial	SY100E116JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^{\circ}C$, DC Electricals only.

2. Tape and Reel.

3. Pb-Free package is recommended for new designs.

LOGIC EQUATION

Qn = Dn

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DC ELECTRICAL CHARACTERISTICS

VEE = VEE(Min.) to VEE(Max.); VCC = VCCO = GND

		TA = −40°C			TA = 0°C			TA = +25°C			TA = +85°C			
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
VBB	Output Reference													V
	Voltage 10E	-1.43	—	-1.30	-1.38	—	-1.27	-1.35	—	-1.25	-1.31	—	-1.19	
	100E	-1.43	_	-1.26	-1.38	—	-1.26	-1.38		-1.26	-1.38	_	-1.26	
Іін	Input HIGH Current			200		_	200			200			200	μA
IEE	Power Supply Current													mA
	10E	—	29	35	—	29	35	—	29	35	—	29	35	
	100E	—	29	35	—	29	35	—	29	35	—	33	40	
VPP (DC)	Input Sensitivity ⁽¹⁾	150		_	150	—	_	150		_	150		-	mV
VCMR	Common Mode Range ⁽²⁾	-2.0	_	-0.6	-2.0	_	-0.6	-2.0		-0.6	-2.0	_	-0.6	V

Notes:

1. VPP is the minimum differential input voltage required to assure full ECL levels are present at the outputs.

2. VCMR is referenced to the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the VCMR range and the input swing is greater than VPP (min.) and <1V.

AC ELECTRICAL CHARACTERISTICS

VEE = VEE(Min.) to VEE(Max.); VCC = VCCO = GND

		TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			
Symbol	Parameter	Min.	Тур.	Max.	Unit									
tPD	Propagation Delay to Output D D (S.E.)	150 150	300 300	500 550	200 150	300 300	450 500	200 150	300 300	450 500	200 150	300 300	450 500	ps
VPP (DC)	Input Sensitivity ⁽¹⁾	150	—	150	150	—	—	150	_	—	150	—	—	mV
tskew	Within-Device Skew ⁽²⁾ Dn to Qn, $\overline{Q}n$	—	50	—	—	50	—	—	50	—	—	50	—	ps
tskew	Duty Cycle Skew ⁽³⁾ tPLH – tPHL	-	±10	-	—	±10	—	—	±10	—	—	±10	-	ps
tr tf	Rise/Fall Time 20% to 80%	250	375	625	275	375	575	275	375	575	275	375	575	ps

Notes:

1. Minimum input swing for which AC parameters are guaranteed.

2. Within-device skew is defined as identical transitions on similar paths through a device.

3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

28-PIN PLCC (J28-1)



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