

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device class V criteria. Add RHA data. Editorial changes throughout - jak.	98-05-29	Monica L. Poelking
B	Add device type 02. Add vendor CAGE F8859. Add case outlines X and Z. Add table II, delta limits. Add radiation features for device type 01. Update boilerplate to MIL-PRF-38535 requirements. - jak	02-09-24	Thomas M. Hess
C	Change lead temperature for case outline X in section 1.3. Add radiation features for device type 02 in section 1.5. Update the boilerplate to include radiation hardness assured requirements for device type 02. Editorial changes throughout. - jak	04-12-14	Thomas M. Hess
D	Update radiation features in section 1.5. Add SEP test table IB and paragraph 4.4.4.2. - jak	11-05-19	David J. Corbett

REV																			
SHEET																			
REV	D	D	D	D	D														
SHEET	15	16	17	18	19														
REV STATUS OF SHEETS	REV			D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14		

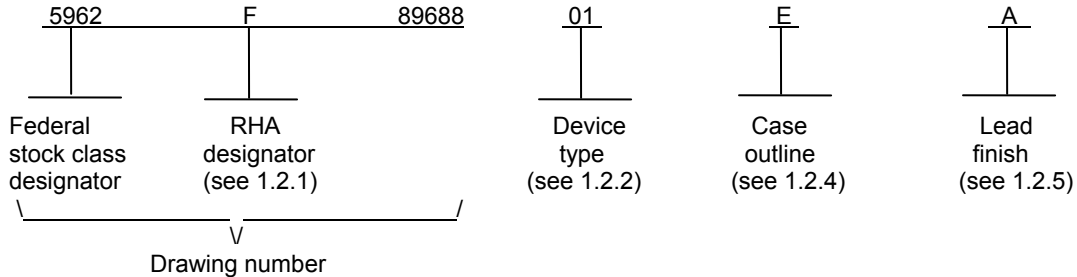
PMIC N/A	PREPARED BY Marcia B. Kelleher	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.dscclia.mil																	
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Ray Monnin	MICROCIRCUITS, DIGITAL, ADVANCED CMOS, QUAD 2-INPUT MULTIPLEXER, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON SIZE A CAGE CODE 67268 5962-89688 SHEET 1 OF 19																	
	APPROVED BY Michael A. Frye																		
	DRAWING APPROVAL DATE 89-06-16																		
	REVISION LEVEL D																		

1. SCOPE

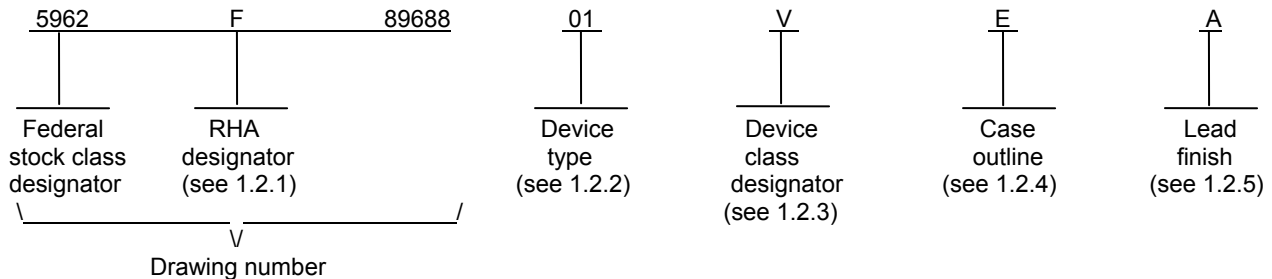
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ACT157	Quad 2-input multiplexer, TTL compatible inputs
02	54ACT157	Quad 2-input multiplexer, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

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1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
Z	GDFP1-G16	16	Flat pack with gullwing
X	CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}).....	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN}).....	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range (V_{OUT}).....	-0.5 V dc to $V_{CC} + 0.5$ V dc
Clamp diode current (I_{IK}, I_{OK}).....	± 20 mA
DC output current (I_{OUT}) (per pin).....	± 50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) (per pin).....	± 100 mA
Maximum power dissipation (P_D).....	500 mW
Storage temperature range (T_{STG}).....	-65°C to +150°C
Lead temperature (soldering, 10 seconds):	
Case outline X.....	+260°C
All other case outlines except case X.....	+300°C
Thermal resistance, junction-to-case (θ_{JC}).....	See MIL-STD-1835
Junction temperature (T_J).....	+175°C <u>4/</u>

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC}).....	4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}).....	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT}).....	+0.0 V dc to V_{CC}
Case operating temperature range (T_C).....	-55°C to +125°C
Input rise or fall times ($V_{CC} = 4.5$ V to 5.5 V) ($\Delta t/\Delta V$).....	0 to 8 ns/V

1.5 Radiation features.

Device type 01:

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s).....	100 krad (Si)
Single event phenomenon (SEP):	
effective LET, no SEL (see 4.4.4.2).....	≤ 100 MeV-cm ² /mg
effective LET, no SEU (see 4.4.4.2).....	≤ 100 MeV-cm ² /mg

Device type 02:

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s).....	300 krad (Si)
Single event phenomenon (SEP):	
effective LET, no SEL (see 4.4.4.2).....	≤ 93 MeV-cm ² /mg <u>5/</u>
effective LET, no SEU (see 4.4.4.2).....	≤ 93 MeV-cm ² /mg <u>5/</u>

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ These limits were obtained during technology characterization and qualification, and are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD-20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

ASTM INTERNATIONAL (ASTM)

ASTM F1192- Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at <http://www.astm.org/> or from ASTM International, P. O. Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

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3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime 's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 39 (see MIL-PRF-38535, appendix A).

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TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and <u>4/</u> device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit
						Min	Max	
Positive input clamp voltage 3022	V _{IC+}	For input under test, I _{IN} = 1.0 mA	All V	0.0 V	1	0.4	1.5	V
	<u>6/ 7/</u>	M, D, P, L, R	01 Q,V	0.0 V	1	0.4	1.5	
Negative input clamp voltage 3022	V _{IC-}	For input under test, I _{IN} = -1.0 mA	All V	Open	1	-0.4	-1.5	V
	<u>6/ 7/</u>	M, D, P, L, R	01 Q,V	Open	1	-0.4	-1.5	
High level output voltage 3006	V _{OH} <u>6/ 7/ 8/</u>	V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V I _{OH} = -50 μA	All	4.5 V	1, 2, 3	4.4		V
			All	5.5 V		5.4		
		M, D, P, L, R	01 Q,V	5.5 V	1	5.4		
		V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V I _{OH} = -24 mA	All	4.5 V	1, 2, 3	3.7		
			M, D, P, L, R	01 Q,V	4.5 V	1	3.7	
			All	5.5 V	1, 2, 3	4.7		
		V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V I _{OH} = -50 mA	All	5.5 V	1, 2, 3	3.85		
			M, D, P, L, R	01 Q,V	5.5 V	1	3.85	
Low level output voltage 3007	V _{OL} <u>6/ 7/ 8/</u>	V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V I _{OL} = 50 μA	All	4.5 V	1, 2, 3		0.1	V
			All	5.5 V			0.1	
		M, D, P, L, R	01 Q,V	5.5 V	1		0.1	
		V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V I _{OL} = 24 mA	All	4.5 V	1, 2, 3		0.5	
			M, D, P, L, R	01 Q,V	4.5 V	1		
			All	5.5 V	1, 2, 3		0.5	
		V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V I _{OL} = 50 mA	All	5.5 V	1, 2, 3		1.65	
			M, D, P, L, R	01 Q,V	5.5 V	1		

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and <u>4/</u> device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit	
						Min	Max		
High level input voltage	V _{IH} <u>9/</u>		All All	4.5 V	1, 2, 3	2.0		V	
				5.5 V		2.0			
Low level input voltage	V _{IL} <u>9/</u>		All All	4.5 V	1, 2, 3		0.8	V	
				5.5 V			0.8		
Input leakage current high 3010	I _{IH} <u>6/ 7/</u>	V _{IN} = 5.5 V	All All	5.5 V	1, 2, 3		1.0	μA	
			M, D, P, L, R	01 Q,V	5.5 V	1	0.1		
Input leakage current low 3009	I _{IL} <u>6/ 7/</u>	V _{IN} = 0.0 V	All All	5.5 V	1, 2, 3		-1.0	μA	
			M, D, P, L, R	01 Q,V	5.5 V	1	-0.1		
Quiescent supply current delta, TTL input levels 3005	ΔI _{CC} <u>6/ 7/ 10/</u>	For input under test, V _{IN} = V _{CC} - 2.1 V For all other inputs, V _{IN} = V _{CC} or GND	All All	5.5 V	1, 2, 3		1.6	mA	
			M, D	01	1	1.6			
			P, L, R	Q,V		3.5			
Quiescent supply current high 3005	I _{CC} H <u>6/ 7/</u>	V _{IN} = V _{CC} or GND I _{OUT} = 0.0 V	01 All	5.5 V	1, 2, 3		80	μA	
			02 All		1	4.0			
					2, 3	80			
			M		01	1	100	mA	
			D		Q,V		1.0		
			P, L, R			3.5			
			M, D, P, L, R, F <u>11/</u>		02 Q,V		50	μA	
Quiescent supply current low 3005	I _{CC} L <u>6/ 7/</u>	V _{IN} = V _{CC} or GND I _{OUT} = 0.0 V	01 All	5.5 V	1, 2, 3		80	μA	
			02 All		1	4.0			
					2, 3	80			
			M		01	1	100	mA	
			D		Q,V		1.0		
			P, L, R			3.5			
			M, D, P, L, R, F <u>11/</u>		02 Q,V		50	μA	
Input capacitance 3012	C _{IN}	See 4.4.1c T _C = +25°C	All All	GND	4		8.0	pF	
Power dissipation capacitance	C _{PD} <u>12/</u>	See 4.4.1c T _C = +25°C, f = 1 MHz	All All	5.0 V	4		70.0	pF	
Functional tests 3014	<u>6/ 7/ 13/</u>	See 4.4.1b, V _{IN} = V _{IH} or V _{IL} Verify output V _{OUT}	All All	4.5 V	7, 8	L	H		
			M, D, P, L, R		01 Q, V	7	L		H
			All All		5.5 V	7, 8	L		H

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and <u>4/</u> device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit	
						Min	Max		
Propagation delay time, S to Zn, 3003	t _{PHL1} <u>6/ 7/ 14/</u>	C _L = 50 pF R _L = 500Ω See figure 4	M, D, P, L, R	All All	4.5 V	9	1.0	9.5	ns
				01 Q,V		9	1.0	9.5	
				All All		10, 11	1.0	11.5	
	t _{PLH1} <u>6/ 7/ 14/</u>	C _L = 50 pF R _L = 500Ω See figure 4	M, D, P, L, R	All All		9	1.0	9.0	
				01 Q,V		9	1.0	9.0	
				All All		10, 11	1.0	11.5	
Propagation delay time, E to Zn, 3003	t _{PHL2} <u>6/ 7/ 14/</u>	C _L = 50 pF R _L = 500Ω See figure 4	M, D, P, L, R	All All	4.5 V	9	1.0	8.5	ns
				01 Q,V		9	1.0	8.5	
				All All		10, 11	1.0	10.0	
	t _{PLH2} <u>6/ 7/ 14/</u>	C _L = 50 pF R _L = 500Ω See figure 4	M, D, P, L, R	All All		9	1.0	10.0	
				01 Q,V		9	1.0	10.0	
				All All		10, 11	1.0	12.0	
Propagation delay time, In to Zn 3003	t _{PHL3} <u>6/ 7/ 14/</u>	C _L = 50 pF R _L = 500Ω See figure 4	M, D, P, L, R	01 All	4.5 V	9	1.0	7.5	ns
				01 Q,V		9	1.0	7.5	
				01 All		10, 11	1.0	9.0	
				02 All		9	1.0	9.0	
						10, 11	1.0	11.0	
	t _{PLH3} <u>6/ 7/ 14/</u>	C _L = 50 pF R _L = 500Ω See figure 4	M, D, P, L, R	01 All	4.5 V	9	1.0	7.5	ns
				01 Q,V		9	1.0	7.5	
				01 All		10, 11	1.0	9.0	
				02 All		9	1.0	9.0	
						10, 11	1.0	11.0	

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TABLE IA. Electrical performance characteristics - Continued.

- 1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table IA herein.
- 2/ Each input/output, as applicable shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:
 - a. V_{IC} (pos) tests, the GND terminal can be open. $T_C = +25^\circ\text{C}$.
 - b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. $T_C = +25^\circ\text{C}$.
 - c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.
- 3/ RHA parts for device type 01 are tested at all levels M, D, P, L, and R of irradiation. Pre and post irradiation values are identical unless otherwise specified in table IA.

RHA parts for device type 02 meet all levels M, D, P, L, R, and F of irradiation. However, these parts are only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table IA.
- 4/ The word "All" in the device type and device class column, means limits for all device types and classes.
- 5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.
- 6/ RHA samples do not have to be tested at -55°C and $+125^\circ\text{C}$ prior to irradiation.
- 7/ When performing postirradiation electrical measurements for RHA level, $T_A = +25^\circ\text{C}$. Limits shown are guaranteed at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$.
- 8/ The V_{OH} and V_{OL} tests shall be tested at $V_{CC} = 4.5\text{ V}$. The V_{OH} and V_{OL} tests are guaranteed, if not tested, for $V_{CC} = 5.5\text{ V}$. Limits shown apply to operation at $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$. Transmission driving tests are performed at $V_{CC} = 5.5\text{ V}$ with a 2 ms duration maximum. Transmission driving tests may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = 2.0\text{ V}$ or 0.8 V .
- 9/ The V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} and V_{OL} tests.
- 10/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1\text{ V}$ (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times ΔI_{CC} maximum limits; and the preferred method and limits are guaranteed.
- 11/ The maximum limit for this parameter at 100 krad (Si) is $4\ \mu\text{A}$.
- 12/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$ and the dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P_D and I_S , n is the number of device inputs at TTL levels, f is the frequency of the input signal, and d is the duty cycle of the input signal.
- 13/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, $V_{IL} = 0.4\text{ V}$ and $V_{IH} = 2.4\text{ V}$. For outputs, $L \leq 0.8\text{ V}$, $H \geq 2.0\text{ V}$.
- 14/ AC limits at $V_{CC} = 5.5\text{ V}$ are equal to the limits at $V_{CC} = 4.5\text{ V}$ and guaranteed by testing at $V_{CC} = 4.5\text{ V}$. Minimum ac limits for $V_{CC} = 5.5\text{ V}$ are 1.0 ns and guaranteed by guardbanding the $V_{CC} = 4.5\text{ V}$ minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

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TABLE IB. SEP test limits. 1/ 2/

Device type	$V_{CC} = 4.5 \text{ V}$ <u>3/</u>		Bias for latch-up test $V_{CC} = 5.5 \text{ V}$ no latch-up $\text{LET} = \text{4/ 5/}$ [MeV/(mg/cm ²)]
	Effective LET no upsets [MeV/(mg/cm ²)]	Maximum device cross section	
01	$\text{LET} \leq 100$ <u>7/</u>	$6 \times 10^{-9} \text{ cm}^2/\text{bit}$ <u>6/</u>	≤ 100
02	$\text{LET} \leq 93$ <u>7/</u>	Not available	≤ 93

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Tested for upsets at operating temperature, $T_A = +25^\circ\text{C} \pm 10^\circ\text{C}$.

4/ Tested at operating temperature, $T_A = +125^\circ\text{C} \pm 10^\circ\text{C}$ for latch-up.

5/ Tested to a $\text{LET} \leq 100 \text{ MeV}/(\text{mg}/\text{cm}^2)$ for device type 01 and $\leq 93 \text{ MeV}/(\text{mg}/\text{cm}^2)$ for device type 02 with no latch-up (SEL).

6/ The bit error cross section is established from a "hard" D flip-flop that is based on the Weibull distribution from SEU testing, and is performed on the Standard Evaluation Circuit (SEC).

7/ Tested to a $\text{LET} \leq 100 \text{ MeV}/(\text{mg}/\text{cm}^2)$ for device type 01 and to a $\text{LET} \leq 93 \text{ MeV}/(\text{mg}/\text{cm}^2)$ for device type 02 with no single event upsets (SEU).

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Device types	01, 02	
Case outlines	E, F, X, and Z	2
Terminal number	Terminal symbol	
1	S	NC
2	I0a	S
3	I1a	I0a
4	Za	I1a
5	I0b	Za
6	I1b	NC
7	Zb	I0b
8	GND	I1b
9	Zd	Zb
10	I1d	GND
11	I0d	NC
12	Zc	Zd
13	I1c	I1d
14	I0c	I0d
15	\bar{E}	Zc
16	V _{CC}	NC
17	---	I1c
18	---	I0c
19	---	\bar{E}
20	---	V _{CC}

NC = no internal connection

Terminal descriptions	
Terminal symbol	Description
S	Select input
\bar{E}	Enable input (active low)
I0n (n = a, b, c, d)	Data inputs from source 0
I1n (n = a, b, c, d)	Data inputs from source 1
Zn (n = a, b, c, d)	Outputs

FIGURE 1. Terminal connections.

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Inputs				Outputs
\bar{E}	S	I0n	I1n	Zn
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Irrelevant

FIGURE 2. Truth table.

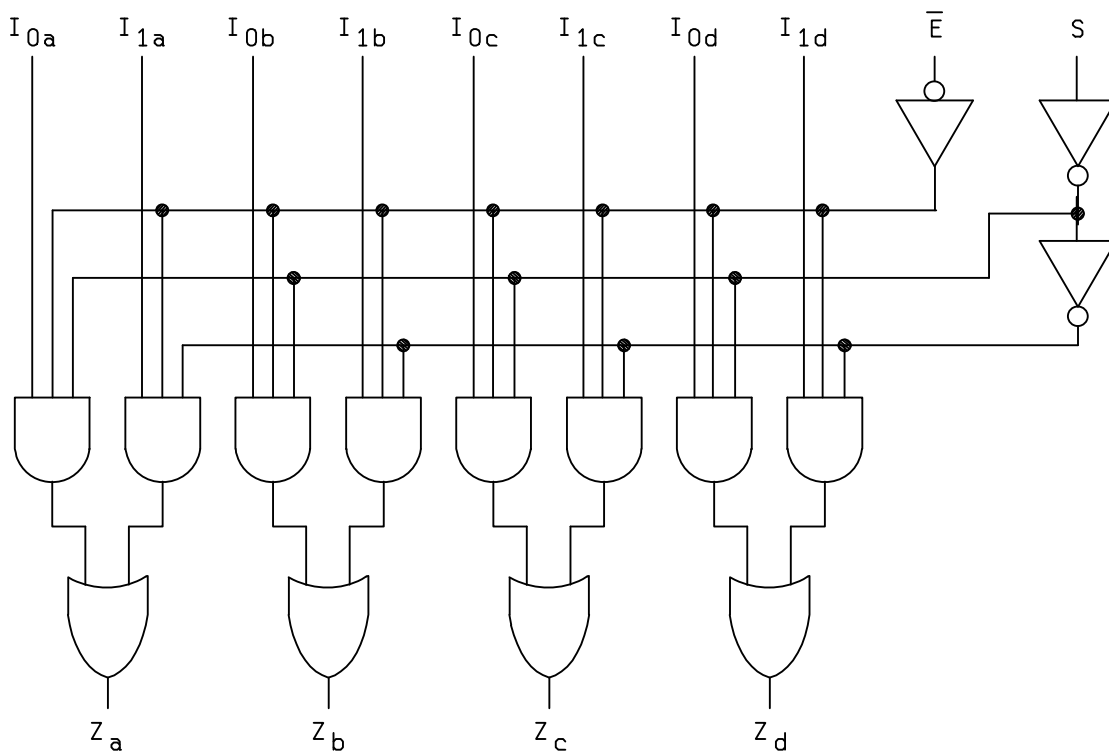


FIGURE 3. Logic diagram.

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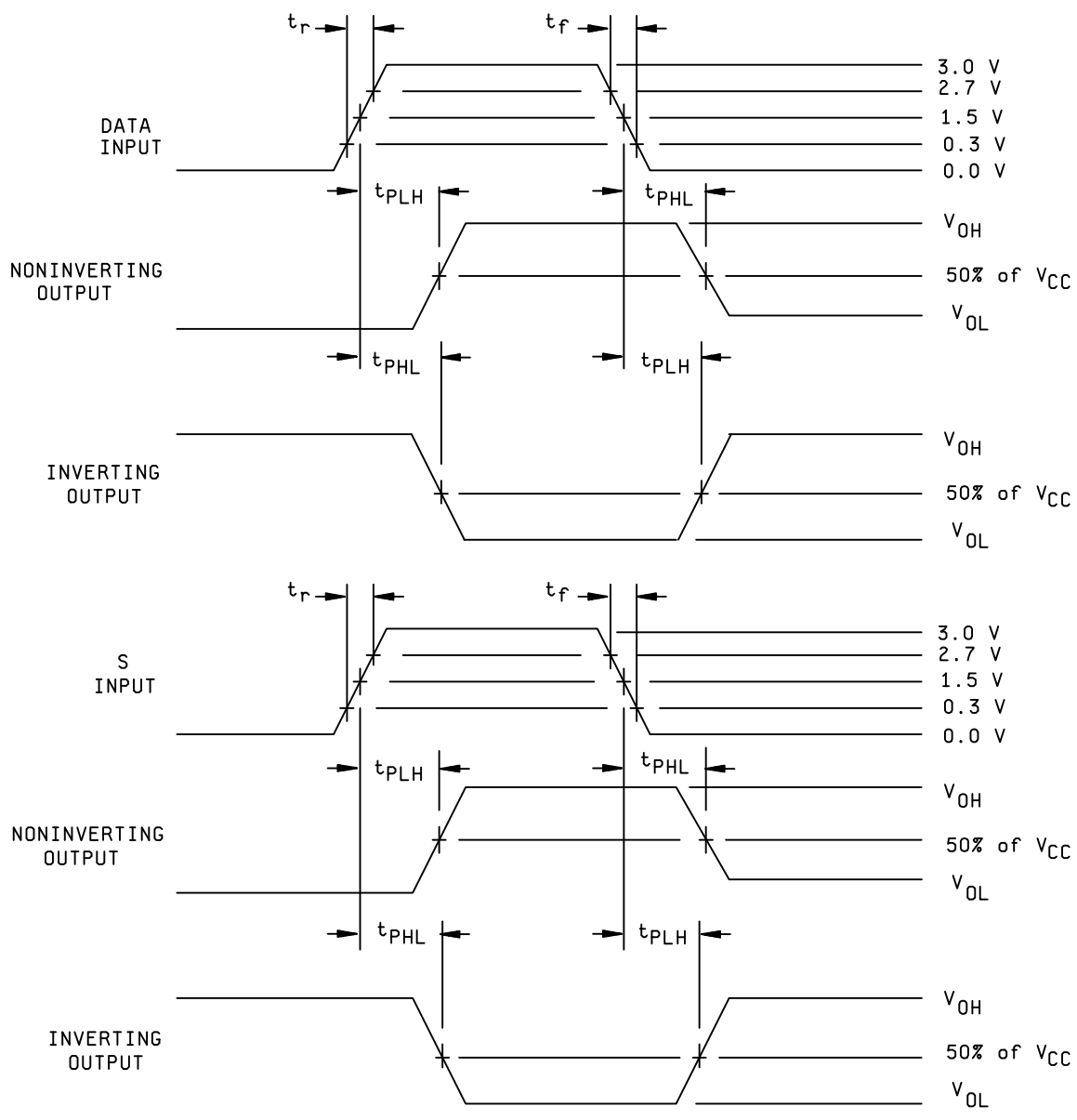
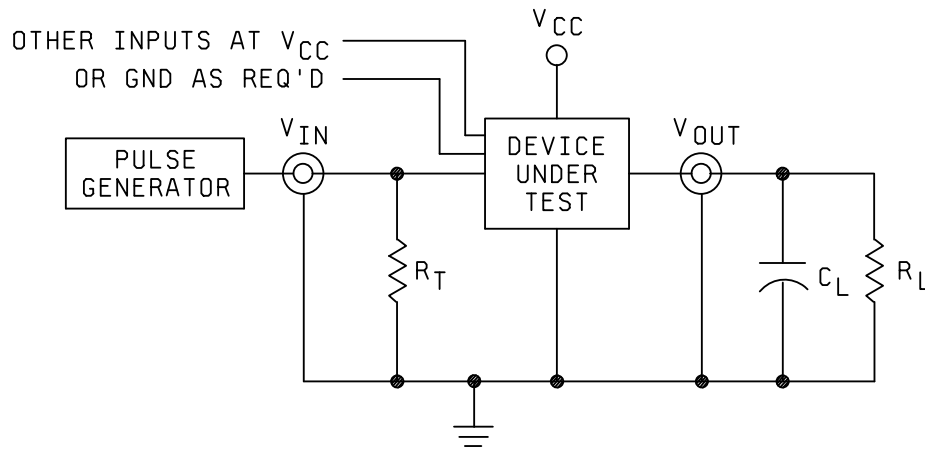
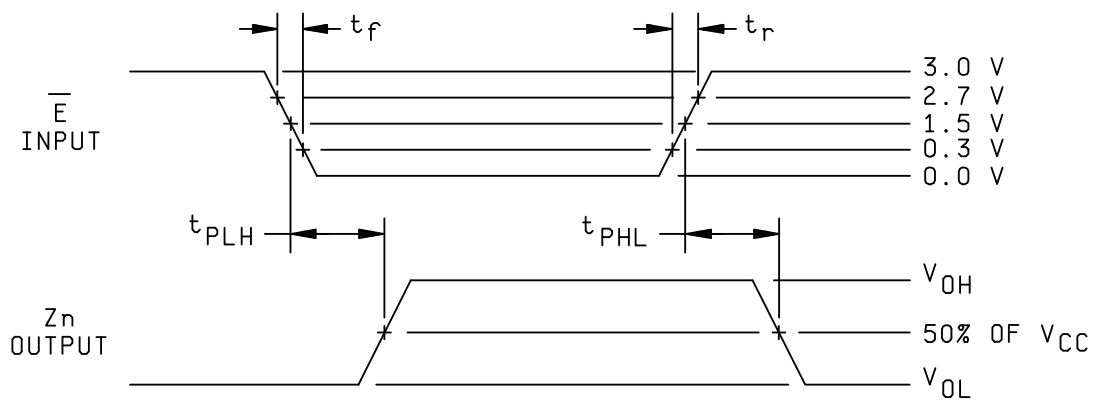


FIGURE 4. Switching waveforms and test circuit.

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NOTES:

1. $C_L = 50 \text{ pF}$ minimum or equivalent (includes test jig and probe capacitance).
2. $R_T = 50\Omega$ or equivalent, $R_L = 500\Omega$ or equivalent.
3. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $PRR \leq 10 \text{ MHz}$; $t_r \leq 3.0 \text{ ns}$; $t_f \leq 3.0 \text{ ns}$; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V , respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz .
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table IA)	Subgroups (in accordance with MIL-PRF-38535, table IIB)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9	<u>1/</u> 1, 2, 3, 7, 8, 9	<u>2/</u> <u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	<u>3/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1, 7, and deltas.

3/ Delta limits, as specified in table IIB, shall be required, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C)

Parameter <u>1/</u>	Symbol	Device type	Delta limits
Quiescent supply current	I_{CCH}, I_{CCL}	01	± 100 nA <u>2/</u>
		02	± 300 nA
Supply current delta	ΔI_{CC}	02	± 0.4 mA
Input current low level	I_{IL}	02	± 20 nA
Input current high level	I_{IH}	02	± 20 nA
Output voltage low level ($I_{OL} = 24$ mA, $V_{CC} = 5.5$ V)	V_{OL}	02	± 0.04 V
Output voltage high level ($I_{OH} = -24$ mA, $V_{CC} = 5.5$ V)	V_{OH}	02	± 0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

2/ Guaranteed if not tested.

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4.4.1 Group A inspection

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD-20 and table IA herein. For C_{IN} and C_{PD} , test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. RHA tests for device classes M, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table IA for subgroups specified in table IIA herein.

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4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Device type 01:

- (1) Inputs tested high, $V_{CC} = 5.5 \text{ V dc } +5\%$, $R_{CC} = 10 \Omega +20\%$, $V_{IN} = 5.0 \text{ V dc } +5\%$, $R_{IN} = 1 \text{ k}\Omega +20\%$, and all outputs are open.
- (2) Inputs tested low, $V_{CC} = 5.5 \text{ V dc } +5\%$, $R_{CC} = 10 \Omega +20\%$, $V_{IN} = 0.0 \text{ V dc}$, $R_{IN} = 1 \text{ k}\Omega +20\%$, and all outputs are open.

b. Device type 02:

- (1) Inputs tested high, $V_{CC} = 5.5 \text{ V dc } \pm 5\%$, $V_{IN} = 5.0 \text{ V dc } +10\%$, $R_{IN} = 1 \text{ k}\Omega \pm 20\%$, and all outputs are open.
- (2) Inputs tested low, $V_{CC} = 5.5 \text{ V dc } \pm 5\%$, $V_{IN} = 0.0 \text{ V dc}$, $R_{IN} = 1 \text{ k}\Omega \pm 20\%$, and all outputs are open.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at $+25^\circ\text{C} \pm 5^\circ\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates that differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The test temperature shall be $+25^\circ\text{C}$ and the maximum rated operating temperature $\pm 10^\circ\text{C}$.
- f. Bias conditions shall be defined by the manufacturer for the latchup measurements.
- g. Test four devices with zero failures.

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4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-05-19

Approved sources of supply for SMD 5962-89688 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.dscc.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8968801EA	0C7V7	54ACT157DMQB
		QP54ACT157DMQB
5962-8968801FA	0C7V7	54ACT157FMQB
		QP54ACT157FMQB
5962-89688012A	0C7V7	54ACT157LMQB
		QP54ACT157LMQB
5962R8968801EA	<u>3/</u>	54ACT157
5962R8968801FA	<u>3/</u>	54ACT157
5962R89688012A	<u>3/</u>	54ACT157
5962R8968801VFA	<u>3/</u>	54ACT157
5962R8968801VEA	<u>3/</u>	54ACT157
5962R8968801V2A	<u>3/</u>	54ACT157
5962R8968801VZA	<u>3/</u>	54ACT157
5962-8968802XA	<u>3/</u>	54ACT157
5962-8968802XC	<u>3/</u>	54ACT157
5962-8968802VXA	<u>3/</u>	54ACT157
5962-8968802VXC	<u>3/</u>	54ACT157
5962F8968802XA	F8859	RHFACT157K02Q
5962F8968802XC	F8859	RHFACT157K01Q
5962F8968802EA	F8859	RHFACT157D04Q
5962F8968802EC	F8859	RHFACT157D03Q
5962F8968802VEA	F8859	RHFACT157D04V
5962F8968802VEC	F8859	RHFACT157D03V
5962F8968802VXA	F8859	RHFACT157K02V
5962F8968802VXC	F8859	RHFACT157K01V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number

Vendor name and address

0C7V7

E2V Aerospace and Defense, Inc.
dba QP Semiconductor, Inc.
2945 Oakmead Village Court
Santa Clara, CA 95051

F8859

ST Microelectronics
3 rue de Suisse
BP4199
35041 RENNES cedex2 - France

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[PI5C3309UEX](#) [PI5C3251QEX](#) [PI3B3251QE](#) [74VHC4052AFT\(BJ\)](#) [PI3PCIE3415AZHEX](#) [NLV74HC4851AMNTWG](#) [MC74LVX257DG](#)
[M74HC151YRM13TR](#) [M74HC151YTTR](#) [PI5USB31213XEAEX](#) [M74HCT4851ADWR2G](#) [XD74LS154](#) [AP4373AW5-7-01](#) [QS3VH251QG8](#)
[QS4A201QG](#) [HCS301T-ISN](#) [HCS500-I/SM](#) [MC74HC151ADTG](#) [TC4066BP\(N,F\)](#) [74ACT11139PWR](#) [HMC728LC3CTR](#) [74VHC238FT\(BJ\)](#)
[74VHC4066AFT\(BJ\)](#) [74VHCT138AFT\(BJ\)](#)