REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Revised to use alternate die/fabrication requirements and “QD” certification mark. New boilerplate. -ljs	00-05-24	Raymond Monnin

The original first page of this drawing has been replaced.

REV																				
SHEET																				
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SHEET																				
REV STATUS				REV			A	A	A	A	A	A	A	A	A	A	A	A		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Thanh V. Nguyen

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY TTL, FLIP-FLOP, MONOLITHIC SILICON

DRAWING APPROVAL DATE
93-02-01

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-90606**

SHEET 1 OF 12

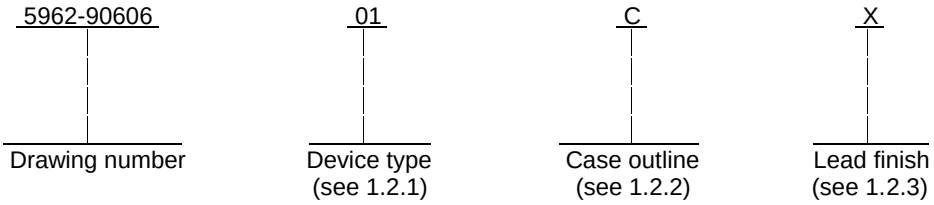
DSCC FORM 2233
APR 97

5962-E274-00

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F113	Dual J-K negative edge-triggered flip-flop with set input
02	54F112	Dual J-K negative edge-triggered flip-flop with set and reset inputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-0.5 V dc minimum to +7.0 V dc maximum
Input current range	-30.0 mA to +5.0 mA
Voltage applied to output in high output state range	-0.5 V to V_{CC}
Current applied to output in low output state	40 mA
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C
Maximum power dissipation (P_D) 2/	
Device type 01	115.5 mW
Device type 02	104.5 mW

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Maximum power dissipation is defined as V_{CC} x I_{CC} and must withstand the added P_D due to the short-circuit output test.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Maximum input clamp current (I_{IK})	-18 mA
Maximum high level output current (I_{OH})	-1.0 mA
Maximum low level output current (I_{OL})	20 mA
Case operating temperature range (T_C)	-55°C to +125°C
Minimum setup time, J_n or K_n to $\overline{CP}n$, high ($t_s(H)$)	
T_C = +25°C	4.0 ns
T_C = -55°C, +125°C	
Device type 01	6.0 ns
Device type 02	5.0 ns
Minimum setup time, J_n or K_n to $\overline{CP}n$, low ($t_s(L)$)	
T_C = +25°C	3.5 ns
T_C = -55°C, +125°C	
Device type 01	5.0 ns
Device type 02	4.0 ns
Minimum hold time, J_n or K_n to $\overline{CP}n$, high or low ($t_h(H)$), $t_h(L)$)	0.0 ns
Minimum $\overline{CP}n$ pulse width, high or low ($t_W(H)$, $t_W(L)$)	
T_C = +25°C	4.5 ns
T_C = -55°C, +125°C	5.0 ns
Minimum $\overline{SD}n$ or $\overline{RD}n$ pulse width, low ($t_w(L)$)	
T_C = +25°C	4.5 ns
T_C = -55°C, +125°C	5.0 ns
Minimum recovery time, $\overline{SD}n$ or $\overline{RD}n$ to $\overline{CP}n$, (t_{rec})	
T_C = +25°C	
Device type 01	4.5 ns
Device type 02	4.0 ns
T_C = -55°C, +125°C	
Device type 01	6.0 ns
Device type 02	5.0 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer's Quality Management (QM) Plan, the "QD" certification mark shall be used in place of the "QML" or "Q" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -1.0 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V		1, 2, 3	All	2.5		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 20 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V		1, 2, 3	All		0.5	
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1, 2, 3	All		-1.2	
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1, 2, 3	All		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V		1, 2, 3	All		100	
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.5 V	J_n, K_n	1, 2, 3	All		-0.6	mA
			$\overline{SDn}$, $\overline{RDn}$				-3.0	
			$\overline{CPn}$				-2.4	
Short circuit output current 1/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.0 V		1, 2, 3	All	-60	-150	
Supply current 2/	I_{CC}	V_{CC} = 5.5 V		1, 2, 3	01		21	mA
					02		19	
Functional tests		See 4.4.1c	V_{CC} = 4.5 V, 5.5 V	7, 8	All			
Maximum clock frequency 3/	f_{MAX}	R_L = 500 Ω C_L = 50 pF See figure 4	V_{CC} = 5.0 V	9	01	85		MHz
			V_{CC} = 4.5 V, 5.5 V	10, 11		80		
			V_{CC} = 5.0 V	9	02	90		
			V_{CC} = 4.5 V, 5.5 V	10, 11		90		

See footnotes at end of table

TABLE I. Electrical performance characteristics. Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay time, $\overline{CPn}$ to Q_n, $\overline{Q}n$	t_{PLH1}, t_{PHL1}	R_L = 500 Ω, C_L = 50 pF, See figure 4	V_{CC} = 5.0 V	9	01	2.0	6.0	ns
			V_{CC} = 4.5 V, 5.5 V	10, 11		2.0	8.0	
			V_{CC} = 5.0 V	9	02	2.0	6.5	
			V_{CC} = 4.5 V, 5.5 V	10, 11		2.0	7.5	
Propagation delay time, $\overline{SDn}$ or $\overline{RDn}$ to Q_n, $\overline{Q}n$	t_{PLH2}, t_{PHL2}		V_{CC} = 5.0 V	9	01	2.0	6.5	
			V_{CC} = 4.5 V, 5.5 V	10, 11		2.0	8.5	
			V_{CC} = 5.0 V	9	02	2.0	6.5	
			V_{CC} = 4.5 V, 5.5 V	10, 11		2.0	7.5	

1/ Not more than one output should be shorted at a time, and the duration of the short-circuit condition should not exceed one second.

2/ With clock input grounded and all outputs open, I_{CC} is measured with Q and $\overline{Q}$ outputs high in turn.

3/ For subgroups 10 and 11, f_{MAX}, if not tested, shall be guaranteed to the specified limits.

Device types	01		02	
Case outlines	C and D	2	E and F	2
Terminal number	Terminal symbol		Terminal symbol	
1	$\overline{CP1}$	NC	$\overline{CP1}$	NC
2	K1	$\overline{CP1}$	K1	$\overline{CP1}$
3	J1	K1	J1	K1
4	$\overline{SD1}$	J1	$\overline{SD1}$	J1
5	Q1	NC	Q1	$\overline{SD1}$
6	$\overline{Q}1$	$\overline{SD1}$	$\overline{Q}1$	NC
7	GND	NC	$\overline{Q}2$	Q1
8	$\overline{Q}2$	Q1	GND	$\overline{Q}1$
9	Q2	$\overline{Q}1$	Q2	$\overline{Q}2$
10	$\overline{SD2}$	GND	$\overline{SD2}$	GND

Device types	01		02	
Case outlines	C and D	2	E and F	2
Terminal number	Terminal symbol		Terminal symbol	
11	J2	NC	J2	NC
12	K2	$\overline{Q}2$	K2	Q2
13	$\overline{CP2}$	Q2	$\overline{CP2}$	$\overline{SD2}$
14	V_{CC}	$\overline{SD2}$	$\overline{RD2}$	J2
15	- - -	NC	$\overline{RD1}$	K2
16	- - -	J2	V_{CC}	NC
17	- - -	NC	- - -	$\overline{CP2}$
18	- - -	K2	- - -	$\overline{RD2}$
19	- - -	$\overline{CP2}$	- - -	$\overline{RD1}$
20	- - -	V_{CC}	- - -	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

Device type 01

Operating mode	Inputs				Outputs	
	$\overline{SD}n$	$\overline{CP}n$	Jn	Kn	Qn	$\overline{Q}n$
Asynchronous set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load “0” (reset)	H	↓	l	h	L	H
Load “1” (set)	H	↓	h	l	H	L
Hold “no change”	H	↓	l	l	q	$\overline{q}$

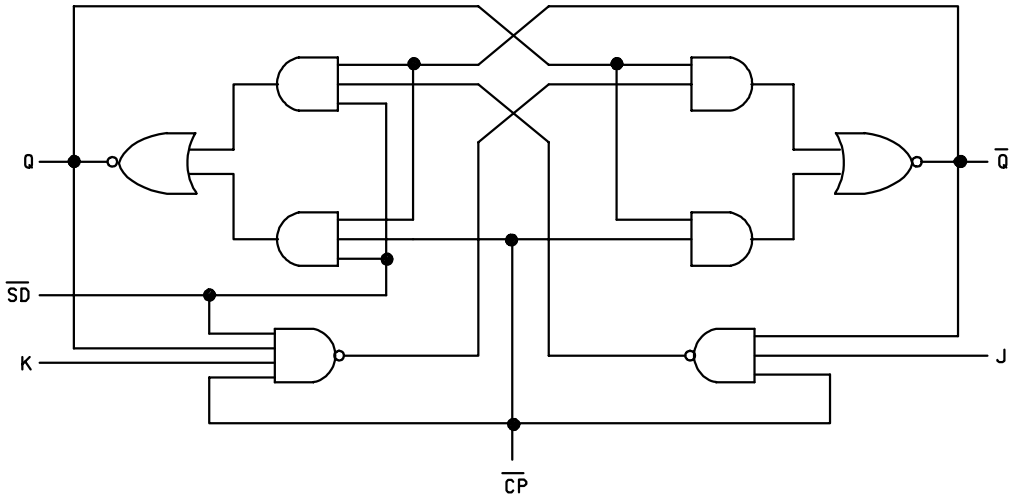
Device type 02

Operating mode	Inputs					Outputs	
	$\overline{SD}n$	$\overline{RD}n$	$\overline{CP}n$	Jn	Kn	Qn	$\overline{Q}n$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load “0” (reset)	H	H	↓	l	h	L	H
Load “1” (set)	H	H	↓	h	l	H	L
Hold “no change”	H	H	↓	l	l	q	$\overline{q}$

H = High voltage level steady state
L = Low voltage level steady state
h = High voltage level one setup time prior to the high-to-low clock transition
l = Low voltage level one setup time prior to the high-to-low clock transition
q = State of the referenced output one setup time prior to the high-to-low clock transition
X = Immaterial
↓ = High-to-low clock transition

FIGURE 2. Truth tables.

Device type 01
(1/2 shown)



Device type 02
(1/2 shown)

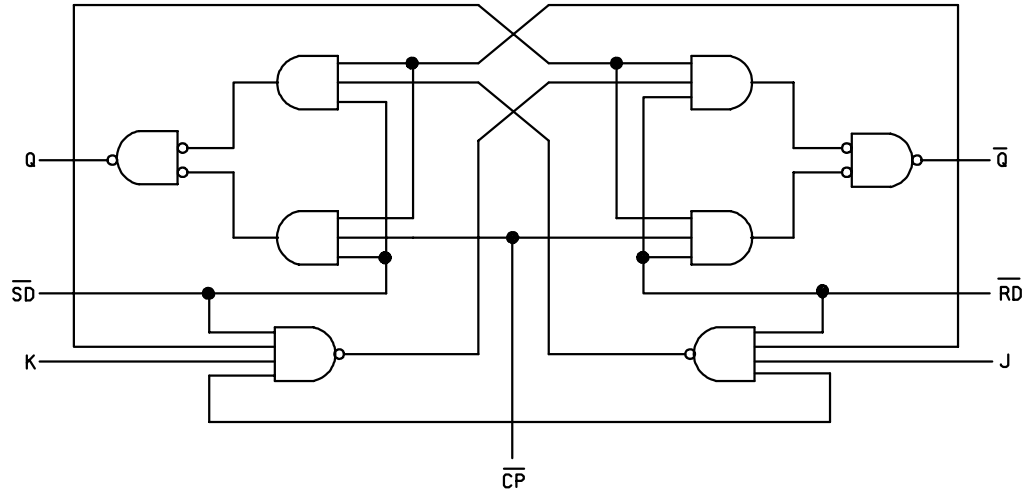


FIGURE 3. Logic diagrams.

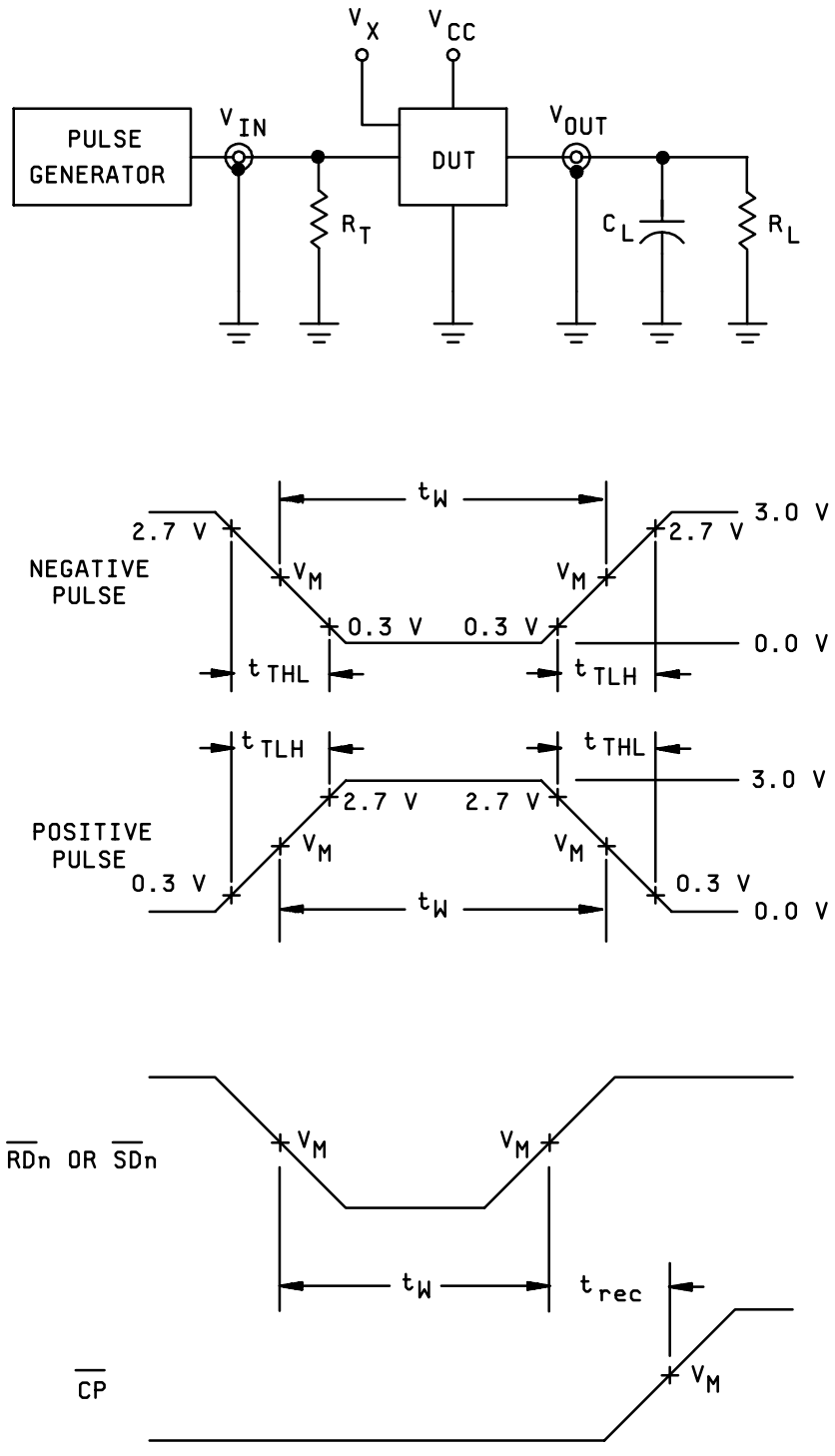
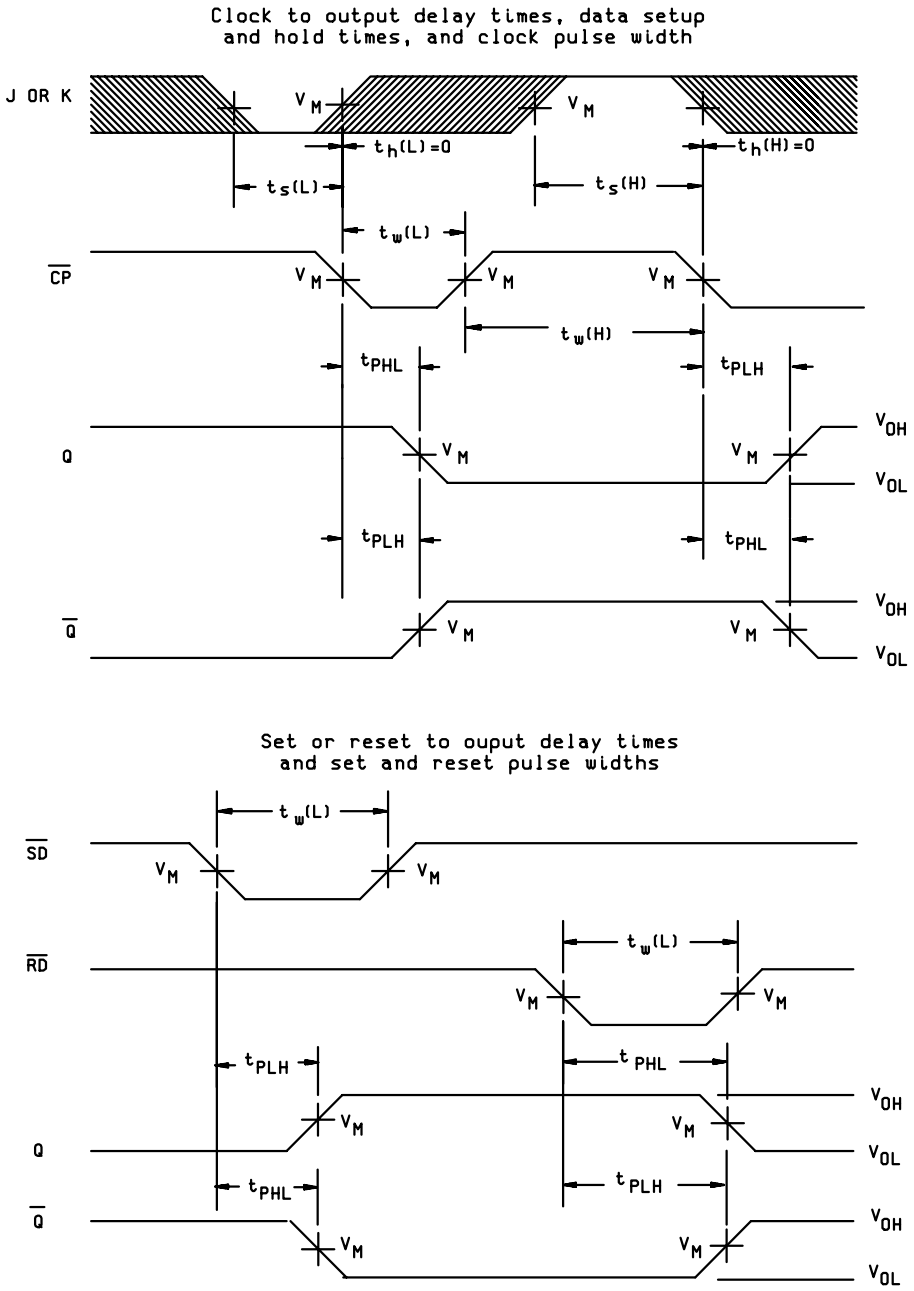


FIGURE 4. Test circuit and switching waveforms.



NOTES:

1. For all waveforms, V_M = 1.5 V.
2. C_L = Load capacitance includes jig and probe capacitance.
3. R_T = Termination resistance should be equal to Z_{OUT} of pulse generator.
4. V_X = Unclocked pins must be held at ≤ 0.8 V, ≥ 2.7 V or open.
5. All input pulses must have the following characteristics: PRR = 1 MHz, $t_{TLH} = t_{THL} \leq 2.5$ ns, t_W = 500 ns, duty cycle = 50 percent.

FIGURE 4. Test circuit and switching waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-05-24

Approved sources of supply for SMD 5962-90606 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9060601CA	3/	
5962-9060601DA	3/	
5962-90606012A	3/	
5962-9060602EA	3/ 0C7V7	54F112/BEA 54F112/EA
5962-9060602FA	3/ 0C7V7	54F112/BFA 54F112/FA
5962-90606022A	3/ 0C7V7	54F112/B2A 54F112/2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Labs 3605 Kifer Road Santa Clara, CA 95051

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5962-8955201EA MC74HC11ADTG MC10EP29MNG MC74HC11ADTR2G NLV14013BDTR2G NLV14027BDG NLX1G74MUTCG 703557B 746431H 5962-90606022A 5962-9060602FA NLV14013BDR2G M38510/30104BDA M38510/07106BFA M38510/06102BFA M38510/06101B2A NLV74HC74ADR2G TC4013BP(N,F) NLV14013BDG NLV74AC32DR2G NLV74AC74DR2G MC74HC73ADG CY74FCT16374CTPACT MC74HC11ADR2G 74LVT74D,118 74VHCT9273FT(BJ) MM74HC374WM 74ALVCH162374PAG TC7WZ74FK,LJ(CT CD54HCT273F HMC853LC3TR HMC723LC3CTR MM74HCT574MTCX MM74HCT273WM SN74LVC74APW SN74LVC74AD MC74HC73ADTR2G MC74HC11ADG SN74ALVTH16374GR M74HCT273B1R M74HC377RM13TR M74HC374RM13TR M74HC175B1R M74HC174RM13TR 74ALVTH16374ZQLR 74ALVTH32374ZKER 74AUP1G74DC,125 74VHC374FT(BJ) 74VHC9273FT(BJ) NLV14013BCPG