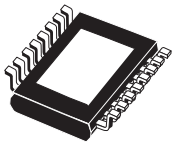
STP04CM05

4-bit constant current power-LED sink driver

Datasheet - production data



TSSOP16
(Exposed pad)

Features

- 4 constant current output channels
- Adjustable output current through one external resistor
- Can be driven by a 3.3 V microcontroller
- Serial data IN/parallel data OUT
- Output current: 80-400 mA
- 20 V of output driving capability
- 30 MHz clock frequency
- UVLO (under voltage lockout) and POR (power ON reset)
- TSD, thermal shutdown, output off when junction temperature exceeds limit
- Operating free-air temperature range -40° to 125 °C
- ESD protection 2.5 kV HBM, 200 V MM
- Available in high thermal TSSOP exposed pad

Description

The STP04CM05 is a high-power LED driver and 4-bit shift register designed for Power-LED applications.

The STP04CM05 contains a 4-bit serial IN, parallel OUT shift register that feeds a 4-bit D-type storage register. In the output stage, four regulated current sources were designed to provide 80-400 mA constant current to drive high power LEDs.

The STP04CM05 guarantees 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, also satisfies the system requirements which include high volume data transmission.

The STP04CM05 is well suited for very high brightness displays and special lighting applications.

The STP04CM05 is offered in TSSOP16 exposed pad packages.

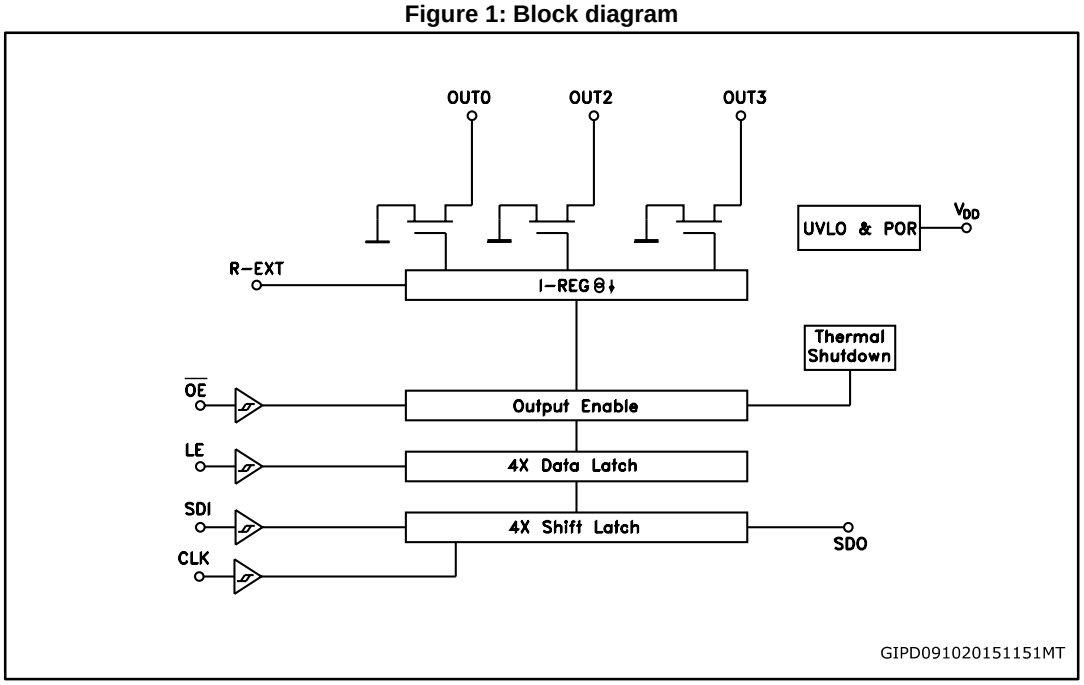
Table 1: Device summary

Order code	Package	Packing
STP04CM05XTTR	TSSOP16 exposed pad (tape and reel)	2500 parts per reel

Contents

1 Internal schematic

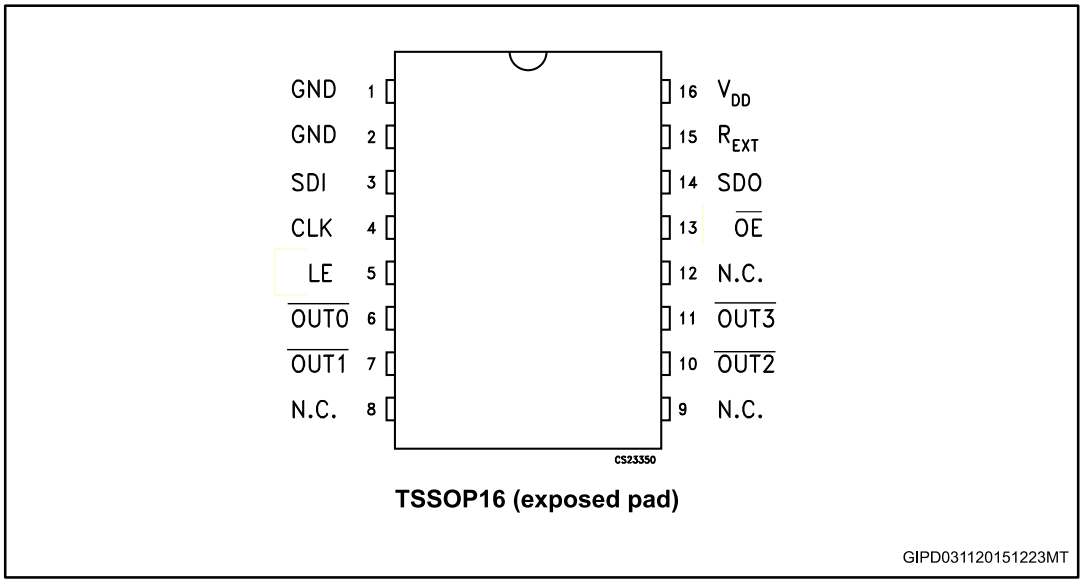
Figure 1: Block diagram



2 Pin settings

2.1 Pin connection

Figure 2: Pin connection



The exposed pad should be attached to a metal land electrically isolated or connected to ground.

2.2 Pin description

Table 2: Pin description

TSSOP16 exposed pad pin N°	Symbol	Name and function
1, 2	GND	Ground terminal
3	SDI	Serial data input terminal
4	CLK	Clock input terminal
5	LE	Latch input terminal
6	OUT 0	Output terminal
7	OUT 1	Output terminal
8, 9, 12	N.C.	Not connected
10	OUT 2	Output terminal
11	OUT 3	Output terminal
13	$\overline{OE}$	Output enable input terminal (active low)
14	SDO	Serial data out terminal
15	R-EXT	Constant current programming
16	V_{DD}	5 V supply voltage terminal

3 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	500	mA
V_I	Input voltage	-0.4 to V_{DD}+0.4	V
I_{GND}	GND terminal current	2000	mA
f_{CLK}	Clock frequency	50	MHz
T_{OPR}	Operating temperature range	-40 to +125	°C
T_{STG}	Storage temperature range	-55 to +150	°C

3.1 Thermal data

Table 4: Thermal data

Symbol	Parameter	TSSOP16 exposed pad	Unit
R_{thJA}	Thermal resistance junction-ambient	37.5 (1)	°C/W

Notes:

(1) Using the PCB multi-layer JEDEC Standard test boards.

3.2 Recommended operating conditions

Table 5: Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.3	5.0	5.5	V
V_O	Output voltage				19	V
I_O	Output current	OUTn V_{DD} = 5 V	80		400	mA
I_{OH}	Output current	Serial-OUT			+1	mA
I_{OL}	Output current	Serial-OUT			-1	mA
V_{IH}	Input voltage		0.7 V_{DD}		V_{DD}+0.3	V
V_{IL}	Input voltage		-0.3		0.3 V_{DD}	V
t_{wEN}	$\overline{OE}$ pulse width	V_{DD} = 5 V, I_O = 350 mA	80	50		ns
		V_{DD} = 3.3 V, I_O = 350 mA	250	150		
t_{wLAT}	LE pulse width	V_{DD} = 3.0 to 3.6 V	8	4		ns
t_{wCLK}	CLK pulse width		8.5	7.5		ns
$t_{SETUP(D)}$	Setup time for DATA		8.5	7.5		ns
$t_{HOLD(D)}$	Hold time for DATA		8.5	7.5		ns
$t_{SETUP(L)}$	Setup time for LATCH		8.5	7.0		ns
$t_{HOLD(E)}$	Hold time for ENABLE		8.5	7.0		ns
f_{CLK}	Clock frequency	Cascade operation (1)			30	MHz
T_{OPR}	Operating temperature range		-40		+125	°C

Notes:

(1) If multiple devices are cascaded, it may not be possible achieve the maximum data transfer. Please consider the timing conditions carefully.

4 Electrical characteristics

T_A = 25 °C, unless otherwise specified.

Table 6: Current accuracy

Output voltage	Current accuracy		Output current
	Between bits	Between ICs	
≥ 1.4 V	Typ. ± 1%	± 6%	80 to 400 mA

Table 7: Electrical characteristics (V_{DD} = 3.3 to 5 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input voltage high level		0.7 V_{DD}		V_{DD}	V
V_{IL}	Input voltage low level		GND		0.3 V_{DD}	V
I_{OH}	Output leakage current	V_{OH} = 19 V			10	µA
V_{OL}	Output voltage (serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (serial-OUT)	I_{OH} = -1 mA	V_{DD}- 0.4 V			V
I_{OL1}	Output current	V_O = 0.3 VR_{EXT} = 980 Ω	75.2	80	84.8	mA
I_{OL2}		V_O = 1.2 VR_{EXT} = 190 kΩ	376	400	424	mA
ΔI_{OL1}	Output current error between bit (all output ON)	V_O = 0.3 VR_{EXT} = 980 Ω I_O = 80 mA		1	1.5	%
ΔI_{OL2}		V_O = 1.2 VR_{EXT} = 190 Ω I_O = 400 mA		1	1.5	%
$R_{SIN(up)}$	Pull-up resistor		150	300	600	kΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	kΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{EXT} = OPEN OUT 0 to 3 = OFF		1	1.5	mA
$I_{DD(OFF2)}$		R_{EXT} = 980 Ω OUT 0 to 3 = OFF		3.8	6	
$I_{DD(OFF3)}$		R_{EXT} = 190 Ω OUT 0 to 3 = OFF		14	18.5	
$I_{DD(ON1)}$	Supply current (ON)	R_{EXT} = 980 Ω OUT 0 to 3 = ON		4.0	6.0	
$I_{DD(ON2)}$		R_{EXT} = 190 Ω OUT 0 to 3 = ON		14.5	19	

Table 8: Switching characteristics (V_{DD} = 3.3 to 5 V)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{PLH1}	Propagation delay time, CLK- $\overline{OUTn}$ LE = H, / $\overline{OE}$ = L	R_L = 5.0 Ω, C_L = 10 pF, I_O = 350 mA, R_{EXT} = 224 Ω, V_L = 3.0 V	V_{DD} = 3.3 V	-	290	377	
			V_{DD} = 5 V	-	200	260	ns
t_{PLH2}	Propagation delay time, LE- $\overline{OUTn}$, / $\overline{OE}$ = L		V_{DD} = 3.3 V	-	200	260	
			V_{DD} = 5 V	-	140	180	ns
t_{PLH3}	Propagation delay time, / $\overline{OE}$ - $\overline{OUTn}$, LE = H		V_{DD} = 3.3 V	-	240	310	ns
			V_{DD} = 5 V	-	170	220	
t_{PLH}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	25	35	
			V_{DD} = 5 V	-	15	20	ns
t_{PHL1}	Propagation delay time, CLK- $\overline{OUTn}$ LE = H, / $\overline{OE}$ = L		V_{DD} = 3.3 V	-	49	64	
			V_{DD} = 5 V	-	36	47	ns
t_{PHL2}	Propagation delay time, $\overline{LE}$ - $\overline{OUTn}$, / $\overline{OE}$ = L		V_{DD} = 3.3 V	-	39	51	
			V_{DD} = 5 V	-	26	34	ns
t_{PHL3}	Propagation delay time, / $\overline{OE}$ - $\overline{OUTn}$ LE = H		V_{DD} = 3.3 V	-	48	62	ns
			V_{DD} = 5 V	-	32	42	
t_{PHL}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	30	39	
			V_{DD} = 5 V	-	19	25	ns
t_{ON}	Output rise time 10~90% of voltage waveform		V_{DD} = 3.3 V	-	880	1150	
			V_{DD} = 5 V	-	616	800	ns
t_{OFF}	Output fall time 90~10% of voltage waveform		V_{DD} = 3.3 V	-	18	24	
			V_{DD} = 5 V	-	14	18	ns
t_r	CLK rise time (1)	V_O = 5.0 V, R_{EXT} = 224 Ω		-		5000	ns
t_f	CLK fall time (1)			-		5000	ns

Notes:

(1) In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

5 Equivalent circuit and outputs

Figure 3: OE terminal

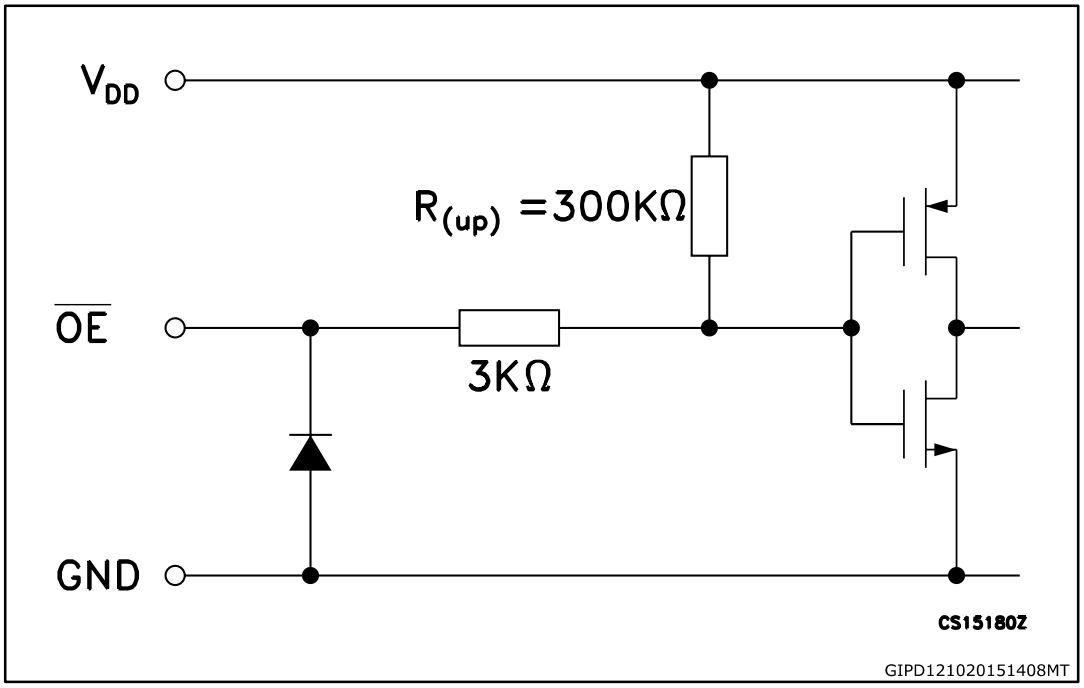


Figure 4: LE terminal

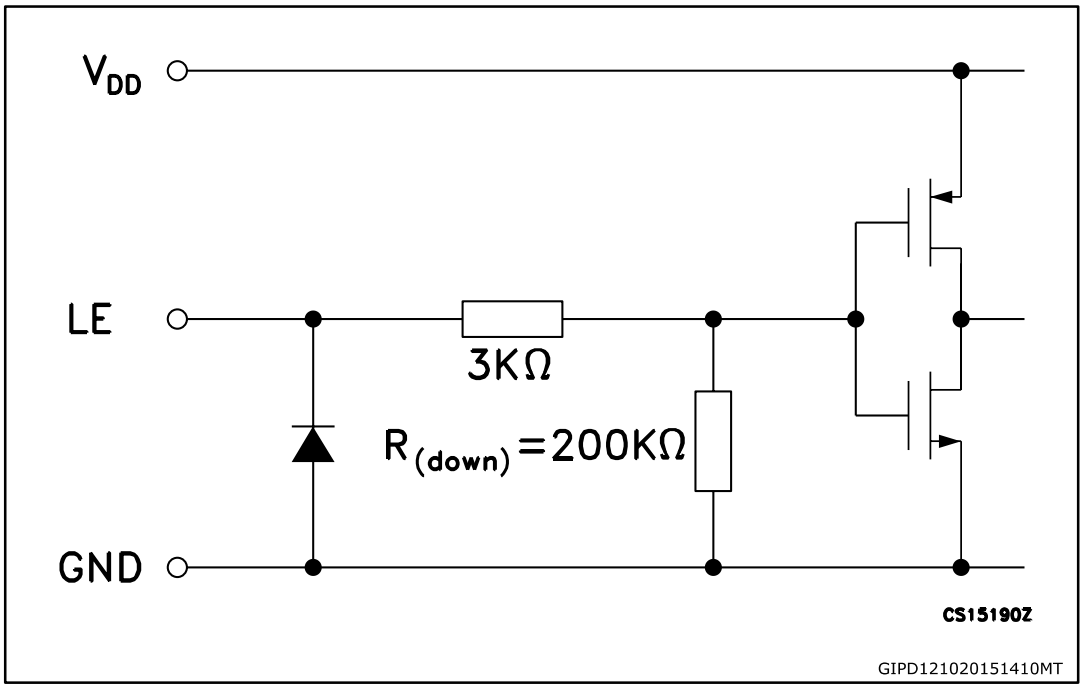


Figure 5: CLK, SDI terminal

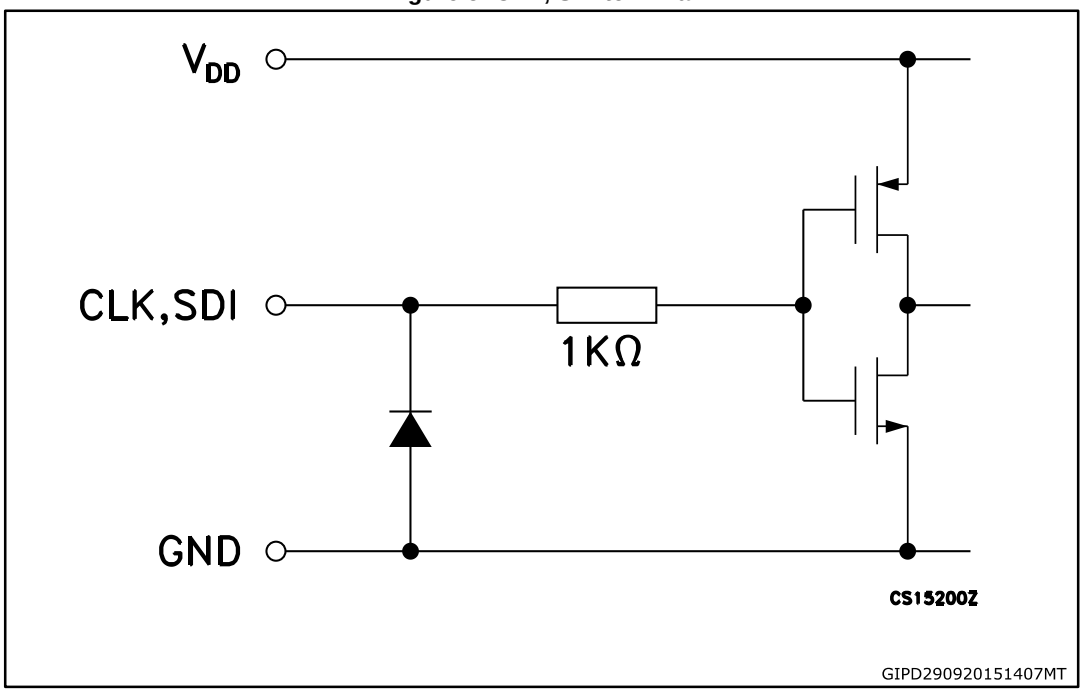
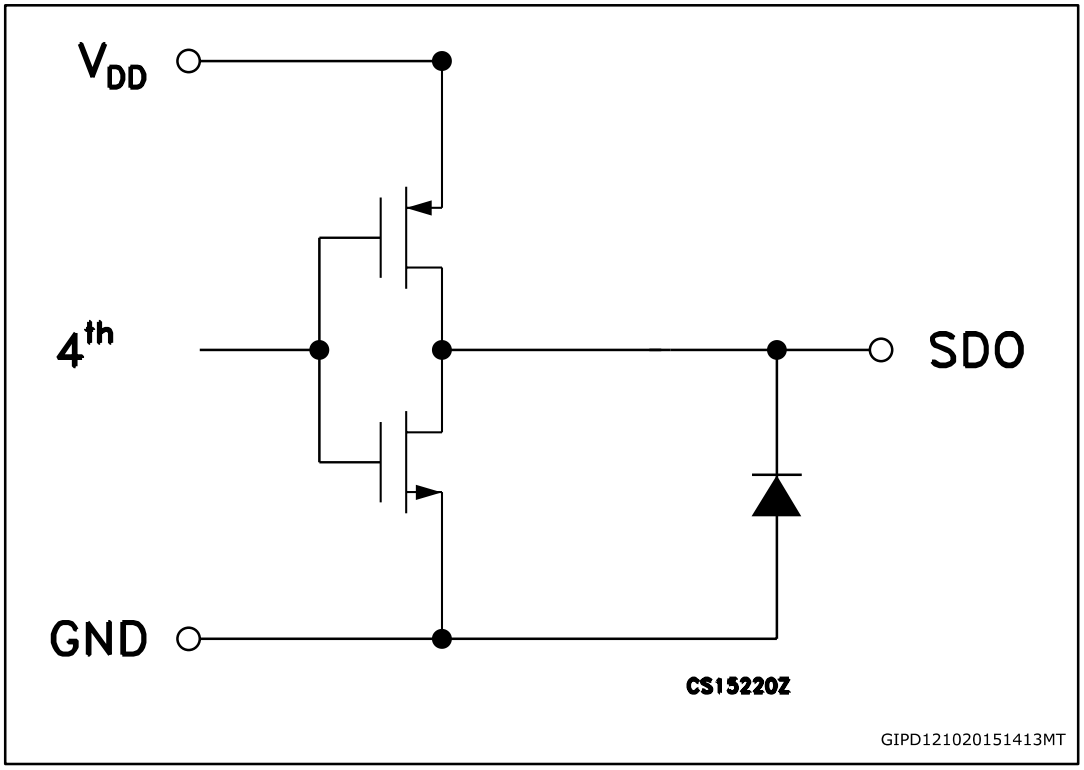
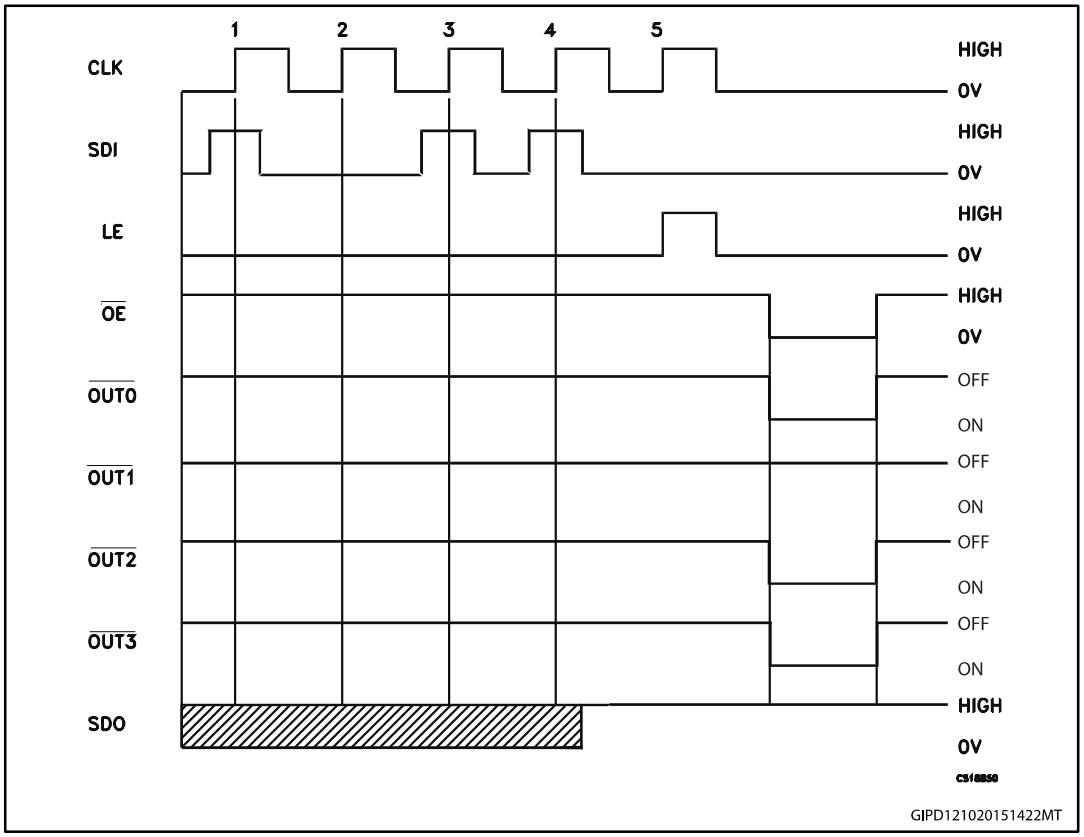


Figure 6: SDO terminal



6 Timing diagrams

Figure 7: Timing diagram



1 Latch and output enable are level sensitive and are not synchronized with rising-or-falling edge of CLK signal.

2 When LE terminal is low level, the latch circuit hold previous set of data.

3 When LE terminal is high level, the latch circuit refresh new set of data from SDI chain.

4 When OE terminal is at low level, the output terminal - Out 0 to Out 03 respond to data in the latch circuits, either ‘1’ for ON or ‘0’ for OFF.

5 When OE terminal is at high level, all output terminals will be switched OFF.

Figure 8: Clock, serial-in, serial-out

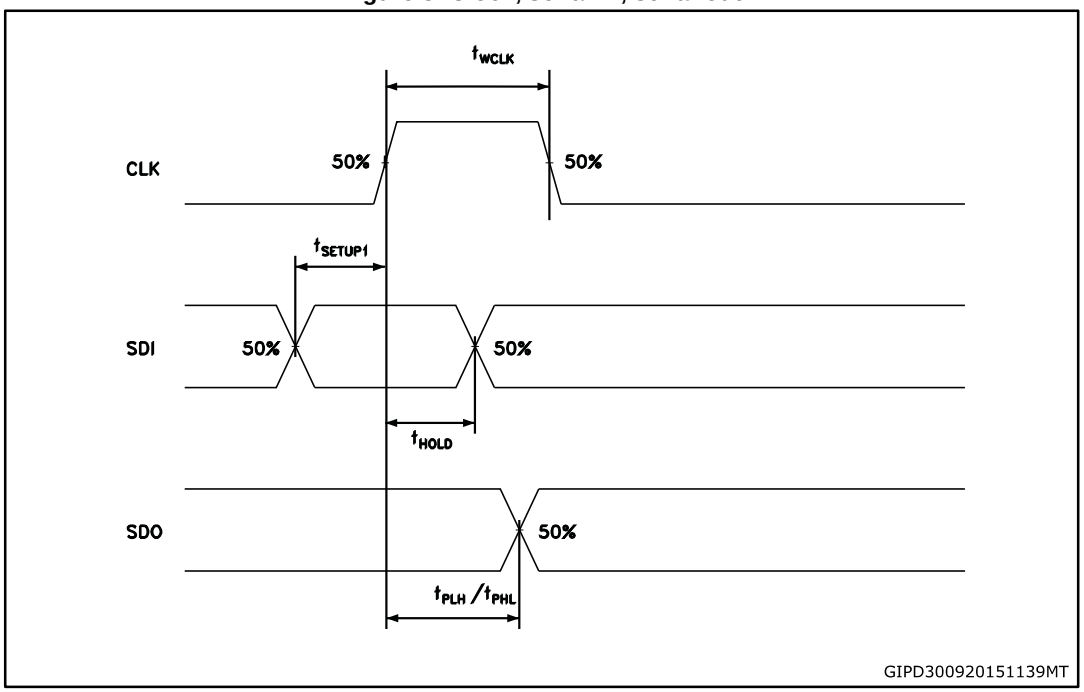


Figure 9: Clock, serial-in, latch, enable, outputs

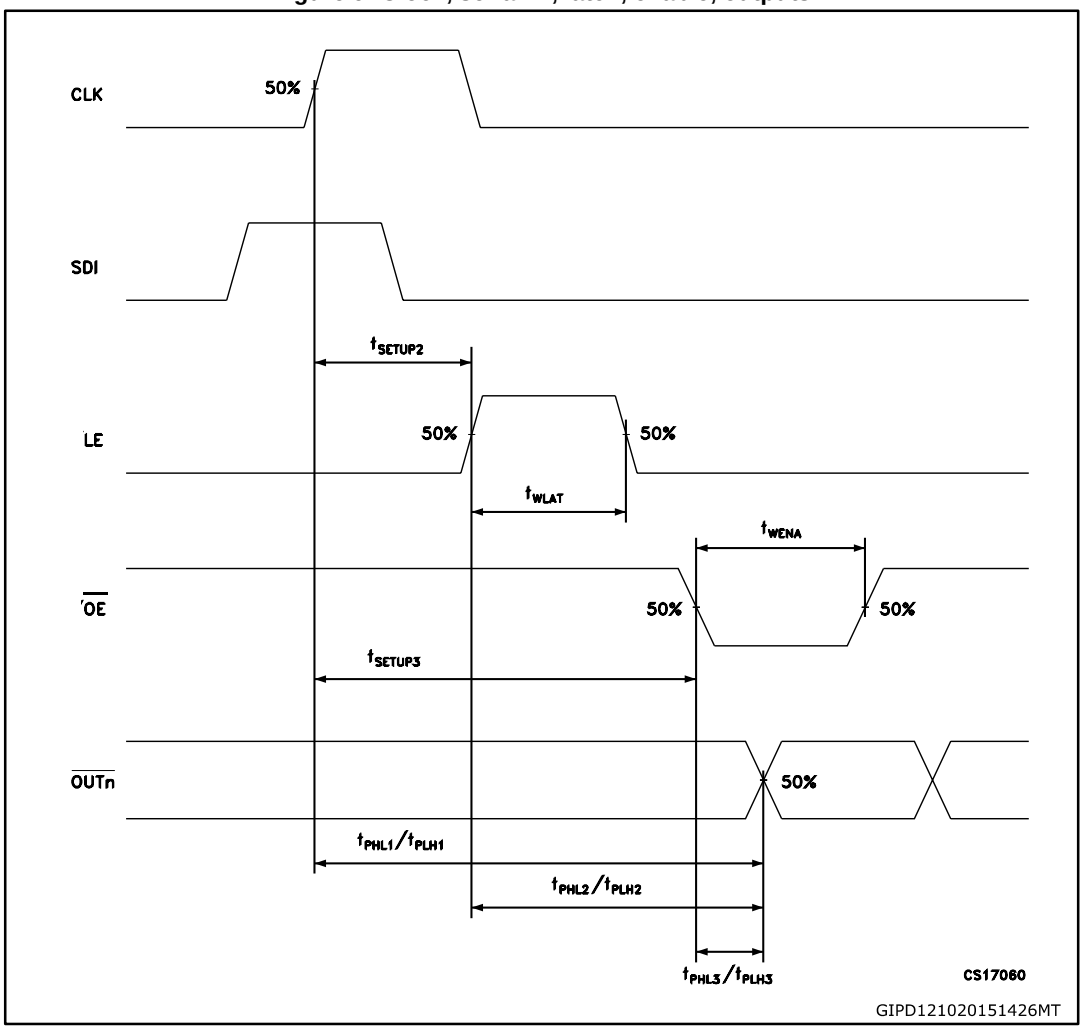
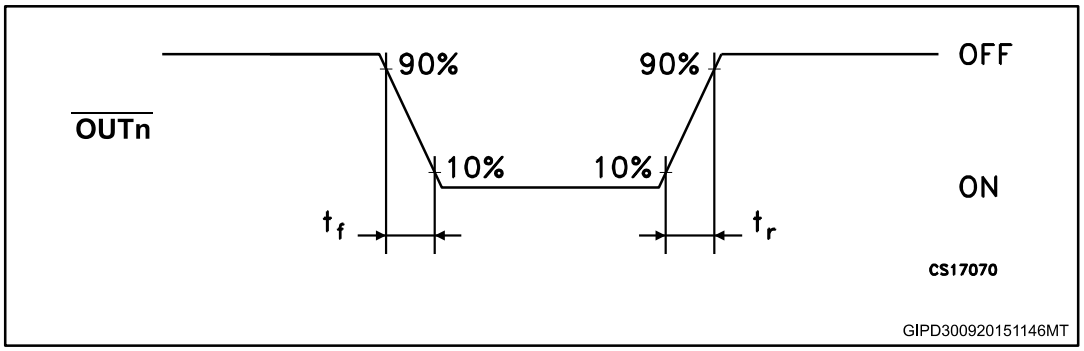


Figure 10: Outputs



7 Test circuit

Figure 11: DC characteristic

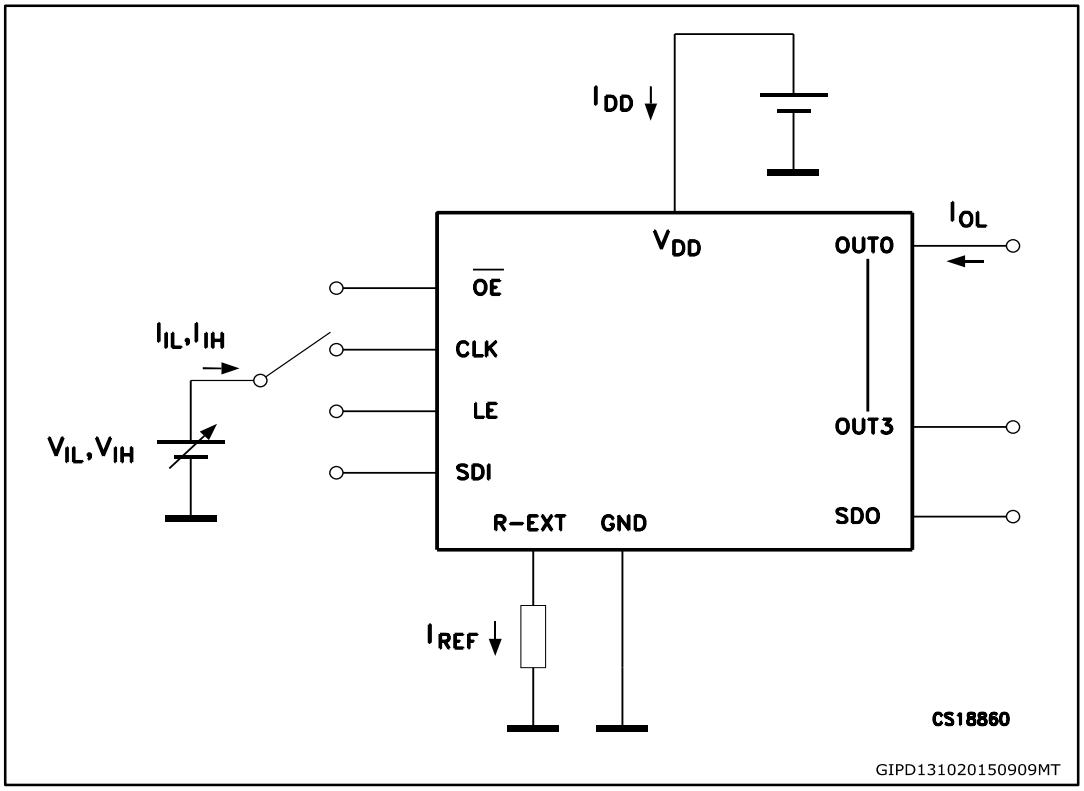
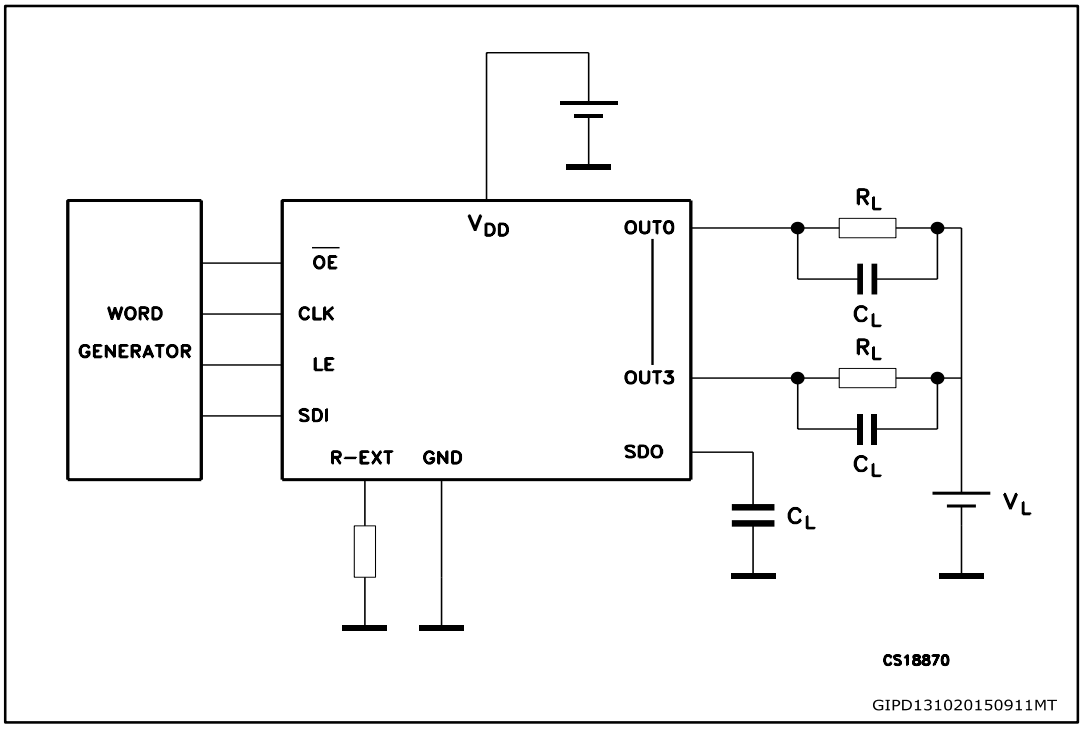


Figure 12: AC characteristic



8 Typical characteristics

Figure 13: Output current-R_{EXT} resistor

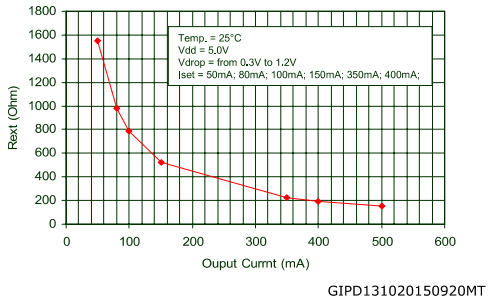


Figure 14: Output current vs dropout voltage

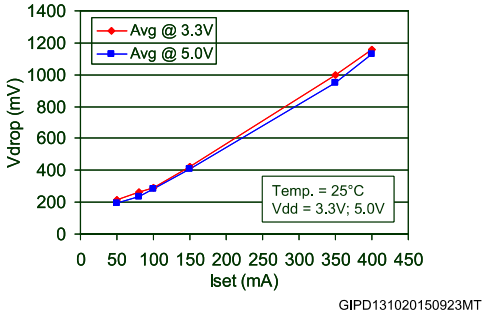


Figure 15: Output current vs ± ΔI_{OL}(%)

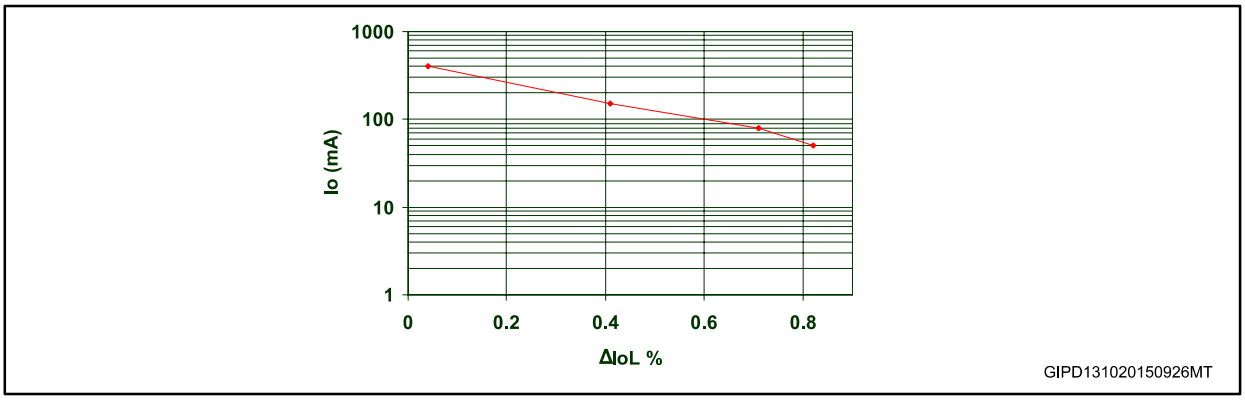
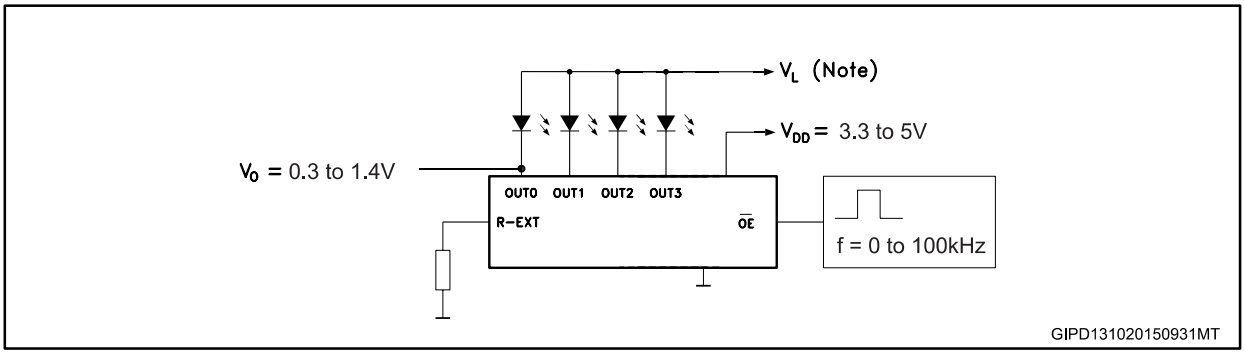


Figure 16: Four power-LED typ. application circuit



V_L will be determined by the V_F of the LEDs.

Condition: T_A = 25 °C, V_{dd} = 5 V,V_L = 3 V, R_{ext} = 227 Ω.

Figure 17: t_{ON}

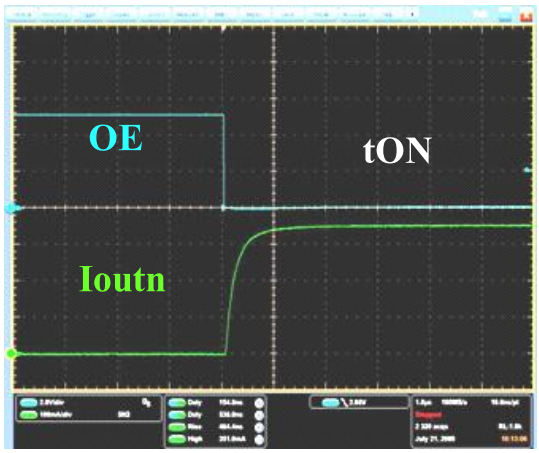


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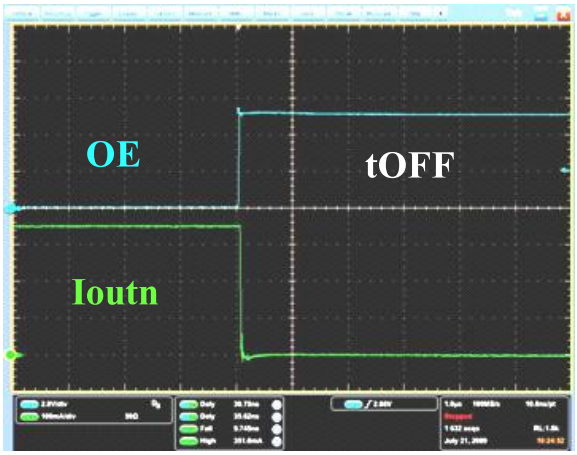
Figure 18: t_{OFF}



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9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

9.1 TSSOP16 exposed pad package information

Figure 19: TSSOP16 exposed pad package outline

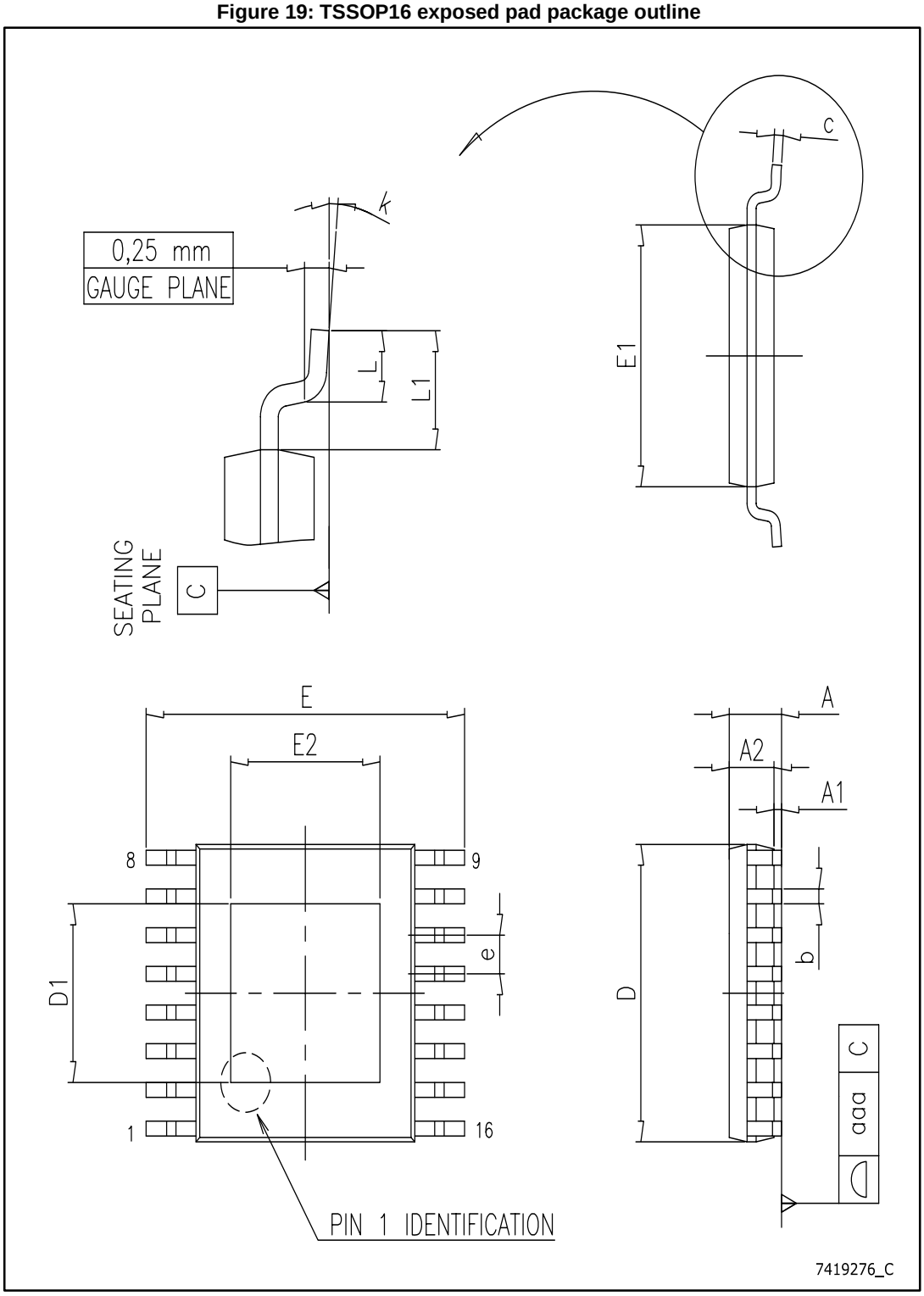

Table 9: TSSOP16 exposed pad package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.10
A1	0.05		0.15
A2	0.85	0.90	0.95
b	0.19		0.30
c	0.09		0.20
D		5.00	
D1	ACCORDING TO PAD SIZE		
E		6.40	
E1	4.30	4.40	4.50
E2	ACCORDING TO PAD SIZE		
e		0.65	
L	0.50	0.60	0.70
L1		1.00	
k			8
aaa			0.076

9.2 TSSOP16 exposed pad packing information

Figure 20: TSSOP16 exposed pad tape and reel outline

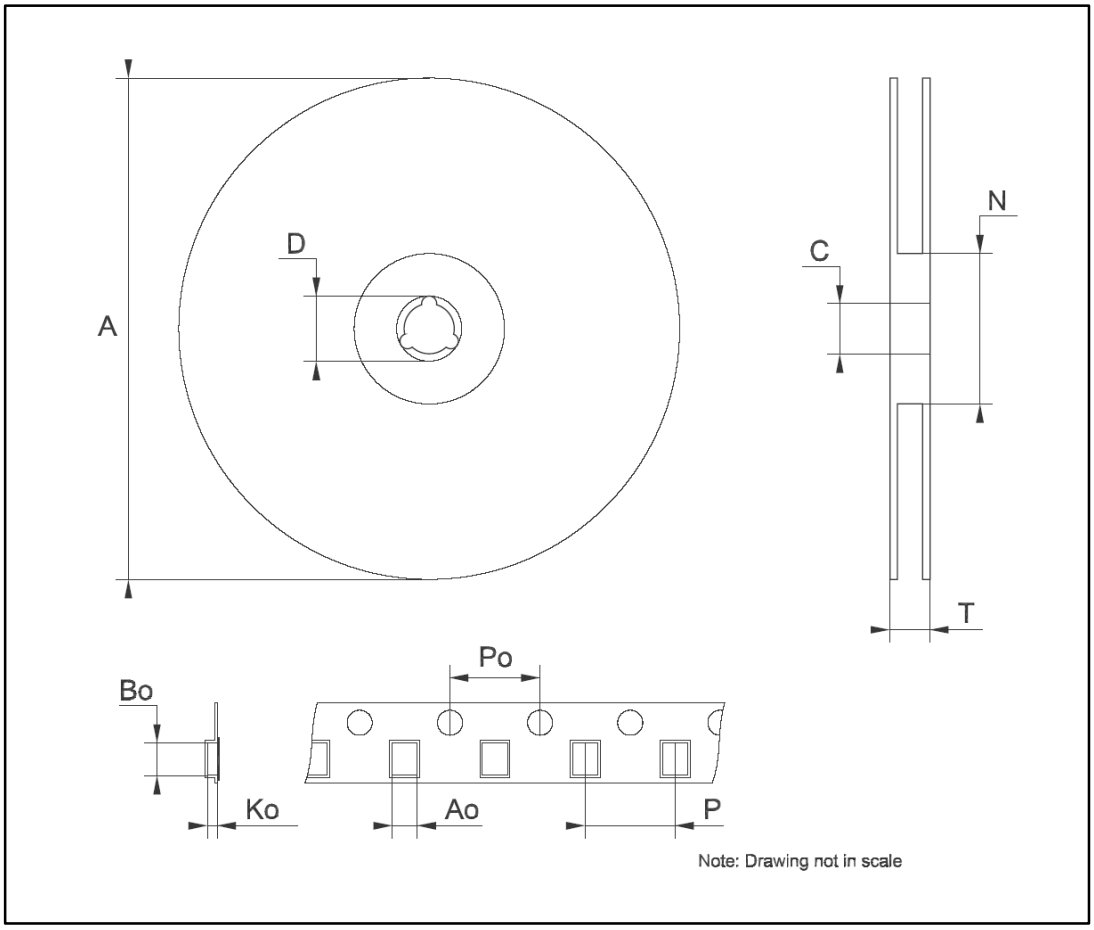

Table 10: TSSOP16 exposed pad packing mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

10 Revision history

Table 11: Document revision history

Date	Revision	Changes
26-Nov-2007	1	Initial release
16-Jan-2008	2	Added: Figure 15 on page 15 and Figure 19 on page 17, Updated: Table 8 on page 8.
12-Mar-2008	3	Updated: Figure 8 on page 12.
23-Jun-2008	4	Updated: Table 1 on page 1, Figure 21 on page 20.
07-Jun-2010	5	Updated: Note: on page 4, Table 10 on page 19.
07-Jan-2016	6	Removed SO-14 package. Updated *Figure 5: "CLK, SDI terminal"*. Minor text changes.

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