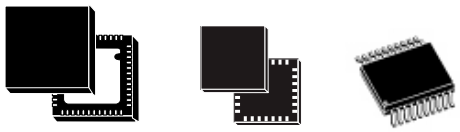
# STM8TL52x4 STM8TL53x4

## 8-bit ultra-low-power touch sensing microcontroller with 16 Kbyte Flash, ProxSense™, timers, USART, SPI, I2C

**Datasheet - production data**

## Features

- Operating conditions
  - Operating power supply: 1.65 V to 3.6 V
  - Temperature range: –40 °C to 85 °C
- Low power features
  - 4 low power modes: Wait, Active-halt with AWU (1 µA), Active-halt with ProxSense™ (10 µA with scan every 200 ms), Halt (0.4 µA)
  - Dynamic power consumption: 150 µA/MHz
  - Fast wakeup from Halt mode: 4.7 µs
  - Ultra-low leakage per I/O: 50 nA
- Advanced STM8 Core
  - Harvard architecture with 3-stage pipeline
  - Max freq.16 MHz,16 CISC MIPS peak
- Memories
  - Up to 16 Kbyte of Flash program including up to 2 Kbyte of data EEPROM
  - Error correction code (ECC)
  - Flexible write and read protection modes
  - In-application and in-circuit programming
  - Data EEPROM capability
  - 4 Kbyte of static RAM
- Clock management
  - Internal 16 MHz factory-trimmed RC
  - Internal 38 kHz low consumption RC driving both the IWDG and the AWU
- Reset and supply management
  - Ultra-low-power, ultra safe power-on reset/ power-down reset
- Interrupt management
  - Nested interrupt controller with software priority control
  - Up to 22 external interrupt sources



UFQFPN48 7x7 mm | UFQFPN28 4x4 mm | TSSOP20

- I/Os
  - Up to 23 with 22 mappable on external interrupt vectors
  - I/Os with programmable input pull-ups, high sink/source capability
- ProxSense™ patented acquisition technology with up to 300 touch sensing channels (20 receiver/transmitter channels and 15 transmitter channels) supporting projected capacitive acquisition method suitable for proximity detection.
- Timers
  - Two 16-bit general purpose timers (TIM2 and TIM3) with up and down counter and two channels (used as IC, OC, PWM)
  - One 8-bit timer (TIM4) with 7-bit prescaler
  - Independent watchdog
  - Window watchdog
  - Auto-wakeup unit
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - SPI synchronous serial interface
  - Fast $I^2C$ Multimaster/slave 400 kHz
  - USART with fractional baud rate generator
- Development support
  - Hardware single wire interface module (SWIM)
  - In-circuit emulation (ICE)

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM8TL52x4 | STM8TL52F4, STM8TL52G4 |
| STM8TL53x4 | STM8TL53C4, STM8TL53F4, STM8TL53G4 |

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# 1 Introduction

This datasheet provides the STM8TL52G4, STM8TL52F4, STM8TL53C4, STM8TL53G4 and STM8TL53F4 pinouts, ordering information, mechanical and electrical device characteristics.

For complete information on the microcontroller memory, registers and peripherals, please refer to the STM8TL5xxx reference manual (RM0312) and to the STM8TL5xxx Flash programming manual (PM0212) for Flash memory related information. For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470). For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

All devices of the STM8TL5xxx product line provide the following benefits:

- Advanced capacitive sensing
  - Patented ProxSense ™ acquisition peripheral, providing high-end acquisition, filtering and environment adaptation
  - Outstanding signal-to-noise ratio for touch and proximity sensing
  - Up to 300 projected capacitive channels
- Reduced system cost
  - Up to 16 Kbyte of low-density embedded Flash program memory including up to 2 Kbyte of data EEPROM
  - High system integration level with internal clock oscillators and watchdogs
  - Smaller battery and cheaper power supplies
- Low power consumption and advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Less than 150 µA/MHz, 0.8 µA in Active-halt mode with AWU, and 0.3 µA in Halt mode
  - Clock gated system and optimized power management
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the-art technology
  - Product family operating from 1.65 V to 3.6 V supply

*Note: ProxSense ™ is a trademark of Azoteq (Pty) Ltd.*

# 2 Description

The STM8TL52x4 and STM8TL53x4 devices feature the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations. It uses a ProxSense charge transfer capacitive acquisition method that is capable of near range proximity detection.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming. All STM8TL52x4 and STM8TL53x4 microcontrollers feature low-power low-voltage single-supply program Flash memory.

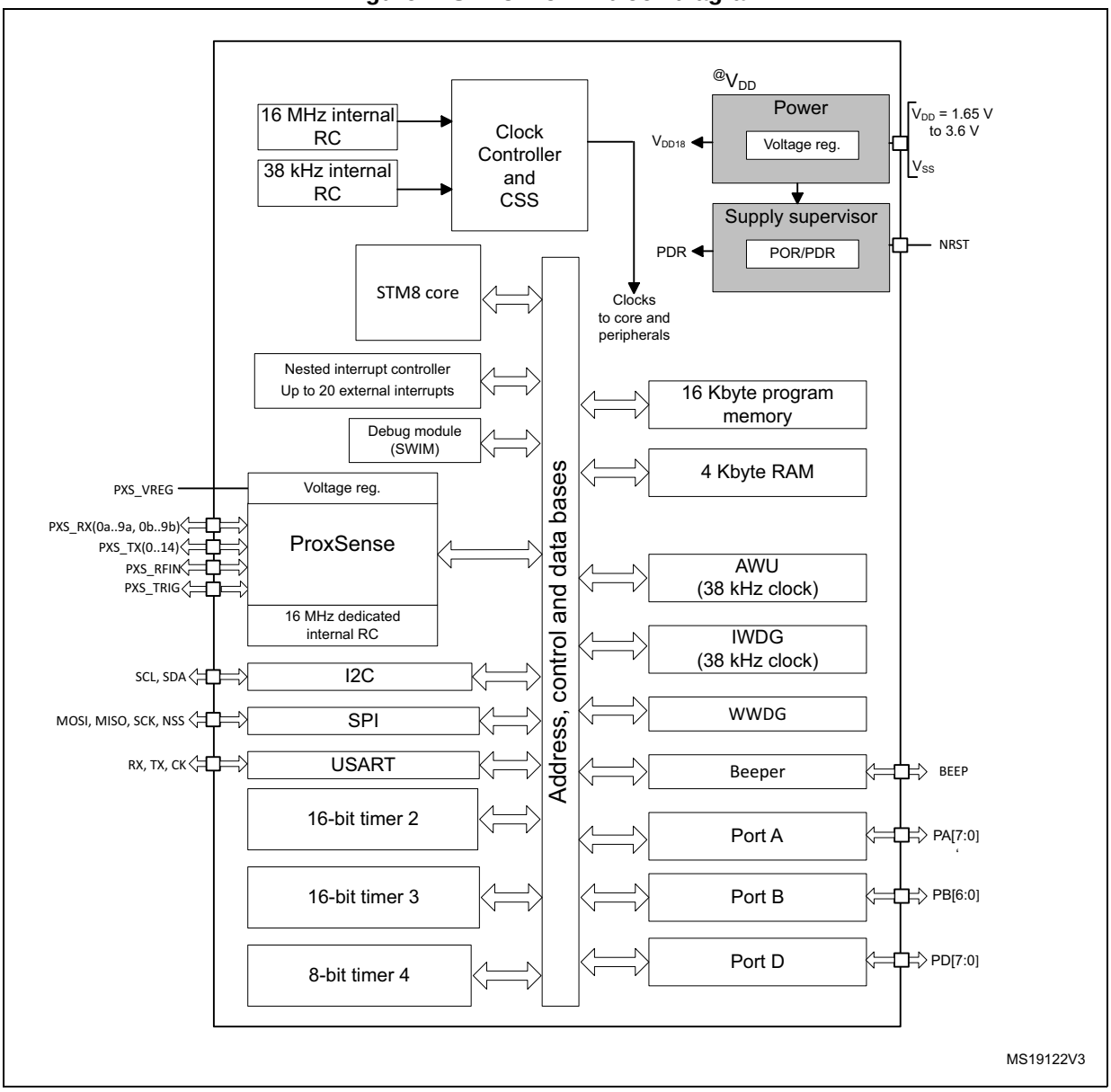
The STM8TL52x4 and STM8TL53x4 devices are based on a generic set of state-of-the-art peripherals. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

**Table 2. Device features**

| Features | | STM8TL52F4 | STM8TL53F4 | STM8TL52G4 | STM8TL53G4 | STM8TL53C4 |
|---|---|---|---|---|---|---|
| Flash (Kbyte) | | 16 | | | | |
| Data EEPROM (Kbyte) | | 2 | | | | |
| RAM (Kbyte) | | 4 | | | | |
| Timers | Basic | 1 (8-bit) | | | | |
| | General purpose | 2 (16-bit) | | | | |
| Communication Interfaces | SPI | 1 | | | | |
| | I2C | 1 | | | | |
| | USART | 1 | | | | |
| GPIOs | | 12 | | 17 | | 23 |
| ProxSense | | Up to 12 touch sensing channels (5 receiver/ transmitter channels and 2 transmitter channels) | Up to 30 touch sensing channels (5 receiver/ transmitter channels and 6 transmitter channels) | Up to 25 touch sensing channels (8 receiver/ transmitter channels and 2 transmitter channels) | Up to 72 touch sensing channels (8 receiver/ transmitter channels and 9 transmitter channels) | Up to 300 touch sensing channels (20 receiver/ transmitter channels and 15 transmitter channels) |
| Others | | Window watchdog, independent watchdog, two 16-MHz and one 38-kHz internal RC, auto-wakeup counter, beeper | | | | |
| CPU frequency | | 16 MHz | | | | |
| Operating voltage | | 1.65 to 3.6 V | | | | |
| Operating temperature | | -40 to +85 °C | | | | |
| Packages | | TSSOP20 | | UFQFPN28 | | UFQFPN48 |

# 3 Product overview

**Figure 1. STM8TL5xx4 block diagram**




Legend:

AWU: Auto-wakeup unit
Int. RC: internal RC oscillator
I²C: Inter-integrated circuit multimaster interface
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous / asynchronous receiver / transmitter
IWDG: Independent watchdog
WWDG: Window watchdog
ProxSense™: capacitive sensing peripheral

## 3.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

### Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify - write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

### Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

### Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

## 3.2 Development tools

Development tools for the STM8 microcontrollers include:

- The ST-Link very low-cost professional tool to debug and program
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software
- The STM-STUDIO real-time and non-intrusive graphical interface used to probe application variables and data

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

## 3.3 Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

## 3.4 Interrupt controller

The STM8TL5xx4 devices feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 22 interrupt vectors with hardware priority
- Up to 22 external interrupt sources on 10 vectors
- TRAP and RESET interrupts

## 3.5 Memory

The STM8TL5xx4 devices have the following main features:

- 4 Kbyte of RAM
- The EEPROM is divided into two memory arrays (see the STM8TL5xxx reference manual (RM0312) for details on the memory mapping):
  - 16 Kbyte of low-density embedded Flash program including up to 2 Kbyte of data EEPROM. Data EEPROM and Flash program areas can be write protected independently by using the memory access security mechanism (MASS).
  - 64 option bytes (one block) of which 5 bytes are already used for the device.
  - Error correction code is implemented on the EEPROM.

## 3.6 Low power modes

To minimize power consumption, the product features three MCU low power modes:

- Wait mode: CPU clock stopped, selected peripherals at full clock speed.
- Active-halt mode:
  - When wakeup time is programmed in the AWU unit, the CPU and peripheral clocks are stopped. The RAM content is preserved.
  - When a ProxSense acquisition is ongoing, the wakeup is on ProxSense interrupts; the CPU and the other peripheral clocks are stopped.
- Halt mode: CPU and peripheral clocks are stopped, the device remains powered on. Wakeup is triggered by an external interrupt.

The ProxSense peripheral can return to low power mode between each conversion.
The ProxSense acquisition can be operated in Run, Wait and Active-halt modes.

## 3.7 Voltage regulators

The STM8TL5xx4 devices embed an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals and a second internal voltage regulator providing a stable power supply (around 1.45V) for the ProxSense peripheral.

### 3.7.1 Dual-mode voltage regulator

This regulator has two different modes: main voltage regulator mode (MVR) and low power voltage regulator mode (LPVR). When in Active-halt mode, the regulator remains in MVR if ProxSense is active. When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption unless ProxSense is enabled.

### 3.7.2 ProxSense voltage regulator

This regulator provides a very stable voltage to power the ProxSense peripheral including ProxSense pins in order to be independent of any power supply variations. This regulator is switched on while the ProxSense peripheral is enabled (bit PXSEN = 1) and bit LOW_POWER is set to ‘0’ in register PXS_CR1. Otherwise, when LOW_POWER is set to ‘1’, this regulator is only enabled during conversions (while CIPF = 1 and SYNCPF = 0).

## 3.8 Clock control

The STM8TL5xx4 embeds a robust clock controller. It is used to distribute the system clock (SYSCLK) to the core and the peripherals and to manage clock gating for low power modes. This system clock is a 16-MHz High Speed Internal RC oscillator (HSI RC), followed by a programmable prescaler.

In addition, a 38 kHz low speed internal RC oscillator is used by the Independent watchdog (IWDG) and Auto-wakeup unit (AWU).

## 3.9 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM3 channels can be remapped.

## 3.10 Independent watchdog

The independent watchdog (IWDG) peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 38 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

## 3.11 Window watchdog

The window watchdog (WWDG) is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

## 3.12 Auto-wakeup counter

The auto-wakeup (AWU) counter is used to wakeup the device from Active-halt mode.

## 3.13 General purpose and basic timers

STM8TL5xx4 devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

### 16-bit general purpose timers

The 16-bit timers consist of 16-bit up/down auto-reload counters driven by a programmable prescaler. They perform a wide range of functions, including:

- Timebase generation
- Measuring the pulse lengths of input signals (input capture)
- Generating output waveforms (output compare, PWM and One pulse mode)
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

### 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

## 3.14 Beeper

STM8TL5xx4 devices include a beeper function used to generate a beep signal in the range of 1, 2 or 4 kHz when the LSI clock is operating at a frequency of 38 kHz.

## 3.15 USART

The USART interface (USART) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Single wire half duplex mode

## 3.16 SPI

The serial peripheral interface (SPI) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK/2)}$ both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

## 3.17 $I^2C$

The $I^2C$ bus interface ($I^2C$) provides multi-master capability, and controls all $I^2C$ bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Dual addressing mode capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- Hardware CRC calculation

## 3.18 ProxSense

The ProxSense peripheral uses a charge-transfer method to detect capacitance changes.

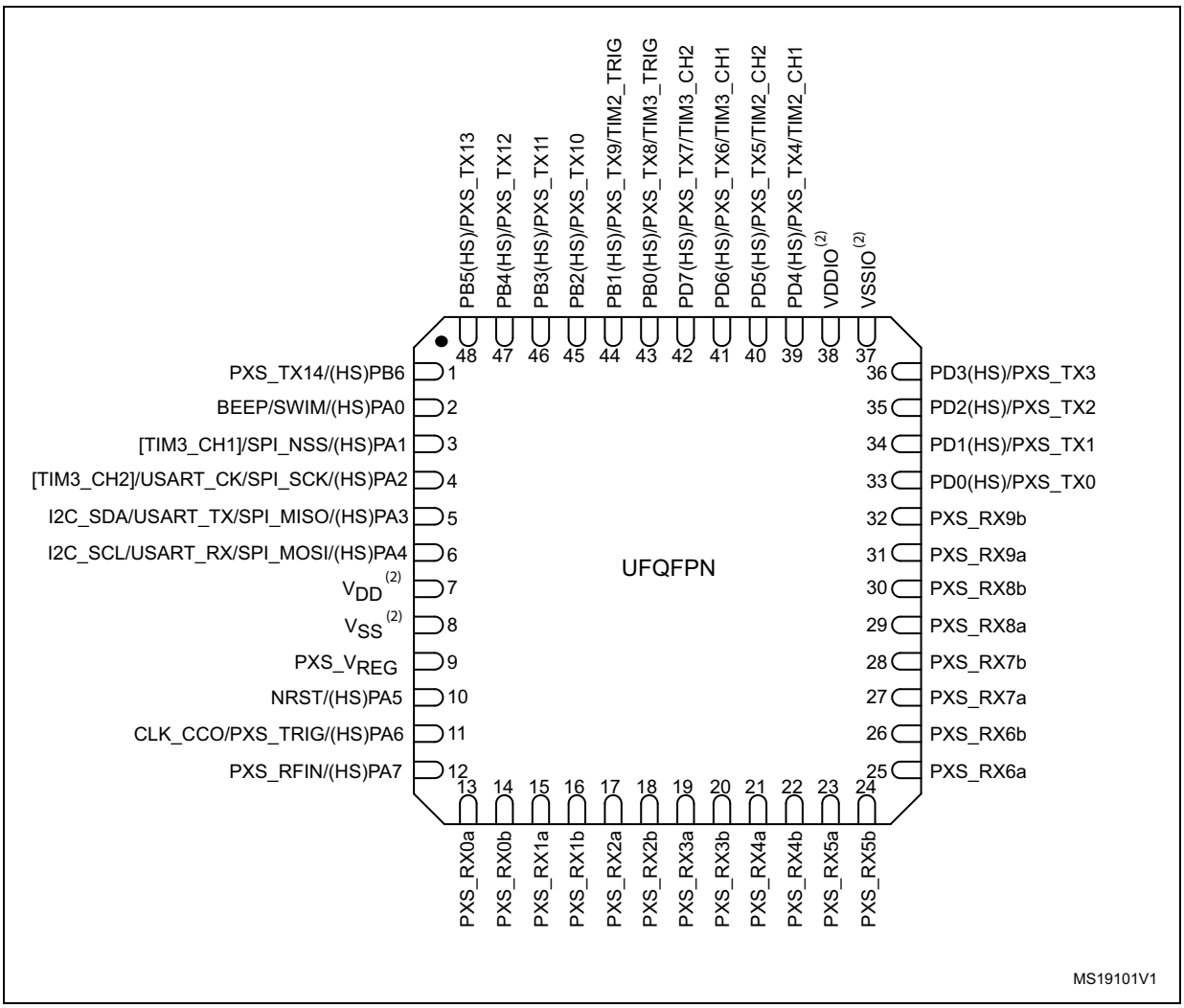
- Up to 300 capacitive sensing channels composed of 15 transmitters and 20 receivers with up to 10 Rx channels acquired in parallel
- Fast acquisition with a typical scan time of 250 µs for 10 Rx channels
- Configurable internal sampling capacitor ($C_S$)
- Electrode Parasitic Capacitance Compensation (EPCC) to ensure the best sensitivity in all user environments
- RF noise detection, allowing to reject corrupted samples
- External trigger to de-synchronize the acquisition from known noise
- Can be configured to return to low power mode between each conversion
- Acquisition possible in Run, Wait and Active-halt modes

## 3.19 TouchSensing dedicated library available upon request

- Complete C source code library with firmware examples (MISRA compliant)
- Multifunction capability to combine capacitive sensing functions with traditional MCU features
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Configuration of all ProxSense parameters
- Extra filtering and calibration functions
- TouchSensing user interface through firmware API for status reporting and application configuration
- Compliance with Cosmic, IAR and Raisonance C compilers

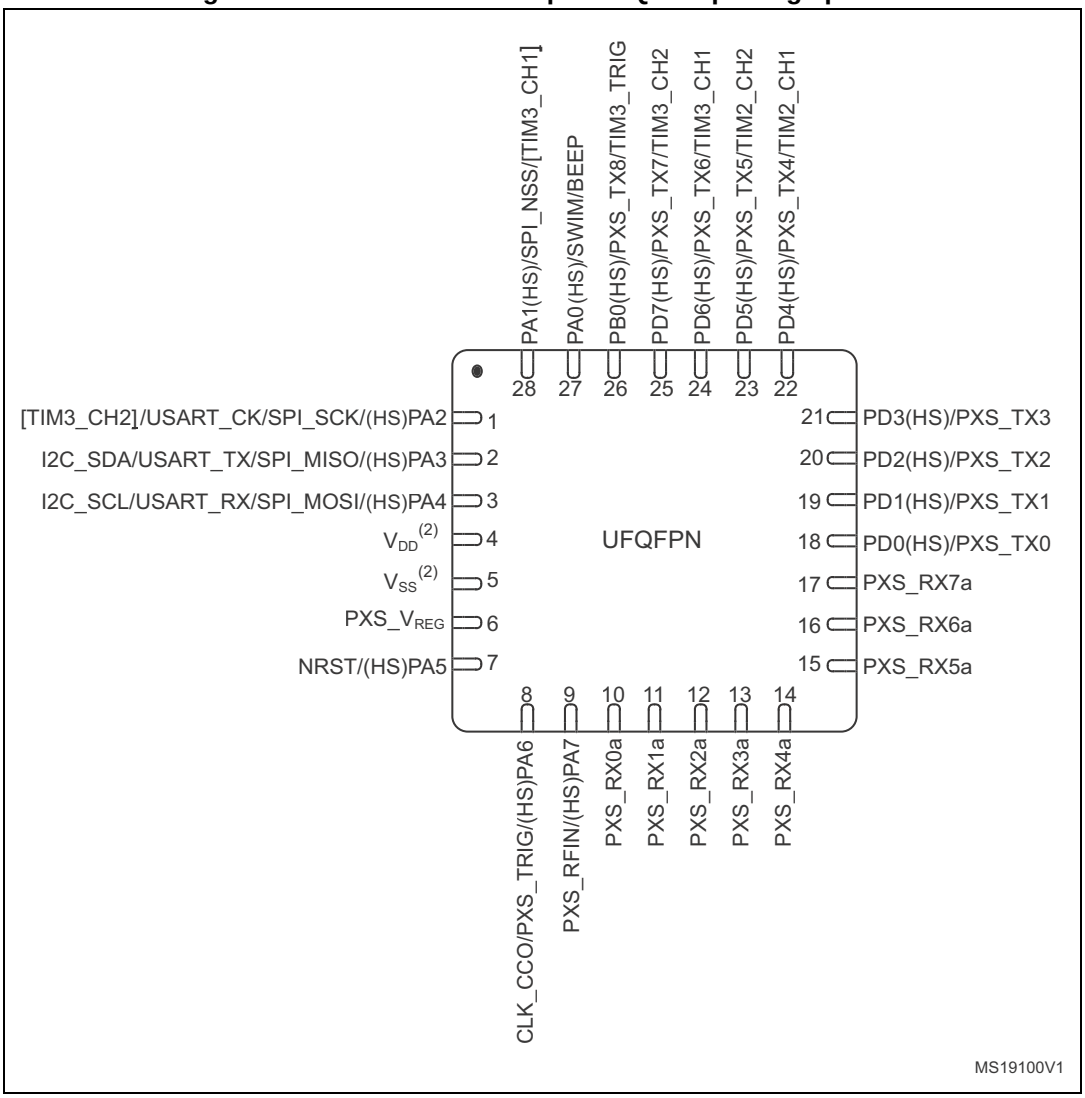
# 4 Pin description

**Figure 2. STM8TL53 48-pin UFQFPN package pinout**




1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312), Section 6: Power supply.

**Figure 3. STM8TL53G4U6 28-pin UFQFPN package pinout**




1. HS corresponds to 20 mA high sink/source capability.
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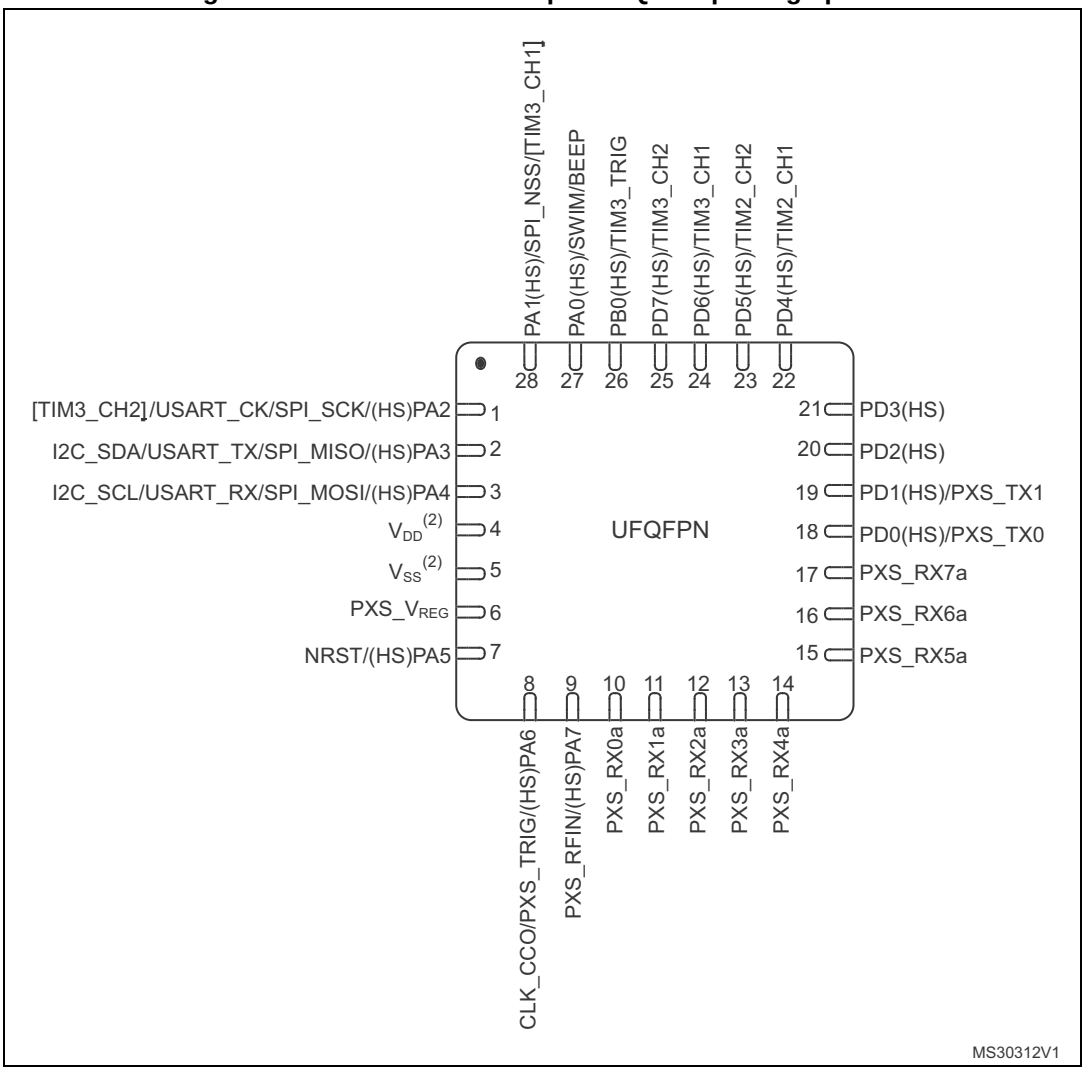
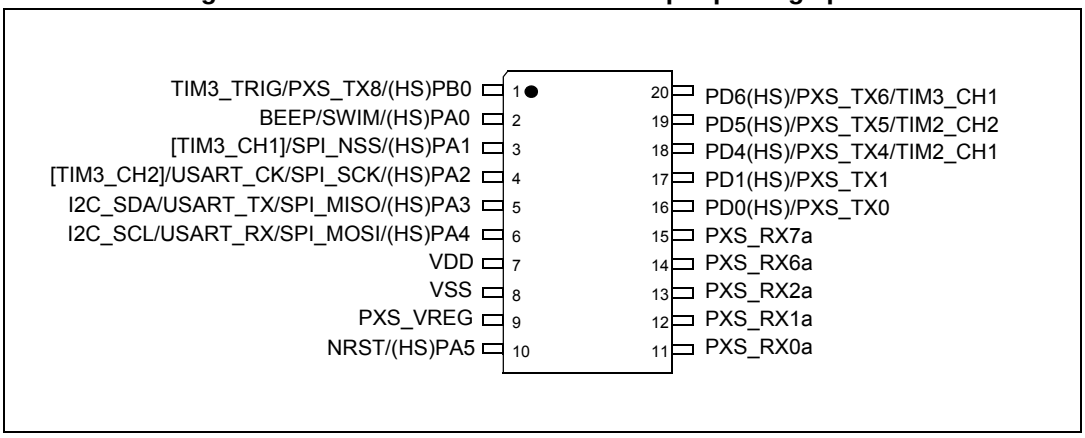
**Figure 4. STM8TL52G4U6 28-pin UFQFPN package pinout**



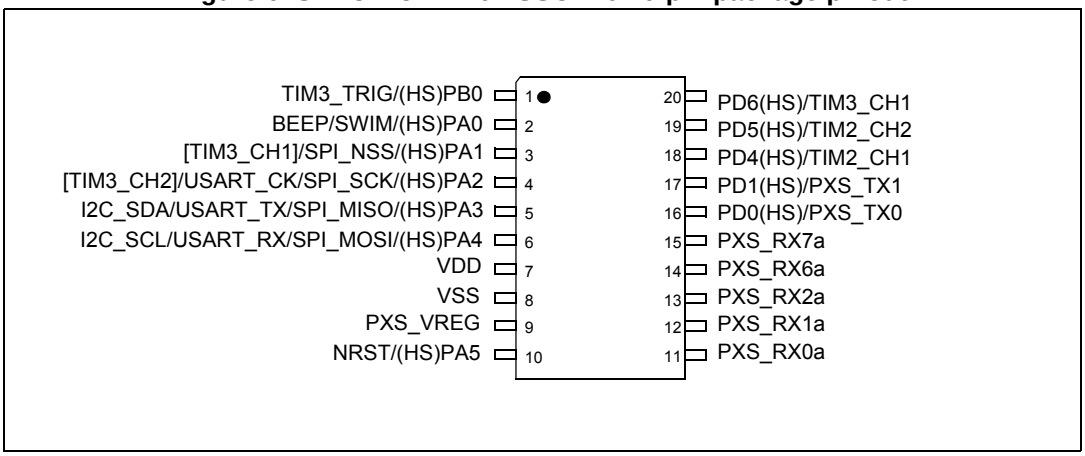

1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312) Section 6: Power supply.

**Figure 5. STM8TL53F4P6 TSSOP20 20-pin package pinout**




1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312) Section 6: Power supply.

**Figure 6. STM8TL52F4P6 TSSOP20 20-pin package pinout**




1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312) Section 6: Power supply.

**Table 3. Legends/abbreviations**

| | | |
|---|---|---|
| Type | I = input, O = output, S = power supply | |
| Level | Input | FT = 5 V tolerant, TC = 3 V capable |
| | Output | HS = high sink/source (20 mA) |
| Port and control configuration | Input | float = floating, wpu = weak pull-up |
| | Output | T = true open drain, OD = open drain, PP = push-pull |
| Reset state | Bold X (pin state after reset release).<br>Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state). | |

**Table 4. STM8TL5xx4 pin description**

| Pin no. | | | Pin name | Type | Input | | | | Output | | | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | UFQFPN28 | TSSOP20 | | | Level | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | Default | Remap |
| 1 | - | - | PB6/ PXS_TX14 | I/O | TC | X | X | X | HS | X | X | Port B6 | ProxSense transmit 14 | - |
| 2 | 27 | 2 | PA0[1]/SWIM/ BEEP | I/O | TC | X | X | X | HS | X | X | SWIM | Port A0[1] | - |
| | | | | | | | | | | | | | SWIM input and output | - |
| | | | | | | | | | | | | | Beep output | - |
| 3 | 28 | 3 | PA1/SPI_NSS/ [TIM3_CH1] | I/O | FT | X | X | X | HS | X | X | Port A1 | SPI master/ slave select | Timer 3 - channel 1 |
| 4 | 1 | 4 | PA2/SPI_SCK/ USART_CK/ [TIM3_CH2][2] | I/O | FT | X | X | X | HS | X | X | Port A2 | SPI clock | Timer 3 - channel 2 |
| | | | | | | | | | | | | | USART synchronous clock | |
| 5 | 2 | 5 | PA3/SPI_MISO/ USART_TX/ I2C_SDA[2] | I/O | FT | X | X | X | HS | X | X | Port A3 | SPI master in/ slave out | - |
| | | | | | | | | | | | | | USART transmit | - |
| | | | | | | | | | | | | | $I^2C$ data | - |
| 6 | 3 | 6 | PA4/SPI_MOSI/ USART_RX/ I2C_SCL | I/O | FT | X | X | X | HS | X | X | Port A4 | SPI master out/ slave in | - |
| | | | | | | | | | | | | | USART receive | - |
| | | | | | | | | | | | | | $I^2C$ clock | - |
| 7 | 4 | 7 | VDD | S | - | - | - | - | - | - | - | Digital power supply | - | - |

Table 4. STM8TL5xx4 pin description (continued)

| Pin no. | | | Pin name | Type | Input | | | | Output | | | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | UFQFPN28 | TSSOP20 | | | Level | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | Default | Remap |
| 8 | 5 | 8 | VSS | S | - | - | - | - | - | - | - | Digital ground | - | - |
| 9 | 6 | 9 | PXS_VREG | S | - | - | - | - | - | - | - | - | ProxSense voltage regulator External decoupling capacitor | - |
| 10 | 7 | 10 | PA5/NRST(3) | I/O | TC | - | - | - | HS | X | X | Reset | Port A5 (output only) | - |
| 11 | 8 | - | PA6/ PXS_TRIG/ CLK_CCO | I/O | FT | X | X | X | HS | X | X | Port A6 | ProxSense external trigger input | - |
| | | - | | | | | | | | | | | CLK clock output | - |
| 12 | 9 | - | PA7/PXS_RFIN | I/O | TC | X | X | X | HS | X | X | Port A7 | ProxSense antenna input | - |
| 13 | 10 | 11 | PXS_RX0a | - | - | - | - | - | - | - | - | PXS_RX0a | ProxSense receiver 0a | - |
| 14 | - | - | PXS_RX0b | - | - | - | - | - | - | - | - | PXS_RX0b | ProxSense receiver 0b | - |
| 15 | 11 | 12 | PXS_RX1a | - | - | - | - | - | - | - | - | PXS_RX1a | ProxSense receiver 1a | - |
| 16 | - | - | PXS_RX1b | - | - | - | - | - | - | - | - | PXS_RX1b | ProxSense receiver 1b | - |
| 17 | 12 | 13 | PXS_RX2a | - | - | - | - | - | - | - | - | PXS_RX2a | ProxSense receiver 2a | - |
| 18 | - | - | PXS_RX2b | - | - | - | - | - | - | - | - | PXS_RX | ProxSense receiver 2b | - |
| 19 | 13 | - | PXS_RX3a | - | - | - | - | - | - | - | - | PXS_RX3a | ProxSense receiver 3a | - |
| 20 | - | - | PXS_RX3b | - | - | - | - | - | - | - | - | PXS_RX3b | ProxSense receiver 3b | - |
| 21 | 14 | - | PXS_RX4a | - | - | - | - | - | - | - | - | PXS_RX4a | ProxSense receiver 4a | - |
| 22 | - | - | PXS_RX4b | - | - | - | - | - | - | - | - | PXS_RX4b | ProxSense receiver 4b | - |

Table 4. STM8TL5xx4 pin description (continued)

| Pin no. | | | Pin name | Type | Input | | | | Output | | | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | UFQFPN28 | TSSOP20 | | | Level | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | Default | Remap |
| 23 | 15 | - | PXS_RX5a | - | - | - | - | - | - | - | - | PXS_RX5a | ProxSense receiver 5a | - |
| 24 | - | - | PXS_RX5b | - | - | - | - | - | - | - | - | PXS_RX5b | ProxSense receiver 5b | - |
| 25 | 16 | 14 | PXS_RX6a | - | - | - | - | - | - | - | - | PXS_RX6a | ProxSense receiver 6a | - |
| 26 | - | - | PXS_RX6b | - | - | - | - | - | - | - | - | PXS_RX6b | ProxSense receiver 6b | - |
| 27 | 17 | 15 | PXS_RX7a | - | - | - | - | - | - | - | - | PXS_RX7a | ProxSense receiver 7a | - |
| 28 | - | - | PXS_RX7b | - | - | - | - | - | - | - | - | PXS_RX7b | ProxSense receiver 7b | - |
| 29 | - | - | PXS_RX8a | - | - | - | - | - | - | - | - | PXS_RX8a | ProxSense receiver 8a | - |
| 30 | - | - | PXS_RX8b | - | - | - | - | - | - | - | - | PXS_RX8b | ProxSense receiver 8b | - |
| 31 | - | - | PXS_RX9a | - | - | - | - | - | - | - | - | PXS_RX9a | ProxSense receiver 9a | - |
| 32 | - | - | PXS_RX9b | - | - | - | - | - | - | - | - | PXS_RX9b | ProxSense receiver 9b | - |
| 33 | 18 | 16 | PD0/PXS_TX0 | I/O | TC | X | X | X | HS | X | X | Port D0 | ProxSense transmitter 0 | - |
| 34 | 19 | 17 | PD1/PXS_TX1 | I/O | TC | X | X | X | HS | X | X | Port D1 | ProxSense transmitter 1 | - |
| 35 | 20 | - | PD2/PXS_TX2(4) | I/O | TC | X | X | X | HS | X | X | Port D2 | ProxSense transmitter 2(4) | - |
| 36 | 21 | - | PD3/PXS_TX3(4) | I/O | TC | X | X | X | HS | X | X | Port D3 | ProxSense transmitter 3(4) | - |
| 37 | - | - | VSSIO | S | - | - | - | - | - | - | - | IOs ground | - | - |
| 38 | - | - | VDDIO | S | - | - | - | - | - | - | - | IOs power supply | - | - |
| 39 | 22 | 18 | PD4/PXS_TX4(4) / TIM2_CH1 | I/O | TC | X | X | X | HS | X | X | Port D4 | ProxSense transmitter 4(4) | - |
| | | | | | | | | | | | | | Timer 2 - channel 1 | - |

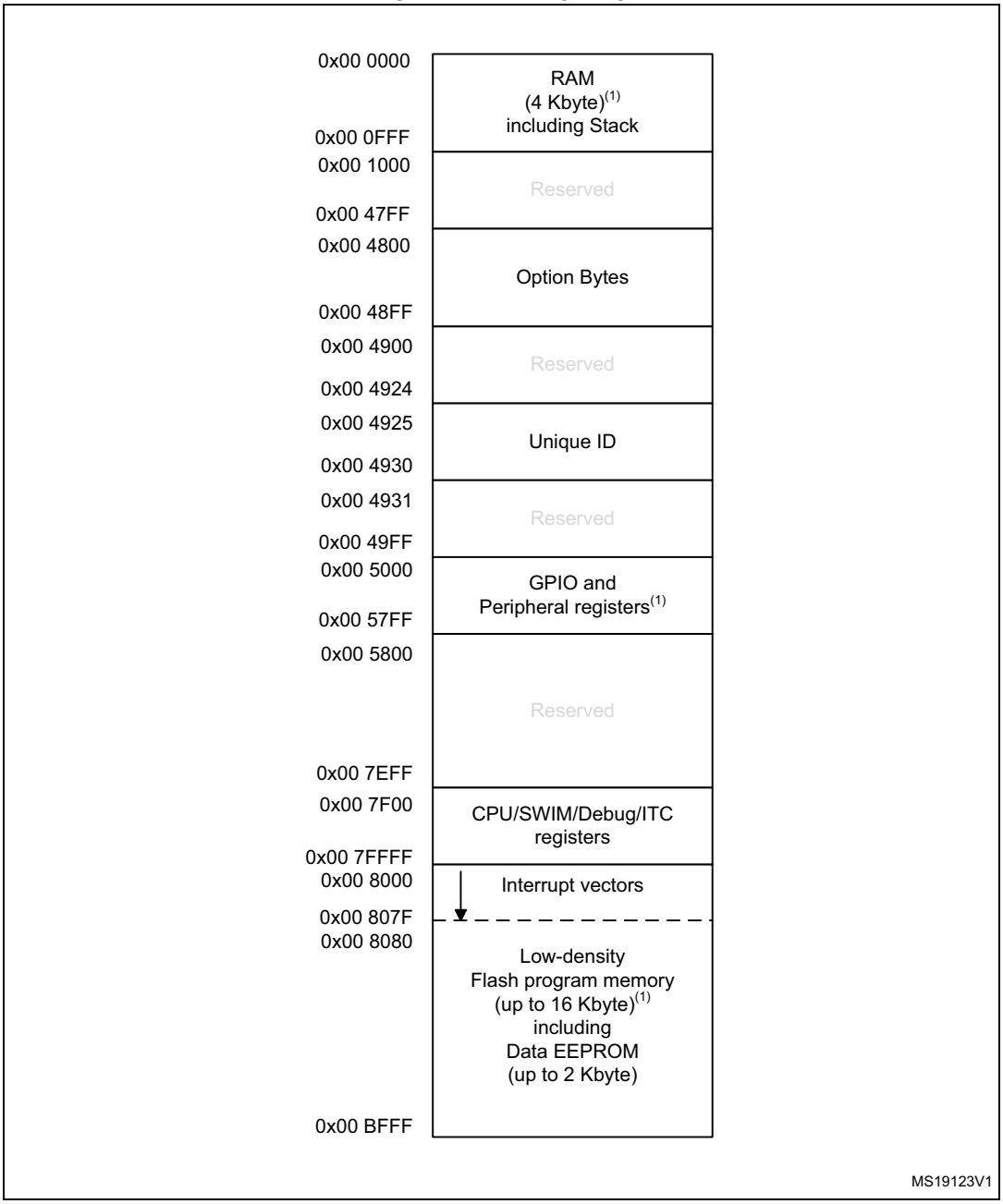
**Table 4. STM8TL5xx4 pin description (continued)**

| Pin no. | | | Pin name | Type | Input | | | | Output | | | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | UFQFPN28 | TSSOP20 | | | Level | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | Default | Remap |
| 40 | 23 | 19 | PD5/PXS_TX5(4) / TIM2_CH2 | I/O | TC | X | X | X | HS | X | X | Port D5 | ProxSense transmitter 5(4) | - |
| | | | | | | | | | | | | | Timer 2 - channel 2 | - |
| 41 | 24 | 20 | PD6/PXS_TX6(4) / TIM3_CH1 | I/O | TC | X | X | X | HS | X | X | Port D6 | ProxSense transmitter 6(4) | - |
| | | | | | | | | | | | | | Timer 3 - channel1 | - |
| 42 | 25 | | PD7/PXS_TX7(4) / TIM3_CH2 | I/O | TC | X | X | X | HS | X | X | Port D7 | ProxSense transmitter 7(4) | - |
| | | | | | | | | | | | | | Timer 3 - channel 2 | - |
| 43 | 26 | 1 | PB0/PXS_TX8(4) / TIM3_ETR | I/O | TC | X | X | X | HS | X | X | Port B0 | ProxSense transmitter 8(4) | - |
| | | | | | | | | | | | | | Timer 3 - external trigger | - |
| 44 | - | - | PB1(2)/PXS_TX9 / TIM2_ETR | I/O | TC | X | X | X | HS | X | X | Port B1 | ProxSense transmitter 9 | - |
| | - | - | | | | | | | | | | | Timer 2 - external trigger | - |
| 45 | - | - | PB2/PXS_TX10 | I/O | TC | X | X | X | HS | X | X | Port B2 | ProxSense transmitter 10 | - |
| 46 | - | - | PB3/PXS_TX11 | I/O | TC | X | X | X | HS | X | X | Port B3 | ProxSense transmitter 11 | - |
| 47 | - | - | PB4/PXS_TX12 | I/O | TC | X | X | X | HS | X | X | Port B4 | ProxSense transmitter 12 | - |
| 48 | - | - | PB5/PXS_TX13 | I/O | TC | X | X | X | HS | X | X | Port B5 | ProxSense transmitter 13 | - |

1. The PA0/SWIM pin is in input pull-up during the reset phase and after reset release.
2. A pull-up is applied to PA2, PA3 and PB1 during the reset phase. These three pins are input floating after reset release.
3. At power-up, the PA5/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA5), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section Configuring NRST/PA5 pin as general purpose output in the STM8TL5xxx reference manual (RM0312).
4. Not available for STM8TL52xx.

# 5 Memory and register map

**Figure 7. Memory map**




1. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

**Table 5. Flash and RAM boundary addresses**

| Memory area | Size | Start address | End address |
|---|---|---|---|
| **RAM** | 4 Kbyte | **0x00 0000** | 0x00 0FFF |
| Flash program memory | 16 Kbyte | 0x00 8000 | 0x00 BFFF |

**Table 6. I/O Port hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5000 | Port A | PA_ODR | Port A data output latch register | 0x00 |
| 0x00 5001 | | PA_IDR | Port A input pin value register | 0xXX |
| 0x00 5002 | | PA_DDR | Port A data direction register | 0x00 |
| 0x00 5003 | | PA_CR1 | Port A control register 1 | 0x00 |
| 0x00 5004 | | PA_CR2 | Port A control register 2 | 0x00 |
| 0x00 5005 | Port B | PB_ODR | Port B data output latch register | 0x00 |
| 0x00 5006 | | PB_IDR | Port B input pin value register | 0xXX |
| 0x00 5007 | | PB_DDR | Port B data direction register | 0x00 |
| 0x00 5008 | | PB_CR1 | Port B control register 1 | 0x00 |
| 0x00 5009 | | PB_CR2 | Port B control register 2 | 0x00 |
| 0x00 500A to 0x00 500E | Reserved area (5 byte) | | | |
| 0x00 500F | Port D | PD_ODR | Port D data output latch register | 0x00 |
| 0x00 5010 | | PD_IDR | Port D input pin value register | 0xXX |
| 0x00 5011 | | PD_DDR | Port D data direction register | 0x00 |
| 0x00 5012 | | PD_CR1 | Port D control register 1 | 0x00 |
| 0x00 5013 | | PD_CR2 | Port D control register 2 | 0x00 |

**Table 7. General hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5050 | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 5051 | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 5052 | | FLASH _PUKR | Flash Program memory unprotection register | 0x00 |
| 0x00 5053 | | FLASH _DUKR | Data EEPROM unprotection register | 0x00 |
| 0x00 5054 | | FLASH _IAPSR | Flash in-application programming status register | 0xX0 |
| 0x00 5055 to 0x00 509D | Reserved area (73 byte) | | | |
| 0x00 509E | SYSCFG | SYSCFG_RMPCR1 | Remapping control register 1 | 0x00 |
| 0x00 509F | Reserved area (1 byte) | | | |
| 0x00 50A0 | ITC-EXTI | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 | | EXTI_CR3 | External interrupt control register 3 | 0x00 |
| 0x00 50A3 | | EXTI_SR1 | External interrupt status register 1 | 0x00 |
| 0x00 50A4 | | EXTI_SR2 | External interrupt status register 2 | 0x00 |
| 0x00 50A5 | | EXTI_CONF | External interrupt port select register | 0x00 |
| 0x00 50A6 | WFE | WFE_CR1 | WFE control register 1 | 0x00 |
| 0x00 50A7 | | WFE_CR2 | WFE control register 2 | 0x00 |
| 0x00 50A8 to 0x00 50AF | Reserved area (8 byte) | | | |
| 0x00 50B0 | RST | RST_CR | Reset control register | 0x00 |
| 0x00 50B1 | | RST_SR | Reset status register | 0x01 (1) |
| 0x00 50B2 to 0x00 50BF | Reserved area (14 byte) | | | |
| 0x00 50C0 | CLK | CLK_CKDIVR | Clock divider register | 0x00 |
| 0x00 50C1 to 0x00 50C2 | | Reserved area (2 byte) | | |
| 0x00 50C3 | | CLK_PCKENR1 | Peripheral clock gating register 1 | 0x00 |
| 0x00 50C4 | | CLK_PCKENR2 | Peripheral clock gating register 2 | 0x01 |
| 0x00 50C5 | | CLK_CCOR | Configurable clock control register | 0x10 |
| 0x00 50C6 to 0x00 50D2 | Reserved area (12 byte) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 50D3 | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D4 | | WWDG_WR | WWDG window register | |
| 0x00 50D5 to 0x00 50D7 | Reserved area (11 byte) | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 byte) | | | |
| 0x00 50F0 | AWU | AWU_CSR | AWU control/status register | 0x00 |
| 0x00 50F1 | | AWU_APR | AWU asynchronous prescaler buffer register | 0x3F |
| 0x00 50F2 | | AWU_TBR | AWU timebase selection register | 0x00 |
| 0x00 50F3 | BEEP | BEEP_CSR | BEEP control/status register | 0x1F |
| 0x00 50F4 to 0x00 51FF | Reserved area (268 byte) | | | |
| 0x00 5200 | SPI | SPI_CR1 | SPI control register 1 | 0x00 |
| 0x00 5201 | | SPI_CR2 | SPI control register 2 | 0x00 |
| 0x00 5202 | | SPI_ICR | SPI interrupt control register | 0x00 |
| 0x00 5203 | | SPI_SR | SPI status register | 0x00 |
| 0x00 5204 | | SPI_DR | SPI data register | 0x00 |
| 0x00 5205 to 0x00 520F | Reserved area (11 byte) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5210 | I2C | I2C_CR1 | I2C control register 1 | 0x00 |
| 0x00 5211 | | I2C_CR2 | I2C control register 2 | 0x00 |
| 0x00 5212 | | I2C_FREQR | I2C frequency register | 0x00 |
| 0x00 5213 | | I2C_OAR1L | I2C own address register 1 low | 0x00 |
| 0x00 5214 | | I2C_OAR1H | I2C own address register 1 high | 0x00 |
| 0x00 5215 | | I2C_OAR2 | I2C own address register 2 | 0x00 |
| 0x00 5216 | | I2C_DR | I2C data register | 0x00 |
| 0x00 5217 | | I2C_SR1 | I2C status register 1 | 0x00 |
| 0x00 5218 | | I2C_SR2 | I2C status register 2 | 0x00 |
| 0x00 5219 | | I2C_SR3 | I2C status register 3 | 0x00 |
| 0x00 521A | | I2C_ITR | I2C interrupt control register | 0x00 |
| 0x00 521B | | I2C_CCRL | I2C Clock control register low | 0x00 |
| 0x00 521C | | I2C_CCRH | I2C Clock control register high | 0x00 |
| 0x00 521D | | I2C_TRISER | I2C TRISE register | 0x00 |
| 0x00 521E to 0x00 522F | Reserved area (18 byte) | | | |
| 0x00 5230 | USART | USART_SR | USART status register | 0xC0 |
| 0x00 5231 | | USART_DR | USART data register | 0xXX |
| 0x00 5232 | | USART_BRR1 | USART baud rate register 1 | 0x00 |
| 0x00 5233 | | USART_BRR2 | USART baud rate register 2 | 0x00 |
| 0x00 5234 | | USART_CR1 | USART control register 1 | 0x00 |
| 0x00 5235 | | USART_CR2 | USART control register 2 | 0x00 |
| 0x00 5236 | | USART_CR3 | USART control register 3 | 0x00 |
| 0x00 5237 | | USART_CR4 | USART control register 4 | 0x00 |
| 0x00 5238 to 0x00 524F | Reserved area (18 byte) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5250 | TIM2 | TIM2_CR1 | TIM2 control register 1 | 0x00 |
| 0x00 5251 | | TIM2_CR2 | TIM2 control register 2 | 0x00 |
| 0x00 5252 | | TIM2_SMCR | TIM2 slave mode control register | 0x00 |
| 0x00 5253 | | TIM2_ETR | TIM2 external trigger register | 0x00 |
| 0x00 5254 | | TIM2_IER | TIM2 interrupt enable register | 0x00 |
| 0x00 5255 | | TIM2_SR1 | TIM2 status register 1 | 0x00 |
| 0x00 5256 | | TIM2_SR2 | TIM2 status register 2 | 0x00 |
| 0x00 5257 | | TIM2_EGR | TIM2 event generation register | 0x00 |
| 0x00 5258 | | TIM2_CCMR1 | TIM2 capture/compare mode register 1 | 0x00 |
| 0x00 5259 | | TIM2_CCMR2 | TIM2 capture/compare mode register 2 | 0x00 |
| 0x00 525A | | TIM2_CCER1 | TIM2 capture/compare enable register 1 | 0x00 |
| 0x00 525B | | TIM2_CNTRH | TIM2 counter register high | 0x00 |
| 0x00 525C | | TIM2_CNTRL | TIM2 counter register low | 0x00 |
| 0x00 525D | | TIM2_PSCR | TIM2 prescaler register | 0x00 |
| 0x00 525E | | TIM2_ARRH | TIM2 auto-reload register high | 0xFF |
| 0x00 525F | | TIM2_ARRL | TIM2 auto-reload register low | 0xFF |
| 0x00 5260 | | TIM2_CCR1H | TIM2 capture/compare register 1 high | 0x00 |
| 0x00 5261 | | TIM2_CCR1L | TIM2 capture/compare register 1 low | 0x00 |
| 0x00 5262 | | TIM2_CCR2H | TIM2 capture/compare register 2 high | 0x00 |
| 0x00 5263 | | TIM2_CCR2L | TIM2 capture/compare register 2 low | 0x00 |
| 0x00 5264 | | TIM2_BKR | TIM2 break register | 0x00 |
| 0x00 5265 | | TIM2_OISR | TIM2 output idle state register | 0x00 |
| 0x00 5266 to 0x00 527F | Reserved area (26 byte) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5280 | TIM3 | TIM3_CR1 | TIM3 control register 1 | 0x00 |
| 0x00 5281 | | TIM3_CR2 | TIM3 control register 2 | 0x00 |
| 0x00 5282 | | TIM3_SMCR | TIM3 slave mode control register | 0x00 |
| 0x00 5283 | | TIM3_ETR | TIM3 external trigger register | 0x00 |
| 0x00 5284 | | TIM3_IER | TIM3 interrupt enable register | 0x00 |
| 0x00 5285 | | TIM3_SR1 | TIM3 status register 1 | 0x00 |
| 0x00 5286 | | TIM3_SR2 | TIM3 status register 2 | 0x00 |
| 0x00 5287 | | TIM3_EGR | TIM3 event generation register | 0x00 |
| 0x00 5288 | | TIM3_CCMR1 | TIM3 capture/compare mode register 1 | 0x00 |
| 0x00 5289 | | TIM3_CCMR2 | TIM3 capture/compare mode register 2 | 0x00 |
| 0x00 528A | | TIM3_CCER1 | TIM3 capture/compare enable register 1 | 0x00 |
| 0x00 528B | | TIM3_CNTRH | TIM3 counter register high | 0x00 |
| 0x00 528C | | TIM3_CNTRL | TIM3 counter register low | 0x00 |
| 0x00 528D | | TIM3_PSCR | TIM3 prescaler register | 0x00 |
| 0x00 528E | | TIM3_ARRH | TIM3 auto-reload register high | 0xFF |
| 0x00 528F | | TIM3_ARRL | TIM3 auto-reload register low | 0xFF |
| 0x00 5290 | | TIM3_CCR1H | TIM3 capture/compare register 1 high | 0x00 |
| 0x00 5291 | | TIM3_CCR1L | TIM3 capture/compare register 1 low | 0x00 |
| 0x00 5292 | | TIM3_CCR2H | TIM3 capture/compare register 2 high | 0x00 |
| 0x00 5293 | | TIM3_CCR2L | TIM3 capture/compare register 2 low | 0x00 |
| 0x00 5294 | | TIM3_BKR | TIM3 break register | 0x00 |
| 0x00 5295 | | TIM3_OISR | TIM3 output idle state register | 0x00 |
| 0x00 5296 to 0x00 52DF | Reserved area (74 byte) | | | |
| 0x00 52E0 | TIM4 | TIM4_CR1 | TIM4 control register 1 | 0x00 |
| 0x00 52E1 | | TIM4_CR2 | TIM4 control register 2 | 0x00 |
| 0x00 52E2 | | TIM4_SMCR | TIM4 Slave mode control register | 0x00 |
| 0x00 52E3 | | TIM4_IER | TIM4 interrupt enable register | 0x00 |
| 0x00 52E4 | | TIM4_SR1 | TIM4 Status register 1 | 0x00 |
| 0x00 52E5 | | TIM4_EGR | TIM4 event generation register | 0x00 |
| 0x00 52E6 | | TIM4_CNTR | TIM4 counter register | 0x00 |
| 0x00 52E7 | | TIM4_PSCR | TIM4 prescaler register | 0x00 |
| 0x00 52E8 | | TIM4_ARR | TIM4 auto-reload register low | 0xFF |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 52E9 to 0x00 52FF | Reserved area (23 byte) | | | |
| 0x00 5300 | PXS | PXS_CR1 | ProxSense control register 1 | 0x00 |
| 0x00 5301 | | PXS_CR2 | ProxSense control register 2 | 0x00 |
| 0x00 5302 | | PXS_CR3 | ProxSense control register 3 | 0x04 |
| 0x00 5303 | | Reserved area (1 byte) | | |
| 0x00 5304 | | PXS_ISR | ProxSense interrupt and status register | 0x00 |
| 0x00 5305 | | Reserved area (1 byte) | | |
| 0x00 5306 | | PXS_CKCR1 | ProxSense clock control register 1 | 0x30 |
| 0x00 5307 | | PXS_CKCR2 | ProxSense clock control register 2 | 0x11 |
| 0x00 5308 | | PXS_RXENRH | ProxSense receiver enable register high | 0x00 |
| 0x00 5309 | | PXS_RXENRL | ProxSense receiver enable register low | 0x00 |
| 0x00 5310 to 0x00 5311 | Reserved area (2 byte) | | | |
| 0x00 530A | PXS | PXS_RXCR1H | ProxSense receiver control register 1 high | 0x00 |
| 0x00 530B | | PXS_RXCR1L | ProxSense receiver control register 1 low | 0x00 |
| 0x00 530C | | PXS_RXCR2H | ProxSense receiver control register 2 high | 0x00 |
| 0x00 530D | | PXS_RXCR2L | ProxSense receiver control register 2 low | 0x00 |
| 0x00 530E | | PXS_RXCR3H | ProxSense receiver control register 3 high | 0x00 |
| 0x00 530F | | PXS_RXCR3L | ProxSense receiver control register 3 low | 0x00 |
| 0x00 5312 | | PXS_RXINSRH | ProxSense receiver inactive state register high | 0x00 |
| 0x00 5313 | | PXS_RXINSRL | ProxSense receiver inactive state register low | 0x00 |
| 0x00 5314 to 0x00 5315 | Reserved area (2 byte) | | | |
| 0x00 5316 | PXS | PXS_TXENRH | ProxSense transmit enable register high | 0x00 |
| 0x00 5317 | | PXS_TXENRL | ProxSense transmit enable register low | 0x00 |
| 0x00 5318 to 0x00 5319 | Reserved area (2 byte) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0X00 531A | PXS | PXS_MAXRH | ProxSense maximum counter value register high | 0xFF |
| 0x00 531B | | PXS_MAXRL | ProxSense maximum counter value register low | 0xFF |
| 0x00 531C | | PXS_MAXENRH | ProxSense maximum counter enable register high | 0x00 |
| 0x00 531D | | PXS_MAXENRL | ProxSense maximum counter enable register low | 0x00 |
| 0x00 531E | | PXS_RXSRH | ProxSense receiver status register high | 0x00 |
| 0x00 531F | | PXS_RXSRL | ProxSense receiver status register low | 0x00 |
| 0x00 5320 | | PXS_RX0CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 5321 | | PXS_RX0CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 5322 | | PXS_RX1CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 5323 | | PXS_RX1CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 5324 | | PXS_RX2CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 5325 | PXS | PXS_RX2CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 5326 | | PXS_RX3CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 5327 | | PXS_RX3CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 5328 | | PXS_RX4CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 5329 | | PXS_RX4CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 532A | | PXS_RX5CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 532B | | PXS_RX5CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 532C | | PXS_RX6CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 532D | | PXS_RX6CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 532E | | PXS_RX7CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 532F | | PXS_RX7CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 5330 | | PXS_RX8CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 5331 | | PXS_RX8CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 5332 | | PXS_RX9CNTRH | ProxSense counter register receiver channel high | 0x00 |
| 0x00 5333 | | PXS_RX9CNTRL | ProxSense counter register receiver channel low | 0x00 |
| 0x00 5334 to 0x00 533F | Reserved area (12 byte) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5340 | PXS | PXS_RX0CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 5341 | | PXS_RX1CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 5342 | | PXS_RX2CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 5343 | | PXS_RX3CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 5344 | | PXS_RX4CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 5345 | | PXS_RX5CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 5346 | | PXS_RX6CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 5347 | | PXS_RX7CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 5348 | | PXS_RX8CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 5349 | | PXS_RX9CSSELR | ProxSense receiver sampling capacitor selection register | 0x00 |
| 0x00 534A to 0x00 534F | Reserved area (6 byte) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5350 | PXS | PXS_RX0EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 5351 | | PXS_RX1EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 5352 | | PXS_RX2EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 5353 | | PXS_RX3EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 5354 | | PXS_RX4EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 5355 | | PXS_RX5EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 5356 | | PXS_RX6EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 5357 | | PXS_RX7EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 5358 | | PXS_RX8EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 5359 | | PXS_RX9EPCCSELR | ProxSense receiver electrode parasitic compensation capacitor selection register | 0x00 |
| 0x00 535A to 0x00 7EFF | Reserved area (11174 byte) | | | |

1. After power-on reset.

**Table 8. CPU/SWIM/debug module/interrupt controller registers**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F00 | CPU | A | Accumulator | 0x00 |
| 0x00 7F01 | | PCE | Program counter extended | 0x00 |
| 0x00 7F02 | | PCH | Program counter high | 0x80 |
| 0x00 7F03 | | PCL | Program counter low | 0x00 |
| 0x00 7F04 | | XH | X index register high | 0x00 |
| 0x00 7F05 | | XL | X index register low | 0x00 |
| 0x00 7F06 | | YH | Y index register high | 0x00 |
| 0x00 7F07 | | YL | Y index register low | 0x00 |
| 0x00 7F08 | | SPH | Stack pointer high | 0x05 |
| 0x00 7F09 | | SPL | Stack pointer low | 0xFF |
| 0x00 7F0A | | CC | Condition code register | 0x28 |

**Table 8. CPU/SWIM/debug module/interrupt controller registers (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F0B to 0x00 7F5F | Reserved area (85 byte) | | | |
| 0x00 7F60 | CFG | CFG_GCR | Global configuration register | 0x00 |
| 0x00 7F61 0x00 7F6F | Reserved area (15 byte) | | | |
| 0x00 7F70 | ITC-SPR (1) | ITC_SPR1 | Interrupt Software priority register 1 | 0xFF |
| 0x00 7F71 | | ITC_SPR2 | Interrupt Software priority register 2 | 0xFF |
| 0x00 7F72 | | ITC_SPR3 | Interrupt Software priority register 3 | 0xFF |
| 0x00 7F73 | | ITC_SPR4 | Interrupt Software priority register 4 | 0xFF |
| 0x00 7F74 | | ITC_SPR5 | Interrupt Software priority register 5 | 0xFF |
| 0x00 7F75 | | ITC_SPR6 | Interrupt Software priority register 6 | 0xFF |
| 0x00 7F76 | | ITC_SPR7 | Interrupt Software priority register 7 | 0xFF |
| 0x00 7F77 | | ITC_SPR8 | Interrupt Software priority register 8 | 0xFF |
| 0x00 7F78 to 0x00 7F79 | Reserved area (2 byte) | | | |
| 0x00 7F80 | SWIM | SWIM_CSR | SWIM control status register | 0x00 |
| 0x00 7F81 to 0x00 7F8F | Reserved area (15 byte) | | | |
| 0x00 7F90 | DM | DM_BK1RE | Breakpoint 1 register extended byte | 0xFF |
| 0x00 7F91 | | DM_BK1RH | Breakpoint 1 register high byte | 0xFF |
| 0x00 7F92 | | DM_BK1RL | Breakpoint 1 register low byte | 0xFF |
| 0x00 7F93 | | DM_BK2RE | Breakpoint 2 register extended byte | 0xFF |
| 0x00 7F94 | | DM_BK2RH | Breakpoint 2 register high byte | 0xFF |
| 0x00 7F95 | | DM_BK2RL | Breakpoint 2 register low byte | 0xFF |
| 0x00 7F96 | | DM_CR1 | Debug module control register 1 | 0x00 |
| 0x00 7F97 | | DM_CR2 | Debug module control register 2 | 0x00 |
| 0x00 7F98 | | DM_CSR1 | Debug module control/status register 1 | 0x10 |
| 0x00 7F99 | | DM_CSR2 | Debug module control/status register 2 | 0x00 |
| 0x00 7F9A | | DM_ENFCTR | Enable function register | 0xFF |

1. Refer to *Table 7: General hardware register map on page 28* (addresses 0x00 50A0 to 0x00 50A5) for a list of external interrupt registers.

# 6 Interrupt vector mapping

**Table 9. Interrupt mapping**

| IRQ No. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Wakeup from Wait (WFI mode) | Wakeup from Wait (WFE mode)(1) | Vector address |
|---|---|---|---|---|---|---|---|
| | RESET | Reset | Yes | Yes | Yes | Yes | 0x00 8000 |
| | TRAP | Software interrupt | - | - | - | - | 0x00 8004 |
| 0 | Reserved | | | | | | 0x00 8008 |
| 1 | FLASH | FLASH end of programing/ write attempted to protected page interrupt | - | - | Yes | Yes | 0x00 800C |
| 2 | PXS | End of conversion/First conversion completed | - | Yes(2) | Yes | Yes | 0x00 8010 |
| 3 | Reserved | | | | | | 0x00 8011 -0x00 8017 |
| 4 | AWU | Auto wakeup from Halt | - | Yes | Yes | Yes | 0x00 8018 |
| 5 | Reserved | | | | | | 0x00 801C |
| 6 | EXTIB | External interrupt port B | Yes | Yes | Yes | Yes | 0x00 8020 |
| 7 | EXTID | External interrupt port D | Yes | Yes | Yes | Yes | 0x00 8024 |
| 8 | EXTI0 | External interrupt 0 | Yes | Yes | Yes | Yes | 0x00 8028 |
| 9 | EXTI1 | External interrupt 1 | Yes | Yes | Yes | Yes | 0x00 802C |
| 10 | EXTI2 | External interrupt 2 | Yes | Yes | Yes | Yes | 0x00 8030 |
| 11 | EXTI3 | External interrupt 3 | Yes | Yes | Yes | Yes | 0x00 8034 |
| 12 | EXTI4 | External interrupt 4 | Yes | Yes | Yes | Yes | 0x00 8038 |
| 13 | EXTI5 | External interrupt 5 | Yes | Yes | Yes | Yes | 0x00 803C |
| 14 | EXTI6 | External interrupt 6 | Yes | Yes | Yes | Yes | 0x00 8040 |
| 15 | EXTI7 | External interrupt 7 | Yes | Yes | Yes | Yes | 0x00 8044 |
| 16 | Reserved | | | | | | 0x00 8048 |
| 17 | Reserved | | | | | | 0x00 804C -0x00 804F |
| 18 | Reserved | | | | | | 0x00 8050 |
| 19 | TIM2 | TIM2 update/overflow/ trigger/break interrupt | - | - | Yes | Yes | 0x00 8054 |
| 20 | TIM2 | TIM2 capture/compare interrupt | - | - | Yes | Yes | 0x00 8058 |
| 21 | TIM3 | TIM3 update/overflow/ trigger/break interrupt | - | - | Yes | Yes | 0x00 805C |

**Table 9. Interrupt mapping (continued)**

| IRQ No. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Wakeup from Wait (WFI mode) | Wakeup from Wait (WFE mode)(1) | Vector address |
|---|---|---|---|---|---|---|---|
| 22 | TIM3 | TIM3 capture/compare interrupt | - | - | Yes | Yes | 0x00 8060 |
| 23-24 | Reserved | | | | | | 0x00 8064-0x00 806B |
| 25 | TIM4 | TIM4 update/overflow/ trigger interrupt | - | - | Yes | Yes | 0x00 806C |
| 26 | SPI | SPI TX buffer empty/ RX buffer not empty/ error/wakeup interrupt | Yes | Yes | Yes | Yes | 0x00 8070 |
| 27 | USART | USART transmit data register empty/ transmission complete interrupt | - | - | Yes | Yes | 0x00 8074 |
| 28 | USART | USART received data ready/overrun error/ idle line detected/parity error/global error interrupt | - | - | Yes | Yes | 0x00 8078 |
| 29 | I2C | I2C interrupt(3) | Yes | Yes | Yes | Yes | 0x00 807C |

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. ProxSense activated before executing HALT instruction.
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

# 7 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated row of the memory.

All option byte can be modified only in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 10* for details on option byte addresses.

Refer to the STM8TL5xxx Flash programming manual (PM0212) and STM8 SWIM and debug manual (UM0470) for information on SWIM programming procedures.

**Table 10. Option byte**

| Addr. | Option name | Option byte No. | Option bits | | | | | | | | Factory default setting |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x4800 | Read-out protection (ROP) | OPT0 | ROP[7:0] | | | | | | | | 0xAA |
| 0x4801 | - | - | Must be programmed to 0x00 | | | | | | | | 0x00 |
| 0x4802 | User Boot code size (UBC) | OPT1 | UBC[7:0] | | | | | | | | 0x00 |
| 0x4803 | DATASIZE | OPT2 | DATASIZE[7:0] | | | | | | | | 0x00 |
| 0x4807 | PCODESIZE | OPT3 | PCODESIZE[7:0] | | | | | | | | 0x00 |
| 0x4808 | Window watchdog and independent window watchdog | OPT4 [3:0] | Reserved | | | | WWDG_HALT | WWDG_HW | IWDG_HALT | IWDG_HW | 0x00 |

**Table 11. Option byte description**

| Option byte number | Description |
|---|---|
| OPT0 | **ROP[7:0]** *Memory readout protection (ROP)*<br>0xAA: Readout protection disabled (write access via SWIM protocol)<br>Refer to *Read-out protection* section in the STM8TL5xxx reference manual (RM0312) for details. |
| OPT1 | **UBC[7:0]** *Size of the user boot code area*<br>0x00: no UBC<br>0x01-0x02: UBC contains only the interrupt vectors.<br>0x03: Page 0 and 1 reserved for the interrupt vectors. Page 2 is available to store user boot code. Memory is write protected<br>...<br>0xFF: Page 0 to 254 reserved for UBC, memory is write protected<br>Refer to *User boot area (UBC)* section in the STM8TL5xxx reference manual (RM0312) for more details. |

**Table 11. Option byte description (continued)**

| Option byte number | Description |
|---|---|
| OPT2 | **DATASIZE[7:0]** Size of the data EEPROM area<br>0x00: no data EEPROM area<br>0x01: 1 page reserved for data storage from 0xBFC0 to 0xBFFF<br>0x02: 2 pages reserved for data storage from 0xBF80 to 0xBFFF<br>...<br>0x20: 32 pages reserved for data storage from 0xB800 to 0xBFFF<br>Refer to *Data EEPROM (DATA)* section in the STM8TL5xxx reference manual (RM0312) for more details. |
| OPT3 | **PCODESIZE[7:0]** Size of the proprietary code area<br>0x00: No proprietary code area<br>0x03: TRAP vector and page 2 (0x8080 to 0x80BF) reserved for the proprietary code and read/write protected<br>...<br>0xFF: TRAP vector and page 2 to 254 (0x8080 to 0xBFBF) reserved for the proprietary code and read/write protected<br>Refer to Proprietary code area (PCODE) section in the STM8TLxxxx Programming Manual(PM0212) for more details. |
| OPT4 | **IWDG_HW:** *Independent watchdog*<br>0: Independent watchdog activated by software<br>1: Independent watchdog activated by hardware |
| | **IWDG_HALT:** *Independent window watchdog reset on Halt/Active-halt*<br>0: Independent watchdog continues running in Halt/Active-halt mode<br>1: Independent watchdog stopped in Halt/Active-halt mode |
| | **WWDG_HW:** *Window watchdog*<br>0: Window watchdog activated by software<br>1: Window watchdog activated by hardware |
| | **WWDG_HALT:** *Window watchdog reset on Halt/Active-halt*<br>0: Window watchdog stopped in Halt/Active-halt mode<br>1: Window watchdog continues running in Halt/Active-halt mode |

**Caution:** After a device reset, read access to the program memory is not guaranteed if address 0x4807 is not programmed to 0x00.

# 8 Unique ID

STM8TL5xx4 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory
- To activate secure boot processes

**Table 12. Unique ID registers (96 bits)**

| Address | Content description | Unique ID bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x4925 | X coordinate on the wafer | U_ID[7:0] | | | | | | | |
| 0x4926 | | U_ID[15:8] | | | | | | | |
| 0x4927 | Y coordinate on the wafer | U_ID[23:16] | | | | | | | |
| 0x4928 | | U_ID[31:24] | | | | | | | |
| 0x4929 | Wafer number | U_ID[39:32] | | | | | | | |
| 0x492A | Lot number | U_ID[47:40] | | | | | | | |
| 0x492B | | U_ID[55:48] | | | | | | | |
| 0x492C | | U_ID[63:56] | | | | | | | |
| 0x492D | | U_ID[71:64] | | | | | | | |
| 0x492E | | U_ID[79:72] | | | | | | | |
| 0x492F | | U_ID[87:80] | | | | | | | |
| 0x4930 | | U_ID[95:88] | | | | | | | |

# 9 Electrical parameters

## 9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to $V_{SS}$.

### 9.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature of $T_A$= 25 °C and $T_A$ = $T_A$ max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

### 9.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3 V. They are given only as design guidelines and are not tested.

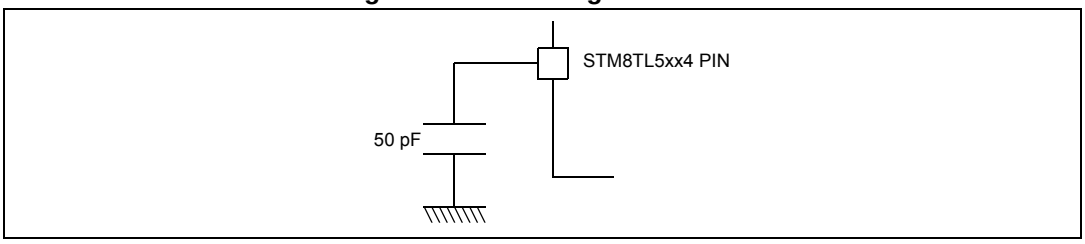
### 9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

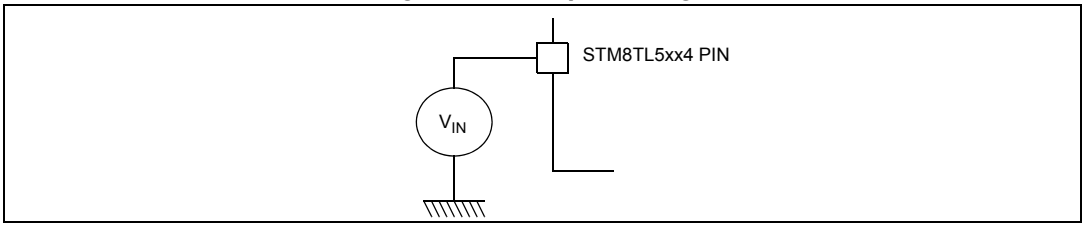
**Figure 8. Pin loading conditions**



### 9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

**Figure 9. Pin input voltage**




## 9.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 13. Voltage characteristics**

| Symbol | Ratings | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$- $V_{SS}$ | External supply voltage (including $V_{DD}$ and $V_{DDIO}$)(1) | | −0.3 | 4.0 | V |
| $V_{IN}$(2) | Receiver channel pins (PXS_Rx0a...Rx9b) | | $V_{SS}$−0.3 | PXS_$V_{REG}$ (~1.45) | |
| | Input voltage on PB0...7 and PD0...7(3) | Pins used as General purpose I/O | $V_{SS}$−0.3 | 4.0 | |
| | | Pins used as transmitter channel pins (PXS_Tx0 to PXS_Tx15) | $V_{SS}$−0.3 | PXS_$V_{REG}$ (~1.45) | |
| | Input voltage on any PA pins | | $V_{SS}$−0.3 | 4.0 | |
| $V_{ESD}$ | Electrostatic discharge voltage | see *Absolute maximum ratings (electrical sensitivity) on page 69* | | | |

1. All power ($V_{DD}$, $V_{DDIO}$) and ground ($V_{SS}$, $V_{SSIO}$) pins must always be connected to the external power supply.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 14.* for maximum allowed injected current values.
3. Current injection on these pins is not allowed.

**Table 14. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ power line (source) | 80 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground line (sink) | 80 | |
| $I_{IO}$ | Output current sunk by any other I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | –25 | |
| $I_{INJ(PIN)}$(1) | Injected current on PA pins(2) | ±5 | |
| $I_{INJ(PIN)}$ | Injected current on PB pins | 0 | |
| $I_{INJ(PIN)}$ | Injected current on PD pins | 0 | |
| $\Sigma I_{INJ(PIN)}$(1) | Total injected current (sum of all I/O and control pins)(2) | ±25 | |

1. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding $V_{IN}$ maximum must always be respected.
2. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

**Table 15. Thermal characteristics**

| Symbol | Ratings | Min | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | ° C |
| $T_J$ | Maximum junction temperature | 150 | |

## 9.3 Operating conditions

Subject to general operating conditions for $V_{DD}$ and $T_A$.

### 9.3.1 General operating conditions

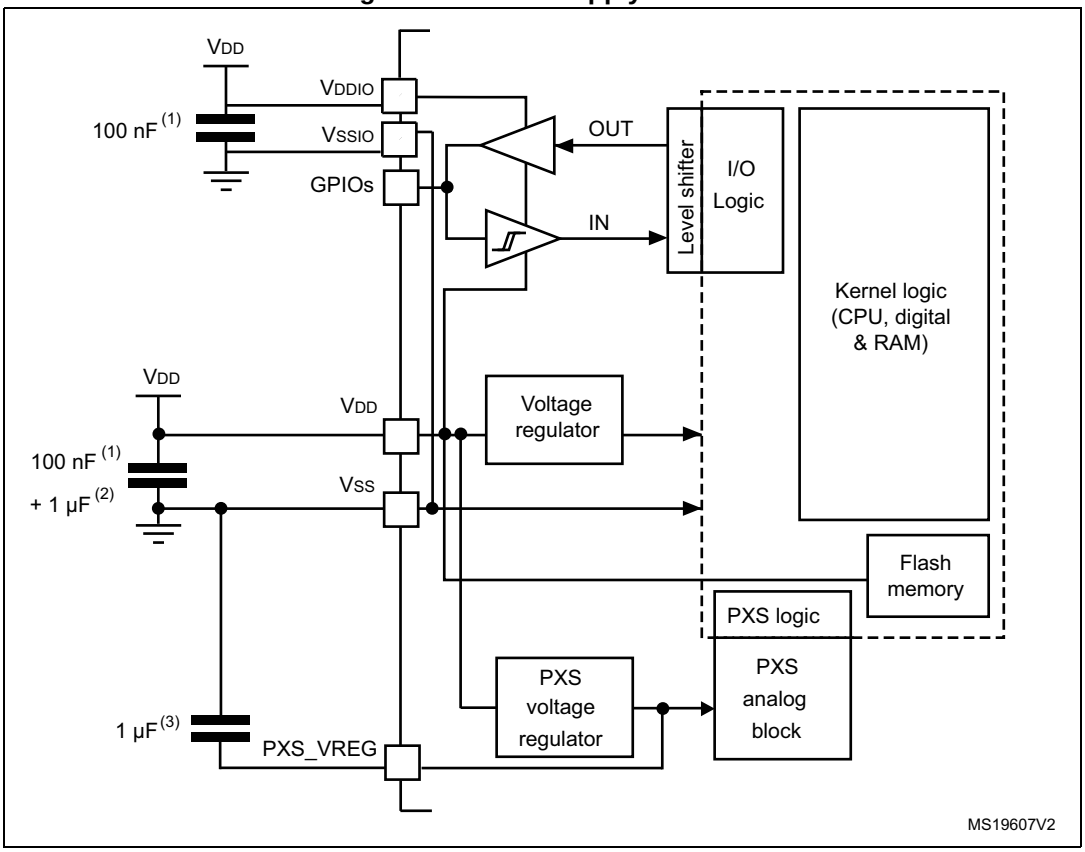
**Table 16. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MASTER}$(1) | Master clock frequency | 1.65 V ≤ $V_{DD}$ < 3.6 V | 2 | 16 | MHz |
| $V_{DD}$ | Standard operating voltage | - | 1.65 | 3.6 | V |
| $P_D$(2) | Power dissipation at $T_A$= 85 °C for suffix 2 devices | UQFPN48 | - | 625 | mW |
| | | UQFPN28 | - | 250 | |
| | | TSSOP20 | | 180 | |
| $T_A$ | Temperature range | 1.65 V ≤ $V_{DD}$ < 3.6 V | –40 | 85 | °C |
| $T_J$ | Junction temperature range | –40 °C ≤ $T_A$ ≤ 85 °C | –40 | 105 | |

1. $f_{MASTER}$ = $f_{CPU}$.
2. To calculate $P_{Dmax}(T_A)$ use the formula given in thermal characteristics $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with $T_{Jmax}$ in this table and $\Theta_{JA}$ in table “Thermal characteristics”.

### 9.3.2 Power supply

**Figure 10. Power supply scheme**




1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins to ensure the correct functionality of the device.
2. The 1µF capacitor must be connected to the $V_{DD}$ pin.
3. The 1µF ceramic capacitor connected to PXS_VREG must be low ESR (ESR ≤ 1Ω).

### 9.3.3 Power-up / power-down operating conditions

**Table 17. Operating conditions at power-up / power-down**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 20 | - | 1300 | µs/V |
| $t_{TEMP}$ | Reset release delay | $V_{DD}$ rising | - | 1 | - | ms |
| $V_{POR}$ | Power on reset threshold | | 1.44(2) | - | 1.65(1) | V |
| $V_{PDR}$ | Power down reset threshold | | 1.30(2) | - | 1.60(2) | V |

1. Tested in production.
2. Data based on characterization results, not tested in production.

### 9.3.4 ProxSense Regulator Voltage

**Table 18. ProxSense voltage regulator characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{reg}$ (1) | Voltage regulator decoupling capacitance (2) | - | 0.5 | 1 | 10 | µF |
| $V_{reg}$ | Regulated voltage during acquisition | - | - | 1.45 | - | V |

1. The capacitor must be routed as close as PXS_VREG as possible (≤ 1cm)
2. Equivalent serial resistor ≤ 1Ω

### 9.3.5 Supply current characteristics

#### Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except if explicitly mentioned

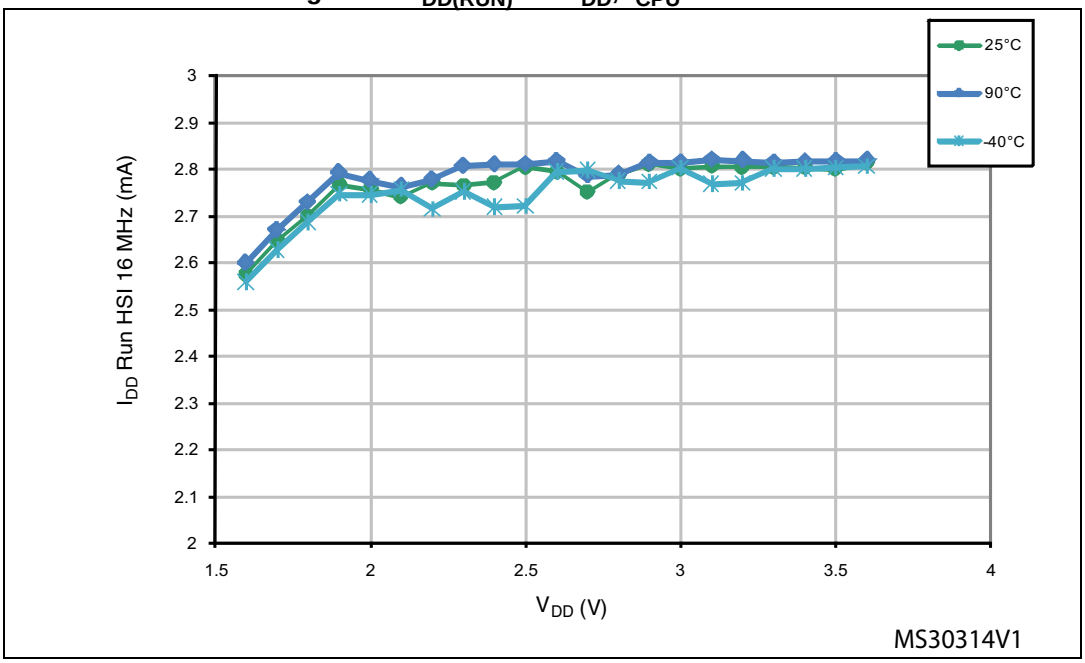
Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 19. Total current consumption in Run mode (1)**

| Symbol | Parameter | Conditions(2) | | Typ. | Max.(3) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\ (Run)}$ | Supply current in Run mode | Code executed from RAM | $f_{MASTER}$ = 2 MHz | 0.4 | 0.6 | mA |
| | | | $f_{MASTER}$ = 4 MHz | 0.55 | 0.7 | |
| | | | $f_{MASTER}$ = 8 MHz | 0.9 | 1.2 | |
| | | | $f_{MASTER}$ = 16 MHz | 1.6 | 2.1(4) | |
| | | Code executed from Flash | $f_{MASTER}$ = 2 MHz | 0.56 | 0.7 | |
| | | | $f_{MASTER}$ = 4 MHz | 0.88 | 1.8 | |
| | | | $f_{MASTER}$ = 8 MHz | 1.5 | 2.5 | |
| | | | $f_{MASTER}$ = 16 MHz | 2.8 | 3.5 | |

1. Based on characterization results, unless otherwise specified.
2. All peripherals off, $V_{DD}$ from 1.65 V to 3.6 V, HSI internal RC oscillator, $f_{CPU}=f_{MASTER}$.
3. Maximum values are given for $T_A$ = – 40 to 85 °C.
4. Tested in production.

Figure 11. $I_{DD(RUN)}$ vs. $V_{DD}$, $f_{CPU}$ = 16 MHz



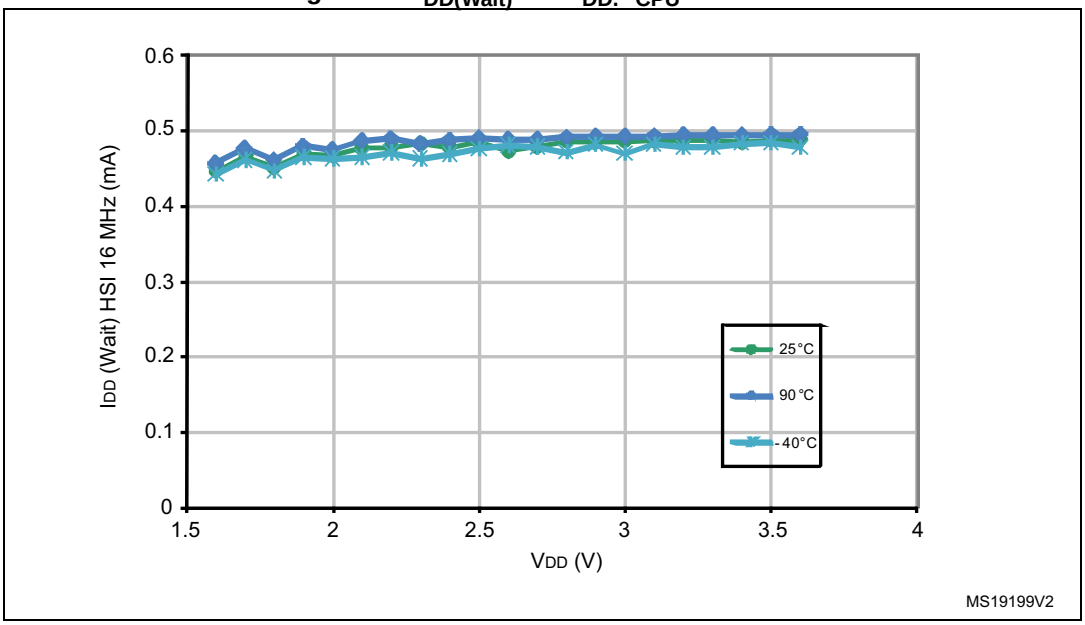

1. Typical current consumption measured with code executed from Flash.

Table 20. Total current consumption in Wait mode(1)

| Symbol | Parameter | Conditions | | Typ. | Max.(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(Wait)}$ | Supply current in Wait mode | CPU not clocked, all peripherals off, HSI internal RC osc | $f_{MASTER}$ = 2 MHz | 260 | 400 | µA |
| | | | $f_{MASTER}$ = 4 MHz | 300 | 450 | |
| | | | $f_{MASTER}$ = 8 MHz | 380 | 600 | |
| | | | $f_{MASTER}$ = 16 MHz | 500 | 800 | |

1. Based on characterization results, unless otherwise specified.
2. Maximum values are given for $T_A$ = –40 to 85 °C.

**Figure 12. $I_{DD(Wait)}$ vs. $V_{DD}$, $f_{CPU}$ = 16 MHz**



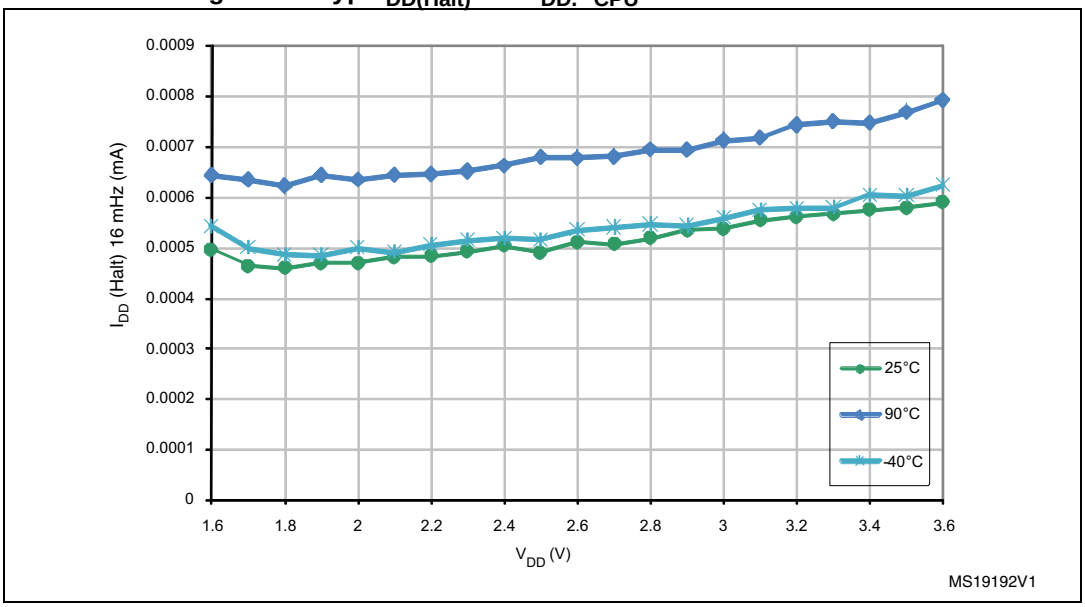

1. Typical current consumption measured with code executed from RAM.

**Table 21. Total current consumption in Halt mode and Active-halt mode $V_{DD}$ = 1.65 V to 3.6 V(1) (2)**

| Symbol | Parameter | Conditions | | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(AH)}$ | Supply current in Active-halt mode | LSI RC osc. (at 38 kHz) | $T_A$ = –40 °C to 25 °C | 1 | 2 | µA |
| | | | $T_A$ = 85 °C | 1.4 | 3.2 | µA |
| $I_{DD(WUProx)}$ | Supply current during wakeup time from Active halt mode (using HSI) | $f_{CPU}$ = 16 MHz | | 2 | - | mA |
| $t_{WU(AH)}$(3) | Wakeup time from Active-halt mode to Run mode | $f_{CPU}$= 16 MHz | | 4 | 6.5 | µs |
| $I_{DD(Halt)}$ | Supply current in Halt mode | $T_A$ = –40 °C to 25 °C | | 0.4 | 1.2(4) | µA |
| | | $T_A$ = 85 °C | | 1 | 2.5(4) | µA |
| $I_{DD(WUFH)}$ | Supply current during wakeup time from Halt mode | $f_{CPU}$ = 16 MHz | | 2 | - | mA |
| $t_{WU(Halt)}$ | Wakeup time from Halt mode to Run mode | $f_{CPU}$ = 16 MHz | | 4 | 6.5 | µs |

1. $T_A$ = –40 to 85 °C, no floating I/O, unless otherwise specified.
2. Data based on characterization, not tested in production.
3. Measured from interrupt event to interrupt vector fetch. To get $t_{WU}$ for another CPU frequency use $t_{WU}(FREQ) = t_{WU}(16\ MHz) + 1.5\ (T_{FREQ}-T_{16\ MHz})$. The first word of interrupt routine is fetched 5 CPU cycles after $t_{WU}$.
4. Tested in production.

**Figure 13. Typ. $I_{DD(Halt)}$ vs. $V_{DD}$, $f_{CPU}$ = 2 MHz and 16 MHz**




1. Typical current consumption measured with code executed from Flash.

### Current consumption of on-chip peripherals

Measurement made for $f_{MASTER}$ = from 2 MHz to 16 MHz

**Table 22. Peripheral current consumption**

| Symbol | Parameter | Typ. $V_{DD}$ = 3.0 V | Unit |
|---|---|---|---|
| $I_{DD(TIM2)}$ | TIM2 supply current(1) | 9 | µA/MHz |
| $I_{DD(TIM3)}$ | TIM3 supply current(1) | 9 | |
| $I_{DD(TIM4)}$ | TIM4 timer supply current(1) | 4 | |
| $I_{DD(USART)}$ | USARTsupply current(2) | 7 | |
| $I_{DD(SPI)}$ | SPI supply current(2) | 4 | |
| $I_{DD(I^2C)}$ | I2C supply current(2) | 4 | |

1. Data based on a differential $I_{DD}$ measurement between all peripherals off and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pin toggling. Not tested in production.
2. Data based on a differential $I_{DD}$ measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pin toggling. Not tested in production.

### Current consumption with ProxSense peripherals

Measurement made for $f_{MASTER}$ = 16 MHz, $f_{ProxSense}$ = 16 MHz, all other peripherals off and under the following conditions:

PXS_Rx*i*CSSELR (Sampling Capacitor) = 0x10

PXS_Rx*i*EPCCSELR (Electrode Parasitic Capacitance Compensation) = 0x80

Capacitance between Tx and Rx of 10nF

**Table 23. ProxSense peripheral current consumption(1)**

| Symbol | ProxSense transmitter Tx | ProxSense receiver Rx | Typical | Unit |
|---|---|---|---|---|
| $I_{DD(PXS)}$ | 1 | 1 | 0.6 | mA |
| | 1 | 4 | 1.1 | |
| | 1 | 10 | 2.3 | |

1. Data based on characterization, not tested in production

## 9.3.6 Clock and timing characteristics

### Internal clock source

The parameters given in *Table 24* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage. They are subject to general operating conditions for $V_{DD}$ and $T_A$.

### High speed internal RC oscillator

**Table 24. HSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | $V_{DD}$ = 3.0 V | - | 16 | - | MHz |
| $ACC_{HSI}$ | Accuracy of HSI oscillator (factory calibrated) | $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | –1 | - | 1 | % |
| | | 1.65 V ≤ VDD ≤ 3.6 V, $T_A$ = -40 to 85°C | –3 | - | 3 | % |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | - | 70 | 100 | µA |

1. $V_{DD}$ = 3V, $T_A$ = –40 to 125 °C, unless otherwise specified.

**Figure 14. Typical HSI frequency vs. $V_{DD}$**

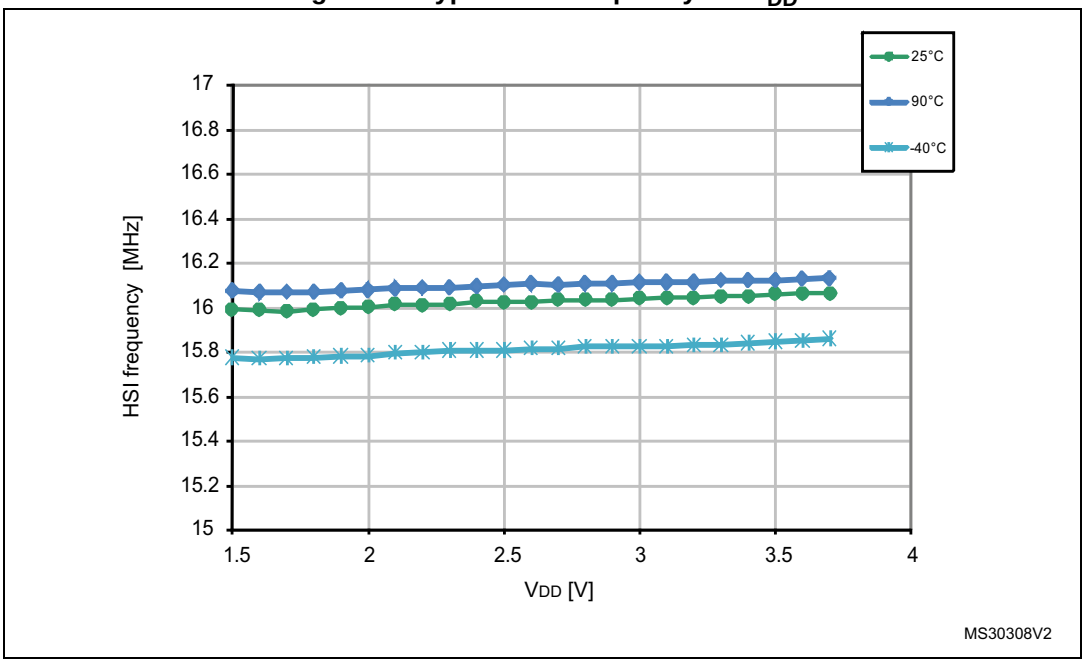
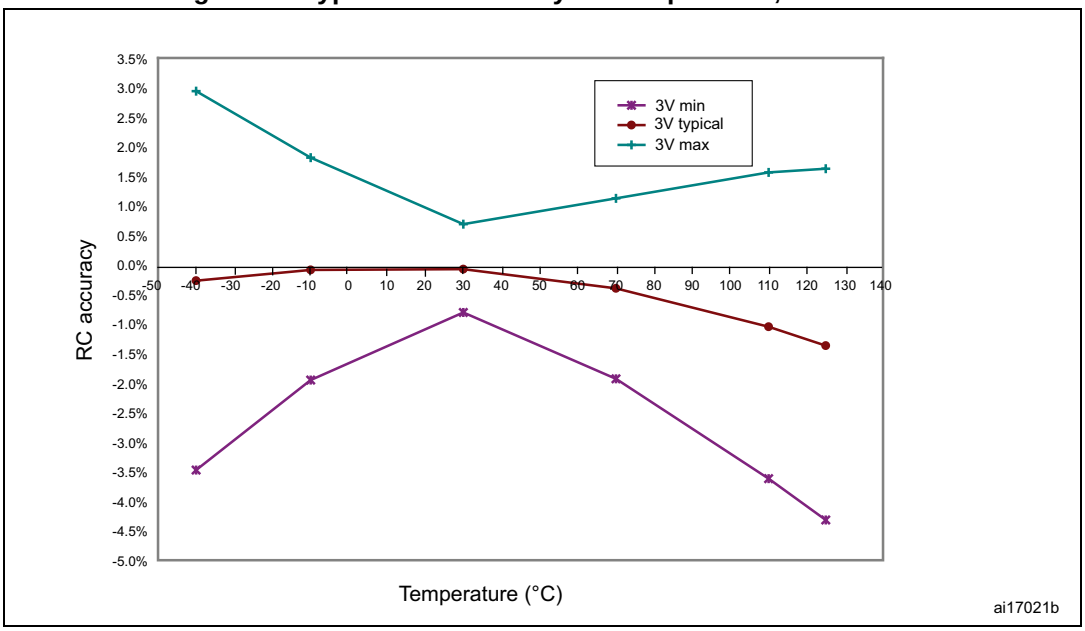


**Figure 15. Typical HSI accuracy vs. temperature, VDD = 3 V**




## High speed ProxSense RC oscillator

**Table 25. HSI_PXS oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI\_PXS}$ | Frequency | $V_{DD}$ = 3.0 V | - | 16 | - | MHz |

1. $V_{DD}$ = 3V, $T_A$ = –40 to 85 °C, unless otherwise specified.

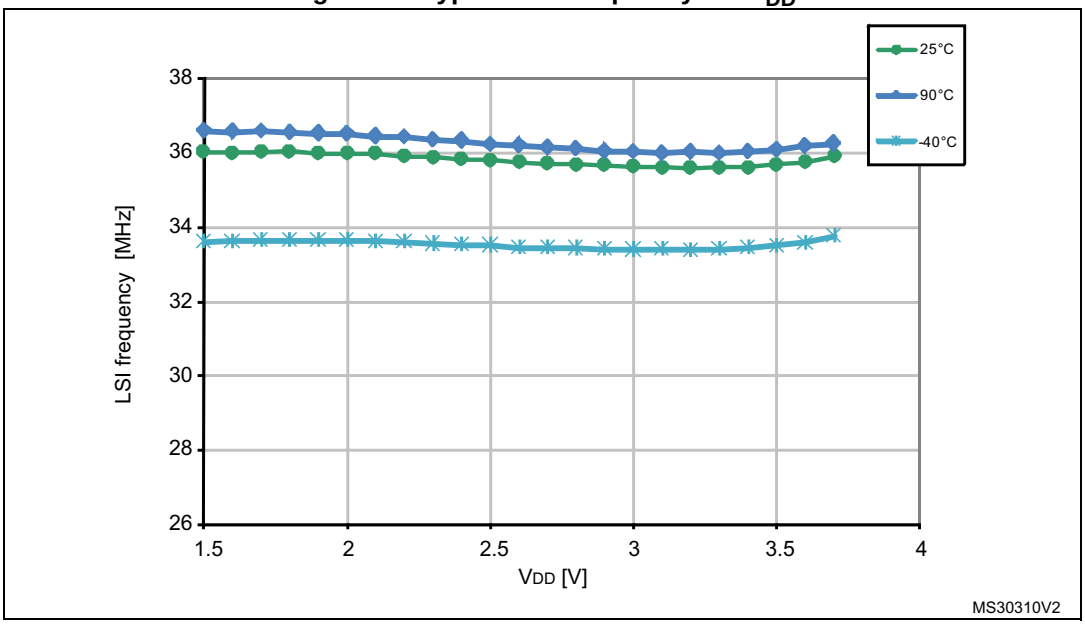
## Low speed internal RC oscillator (LSI)

**Table 26. LSI oscillator characteristics (1)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | Frequency | | 26 | 38 | 56 | kHz |
| $f_{drift(LSI)}$ | LSI oscillator frequency drift(2) | 0 °C ≤ $T_A$ ≤ 85°C | –12 | - | 11 | % |

1. $V_{DD}$ = 1.65 V to 3.6 V, $T_A$ = –40 to 85°C unless otherwise specified.
2. For each individual part, this value is the frequency drift from the initial measured frequency.

Figure 16. Typical LSI frequency vs. $V_{DD}$




## 9.3.7 Memory characteristics

$T_A$ = –40 to 85°C unless otherwise specified.

### RAM characteristics

Table 27. RAM and hardware registers

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{RM}$ | Data retention mode (1) | Halt mode (or Reset) | 1.4 | - | - | V |

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

### Flash memory characteristics

Table 28. Flash program memory

| Symbol | Parameter | Conditions | Min. | Typ. | Max.(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage (all modes, read/write/erase) | $f_{MASTER}$ = 16 MHz | 1.65 | - | 3.6 | V |
| $t_{prog}$ | Programming time for 1 or 64 byte (block) erase/write cycles (on programmed byte) | | - | 6 | - | ms |
| | Programming time for 1 to 64 byte (block) write cycles (on erased byte) | | - | 3 | - | ms |
| $I_{prog}$ | Programming/ erasing consumption | $T_A$=+25 °C, $V_{DD}$ = 3.0 V | - | 0.7 | - | mA |
| | | $T_A$=+25 °C, $V_{DD}$ = 1.8 V | - | | - | |

1. Data based on characterization results, not tested in production.

**Table 29. Program memory endurance and retention**

| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Endurance | $T_A$ = –40 to 85°C | 10(1) | - | - | kcycles |
| Data retention | 10 kcycles at $T_A$ = 85°c | 30(1) | - | - | Years |

1. Data based on characterization results, not tested in production.

**Table 30. Data memory endurance and retention**

| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Endurance | $T_A$ = –40 to 85°C | 300(1)(2) | - | - | kcycles |
| Data retention | 300 kcycles at $T_A$ = 85°c | 30(1) | - | - | Years |

1. Data based on characterization results, not tested in production.
2. Data based on characterization performed on the whole data memory (2 Kbyte).

## 9.3.8 I/O port pin characteristics

### General characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 31. I/O static characteristics (1)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage(2) | Standard I/Os | $V_{SS}$–0.3 | - | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | Input high level voltage(2) | Standard I/Os | 0.70 x $V_{DD}$ | - | $V_{DD}$+0.3 | |
| $V_{hys}$ | Schmitt trigger voltage hysteresis(3) | Standard I/Os | - | 200 | - | mV |
| $I_{lkg}$ | Input leakage current(4) | $V_{SS} \le V_{IN} \le V_{DD}$ | - | - | 50 | nA |
| | | $V_{SS} \le V_{IN} \le V_{reg}$ Rx, Tx I/Os | - | - | 50 | |
| $R_{PU}$ | Weak pull-up equivalent resistor(5) | $V_{IN} = V_{SS}$ | 30 | 45 | 60 | kΩ |
| $C_{IO}$(6) | I/O pin capacitance | - | - | 5 | - | pF |

1. $V_{DD}$ = 3.0 V, $T_A$ = –40 to 85 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The maximum value may be exceeded if negative current is injected on adjacent pins.
5. $R_{PU}$ pull-up equivalent resistor based on a resistive transistor (corresponding $I_{PU}$ current characteristics.
6. Data guaranteed by Design, not tested in production.

**Figure 17. Typical pull-up resistance $R_{PU}$ vs. $V_{DD}$ with $V_{IN}=V_{SS}$**

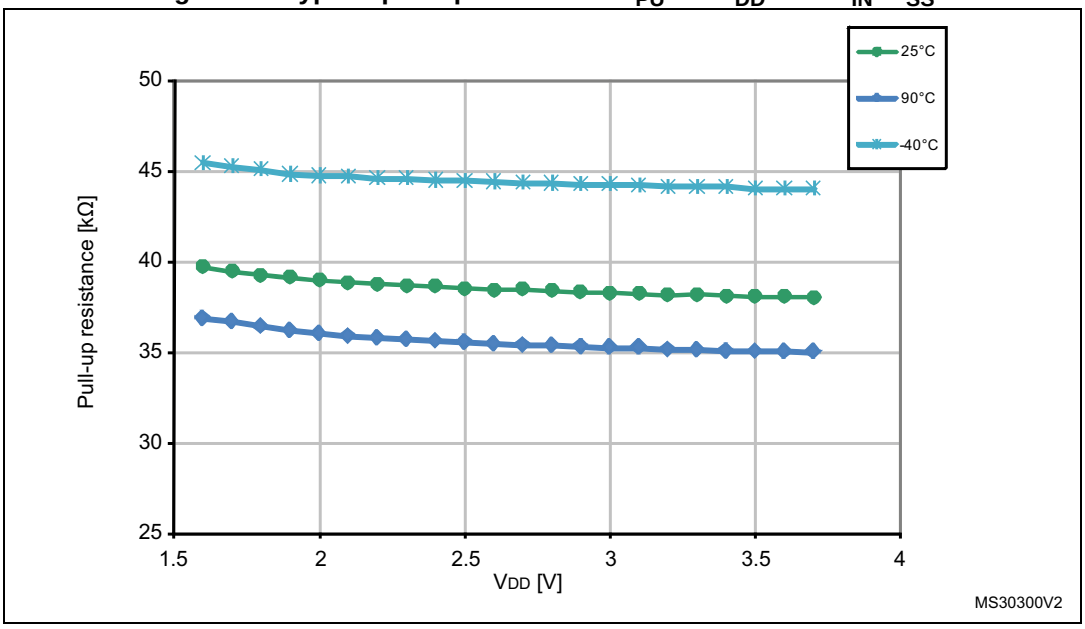
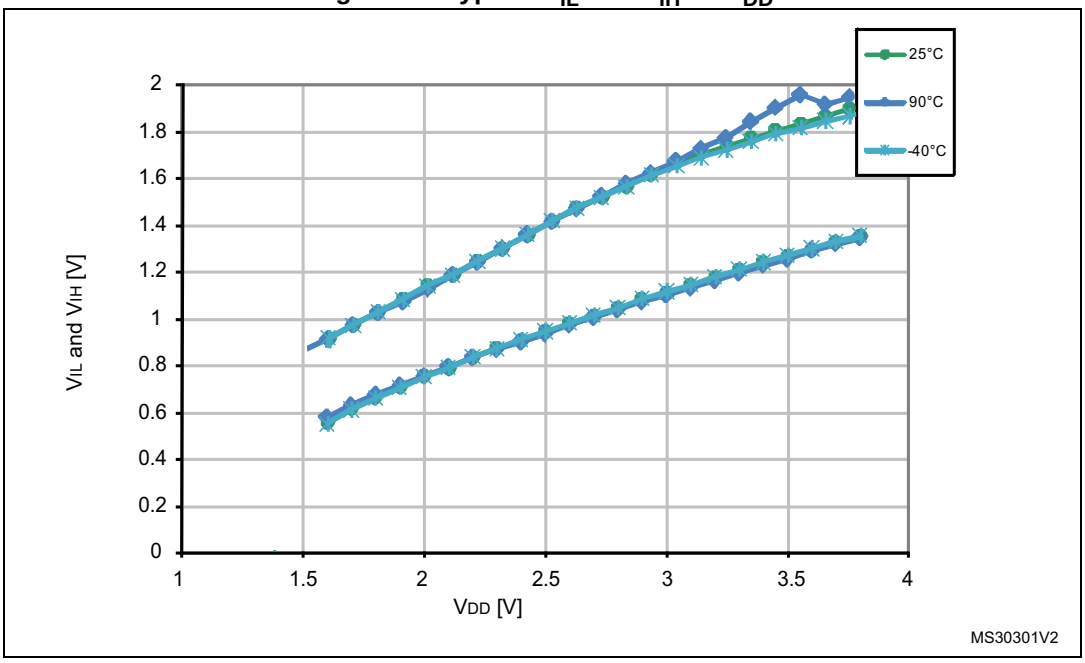


**Figure 18. Typical $V_{IL}$ and $V_{IH}$ vs $V_{DD}$**



### Output driving current

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 32. Output driving current (high sink ports)**

| I/O type | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Standard | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +2 mA, $V_{DD}$ = 1.8 V | - | 0.45 | V |
| | | | $I_{IO}$ = +2 mA, $V_{DD}$ = 3.0 V | - | 0.45 | |
| | | | $I_{IO}$ = +10 mA, $V_{DD}$ = 3.0 V | - | 0.7 | |
| | $V_{OH}$ (2) | Output high level voltage for an I/O pin | $I_{IO}$ = –1 mA, $V_{DD}$ = 1.8 V | $V_{DD}$-0.45 | - | |
| | | | $I_{IO}$ = –1 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-0.45 | - | |
| | | | $I_{IO}$ = –10 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-0.7 | - | |
| ProxSense I/O | $V_{OH}$ | Output high level voltage for PXS_TX ProxSense I/O | $I_{PXS\_TX}$ = 0.2 mA | $V_{REG}$ | - | |
| | $V_{OH}$ | Output high level voltage for PXS_RX ProxSense I/O | $I_{PXS\_RX}$ = 0.1 mA | $V_{REG}$ | - | |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. The $I_{IO}$ current sourced must always respect the absolute maximum rating and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.

**Figure 19. Typ. $V_{OL}$ at $V_{DD}$ = 1.8 V (standard ports)**

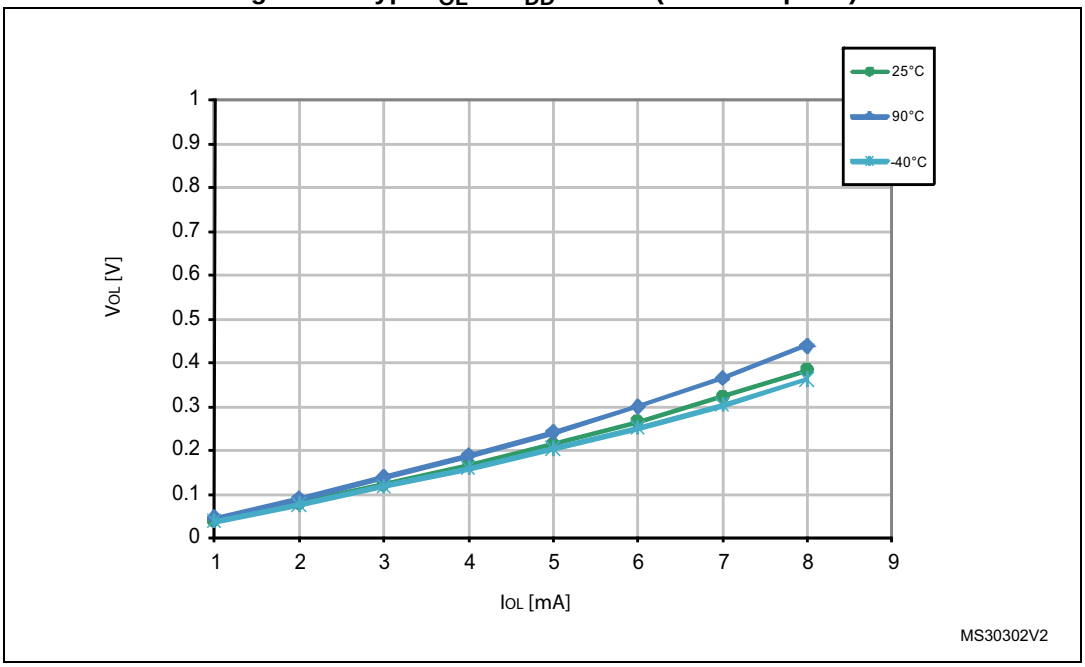


Figure 20. Typ. $V_{OL}$ at $V_{DD}$ = 3.0 V (standard ports)

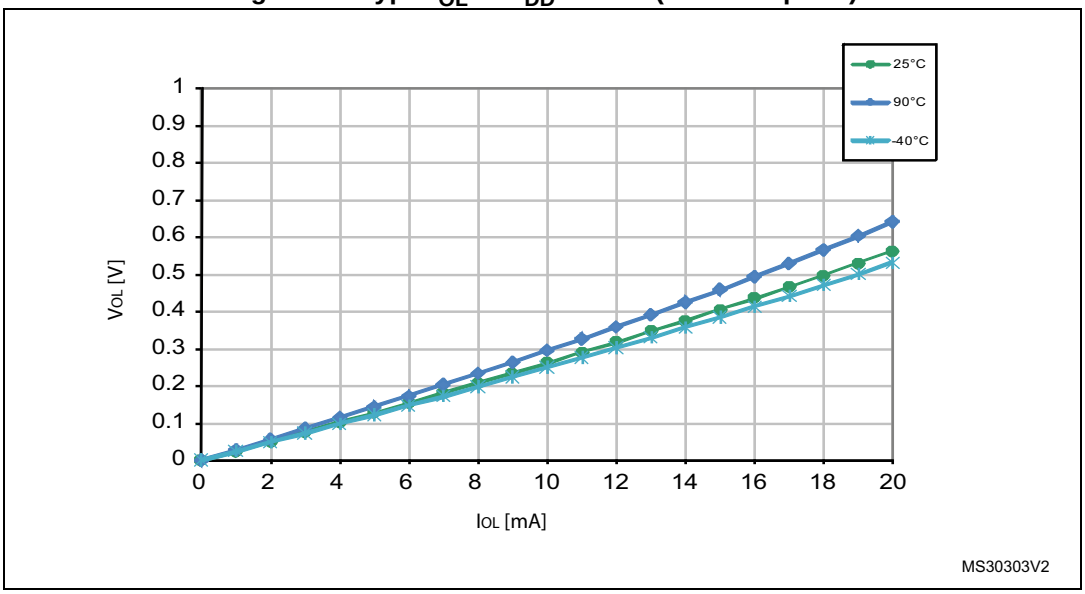



Figure 21. Typ. $V_{DD}$ - $V_{OH}$ at $V_{DD}$ = 1.8 V (standard ports)

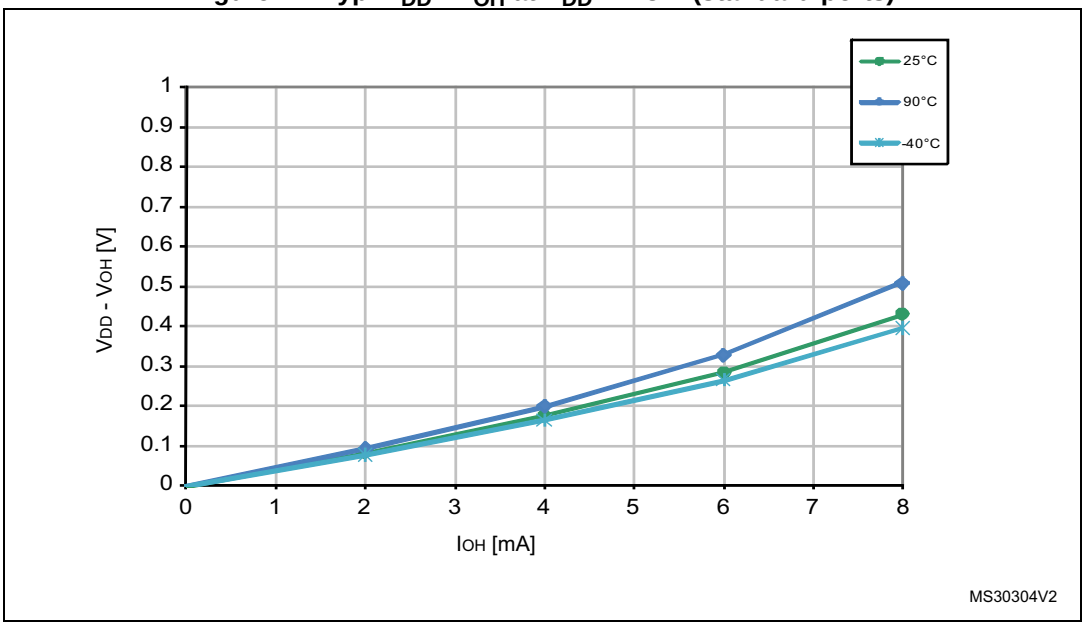


**Figure 22. Typ. $V_{DD}$ - $V_{OH}$ at $V_{DD}$ = 3.0 V (standard ports)**

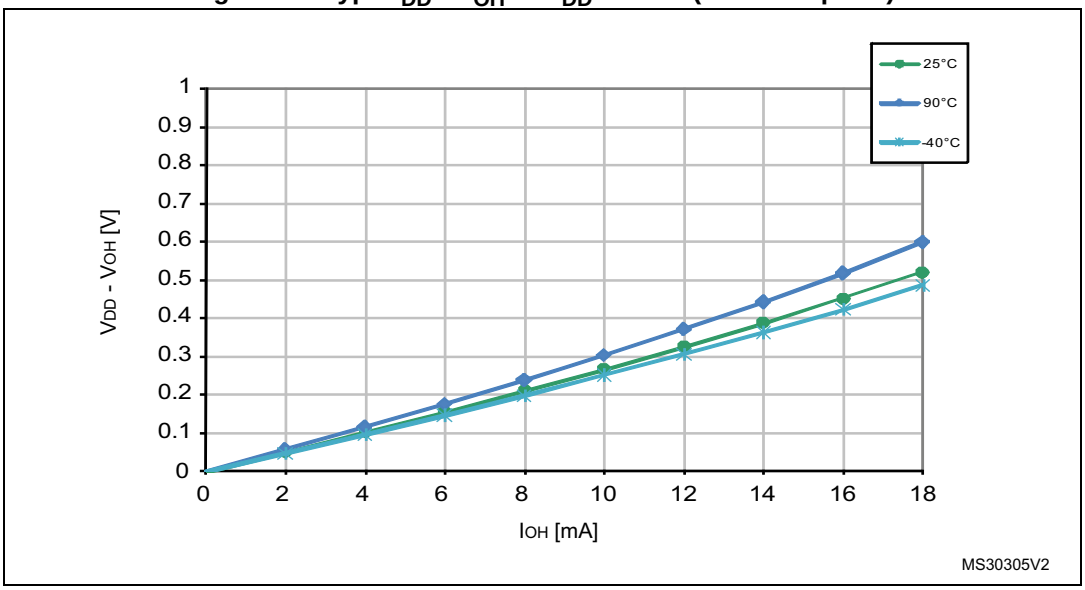



**Figure 23. Typ. $V_{DD}$ - $V_{OH}$ at $V_{DD}$ = 1.8 V (ProxSense TX ports)**

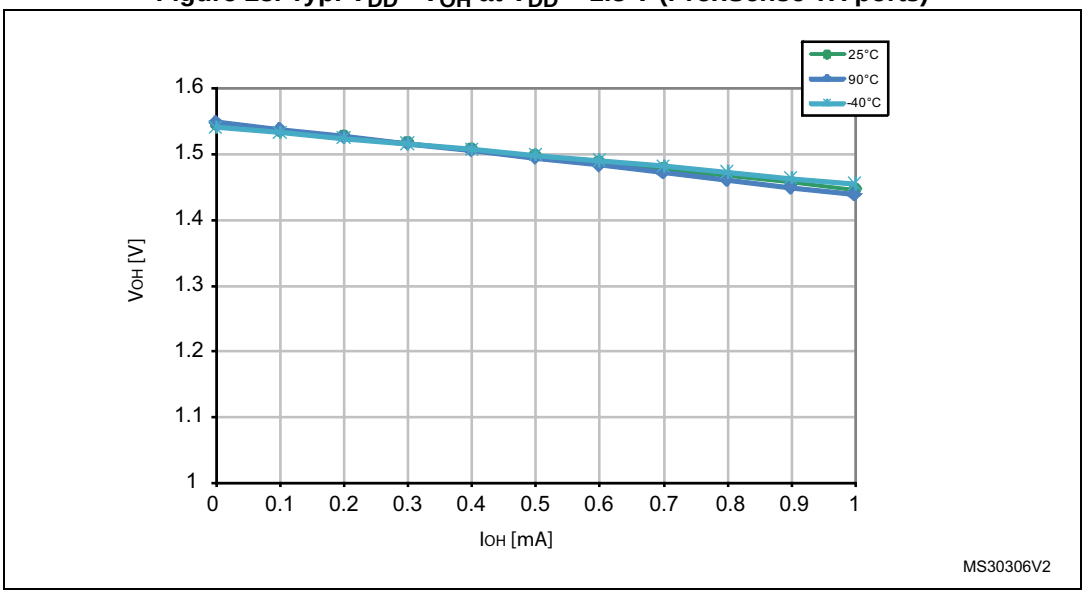
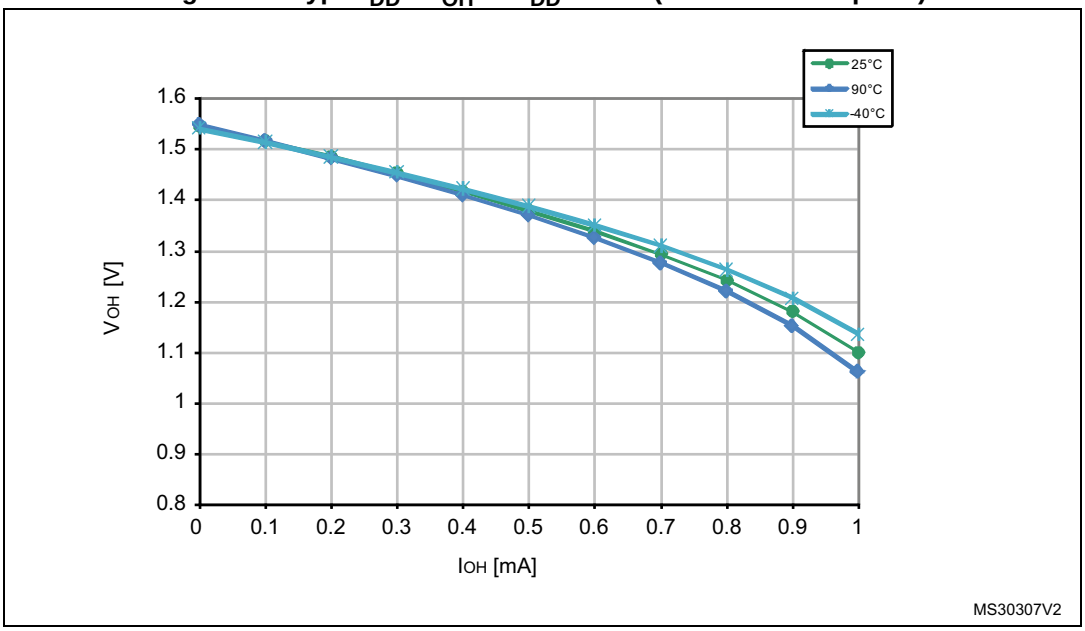


**Figure 24. Typ. $V_{DD}$ - $V_{OH}$ at $V_{DD}$ = 1.8V (ProxSense RX ports)**



### NRST pin

The NRST pin input driver is CMOS. A permanent pull-up is present which is the same as $R_{PU}$ (see *Table 31 on page 56*).

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 33. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low level voltage(1) | - | $V_{SS}$ | - | 0.8 | V |
| $V_{IH(NRST)}$ | NRST input high level voltage(1) | - | 1.4 | - | $V_{DD}$ | |
| $V_{OL(NRST)}$ | NRST output low level voltage | $I_{OL}$ = 2 mA | - | - | $V_{DD}$-0.8 | |
| $R_{PU(NRST)}$ | NRST pull-up equivalent resistor(2) | - | 30 | 45 | 60 | kΩ |
| $V_{F(NRST)}$ | NRST input filtered pulse(3) | - | - | - | 50 | ns |
| $t_{OP(NRST)}$ | NRST output pulse width | - | 20 | - | - | |
| $V_{NF(NRST)}$ | NRST input not filtered pulse(3) | - | 300 | - | - | |

1. Data based on characterization results, not tested in production.
2. The $R_{PU}$ pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

The reset network shown in *Figure 26* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the $V_{IL}$ max. level specified in *Table 33*. Otherwise the reset is not taken into account internally.

**Figure 25. Typical NRST pull-up resistance $R_{PU}$ vs. $V_{DD}$**

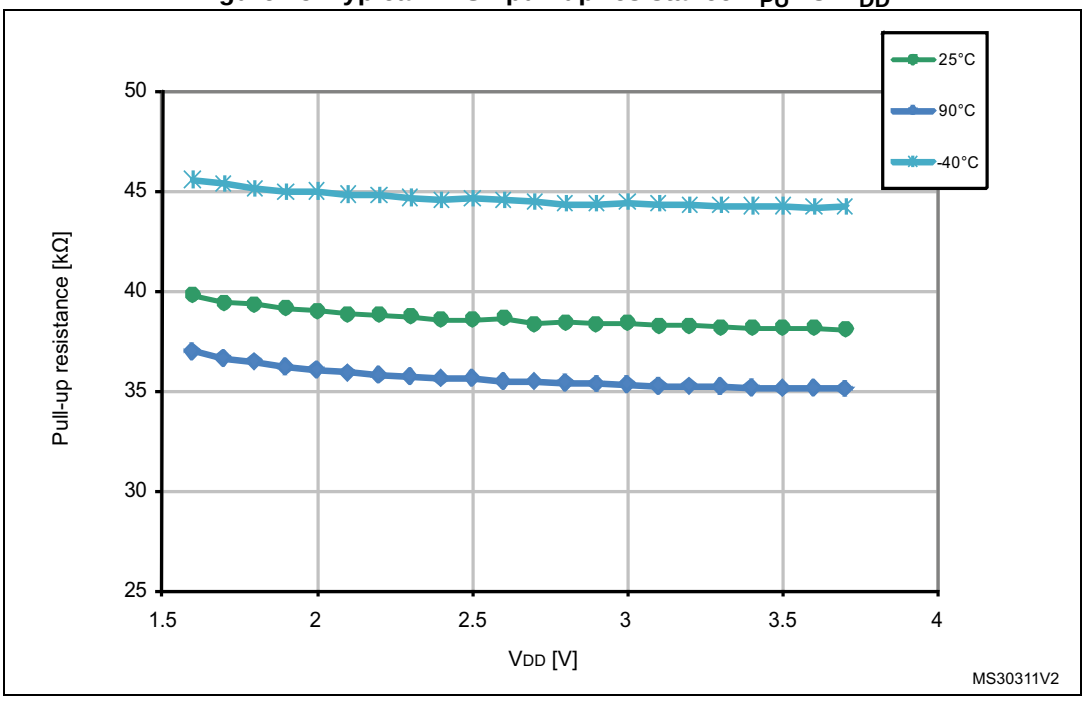
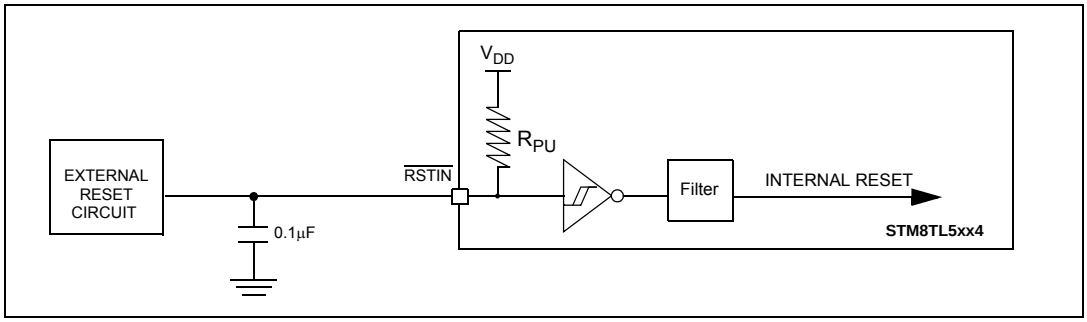


**Figure 26. Recommended NRST pin configuration**




The reset network shown in *Figure 26* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the $V_{IL}$ max. level specified in *Table 33*. Otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

## 9.3.9 Communication interfaces

### Serial peripheral interface (SPI)

The parameters given in *Table 34* are derived from tests performed under ambient temperature, $f_{MASTER}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Section 9.3.1 on page 45*, unless otherwise specified. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 34. SPI characteristics**

| Symbol | Parameter | Conditions(1) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 8 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 30 | ns |
| $t_{su(NSS)}$(2) | NSS setup time | Slave mode | 4 x $t_{MASTER}$ | - | |
| $t_{h(NSS)}$(2) | NSS hold time | Slave mode | 80 | - | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode,<br>$f_{MASTER}$ = 8 MHz, $f_{SCK}$= 4 MHz | 105 | 145 | |
| $t_{su(MI)}$(2)<br>$t_{su(SI)}$(2) | Data input setup time | Master mode | 30 | - | |
| | | Slave mode | 3 | - | |
| $t_{h(MI)}$(2)<br>$t_{h(SI)}$(2) | Data input hold time | Master mode | 15 | - | |
| | | Slave mode | 0 | - | |
| $t_{a(SO)}$(2)(3) | Data output access time | Slave mode | - | 3x $t_{MASTER}$ | |
| $t_{dis(SO)}$(2)(4) | Data output disable time | Slave mode | 30 | - | |
| $t_{v(SO)}$(2) | Data output valid time | Slave mode (after enable edge) | - | 60 | |
| $t_{v(MO)}$(2) | Data output valid time | Master mode<br>(after enable edge) | - | 20 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$(2) | | Master mode<br>(after enable edge) | 1 | - | |

1. Parameters are given by selecting 10–MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi–Z.

**Figure 27. SPI timing diagram - slave mode and CPHA = 0**

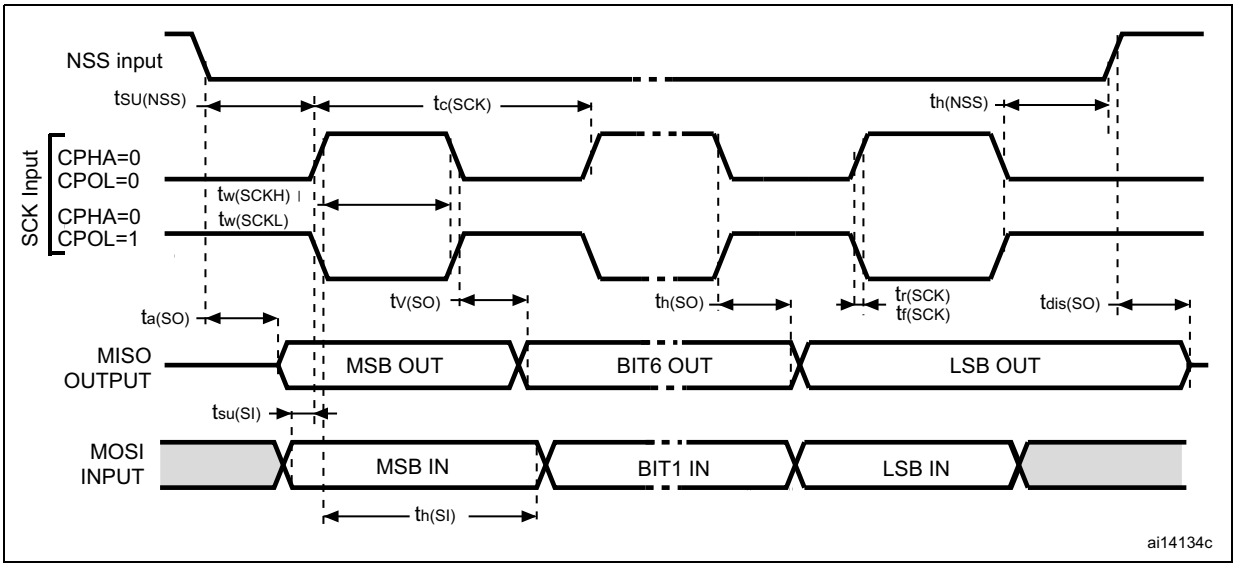
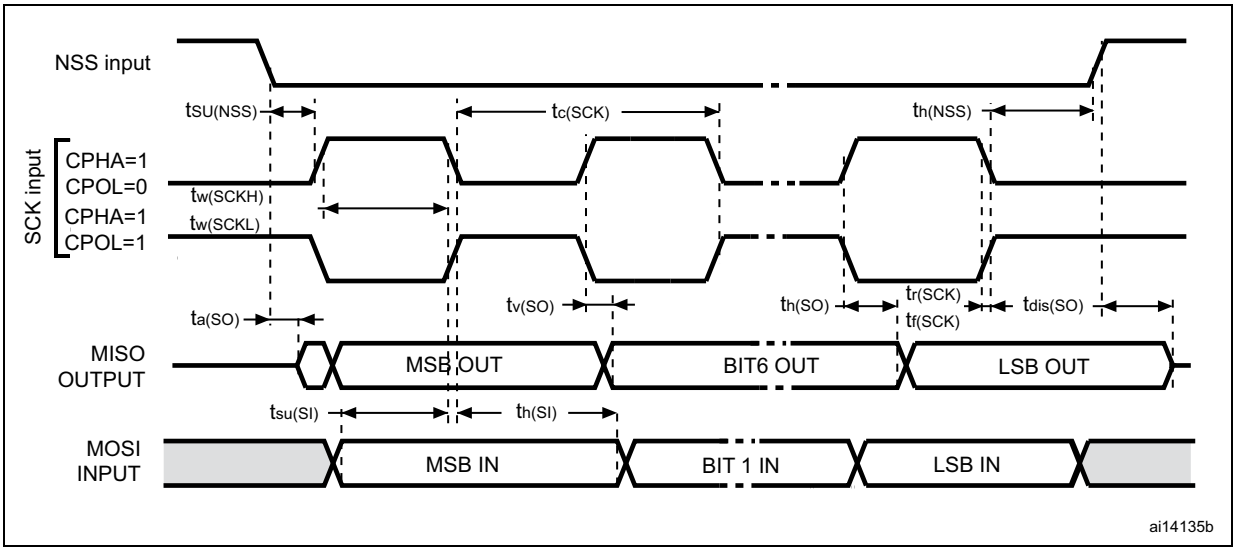
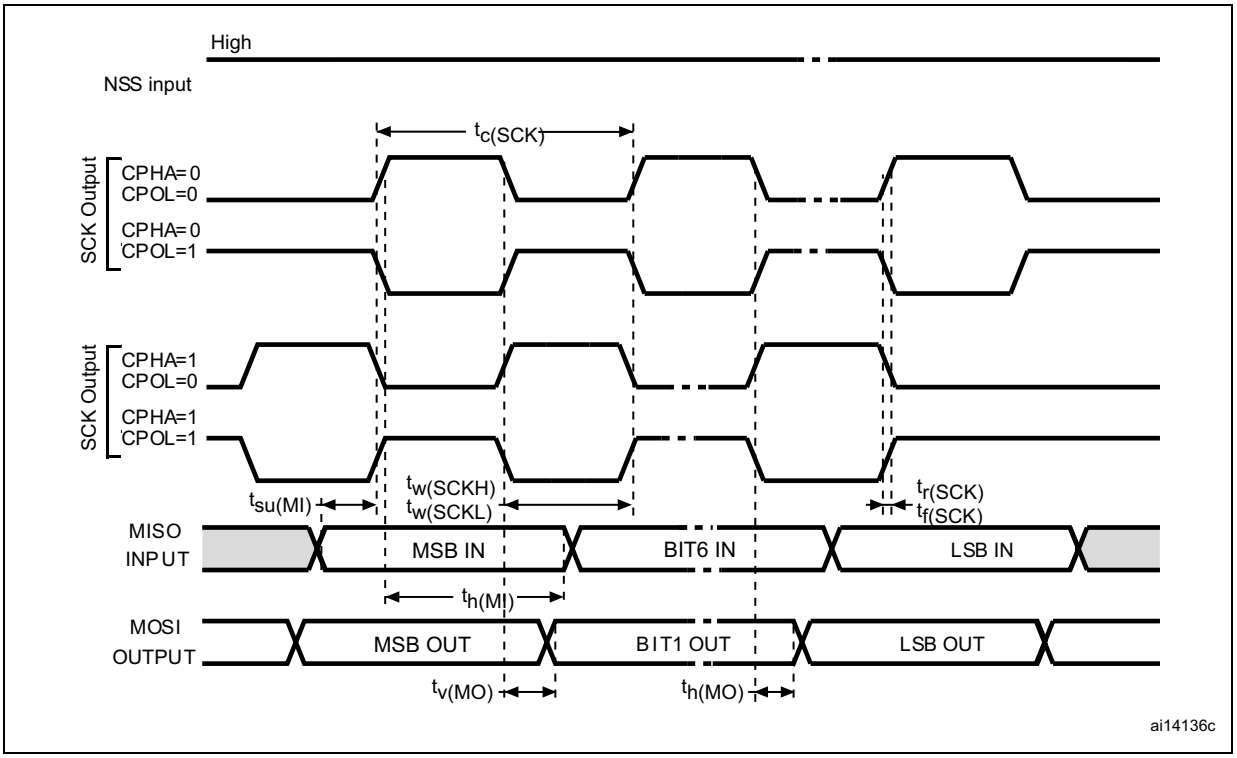



**Figure 28. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Figure 29. SPI timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

### Inter IC control interface (I2C)

Subject to general operating conditions for $V_{DD}$, $f_{MASTER}$, and $T_A$ unless otherwise specified.

The STM8TL5xx4 I2C interface meets the requirements of the Standard I2C communication protocol described in the following table with the restrictions mentioned below.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

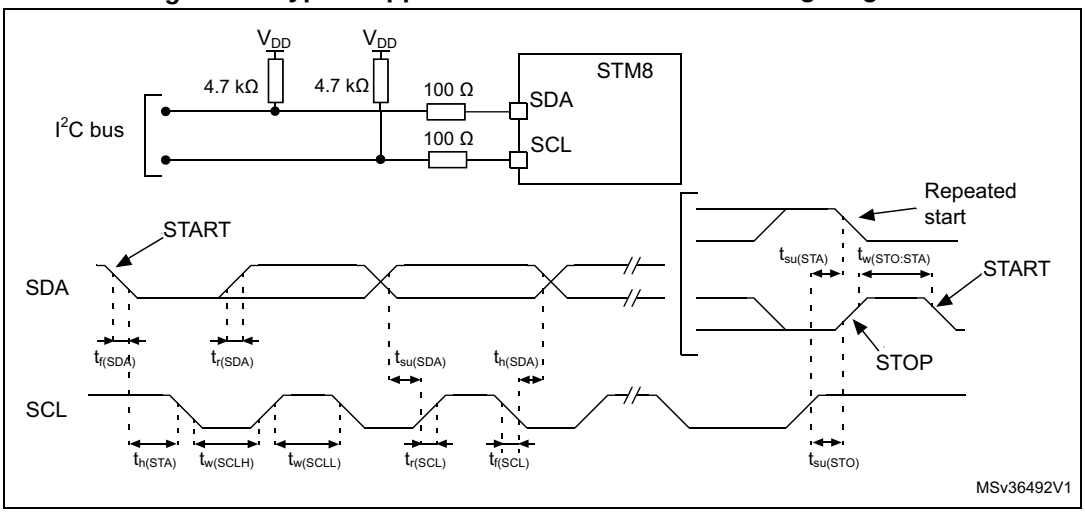
**Table 35. $I^2C$ characteristics**

| Symbol | Parameter | Standard mode $I^2C$ | | Fast mode $I^2C$(1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min(2) | Max (2) | Min (2) | Max (2) | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 (3) | - | 0 (4) | 900 (3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | START condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | STOP condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | STOP to START condition time (bus free) | 4.7 | - | 1.3 | - | µs |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. $f_{SCK}$ must be at least 8 MHz to achieve max fast $I^2C$ speed (400 kHz).
2. Data based on standard $I^2C$ protocol requirement, not tested in production.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL).

*Note: For speeds around 200 kHz, achieved speed can have ±5% tolerance.*
*For other speed ranges, achieved speed can have ±2% tolerance.*
*The above variations depend on the accuracy of the external components used.*

**Figure 30. Typical application with I²C bus and timing diagram [1)]**




1. Measurement points are done at CMOS levels: 0.3 x $V_{DD}$ and 0.7 x $V_{DD}$.

## 9.3.10 EMC characteristics

Susceptibility tests are performed on a sample 36 basis during product characterization.

### Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Table 36. EMS data**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | UFQFPN48, $V_{DD}$ = 3.3 V | 3B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | UFQFPN48, $V_{DD}$ = 3.3 V, $f_{HSI}$ | 3B |

## Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

**Table 37. EMI data (1)**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. 16 MHz | Unit |
|---|---|---|---|---|---|
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = +25 °C | 0.1 MHz to 30 MHz | -5 | dBµV |
| | | | 30 MHz to 130 MHz | -5 | |
| | | | 130 MHz to 1 GHz | 0 | |
| | | | SAE EMI Level | 1 | - |

1. Not tested in production.

## Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to application note AN1181.

## Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/A115A standard.

**Table 38. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Maximum value (1) | Unit |
|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C | 2000(2) | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | | 1000 | |

1. Data based on characterization results, not tested in production.
2. Device sustained up to 3000 V during ESD trials.

### Static latch-up

- **LU**: 3 complementary static tests are required on 6 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to application note AN1181.

**Table 39. Electrical sensitivities**

| Symbol | Parameter | Class |
|---|---|---|
| LU | Static latch-up class | II |

## 9.4 Thermal characteristics

The maximum chip junction temperature ($T_{Jmax}$) must never exceed the values given in *Table 16: General operating conditions on page 45*.

The maximum chip-junction temperature, $T_{Jmax}$, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- $T_{Amax}$ is the maximum ambient temperature in °C
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance in °C/W
- $P_{Dmax}$ is the sum of $P_{INTmax}$ and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- $P_{INTmax}$ is the product of $I_{DD}$ and $V_{DD}$, expressed in watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual $V_{OL}/I_{OL}$ and $V_{OH}/I_{OH}$ of the I/Os at low and high level in the application.

**Table 40. Thermal characteristics(1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient UFQFPN 48 - 7 x 7 mm | 32 | °C/W |
| | Thermal resistance junction-ambient UFQFPN 28 - 4 x 4 mm | 80 | |
| | Thermal resistance junction-ambient TSSOP20 | 110 | |

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

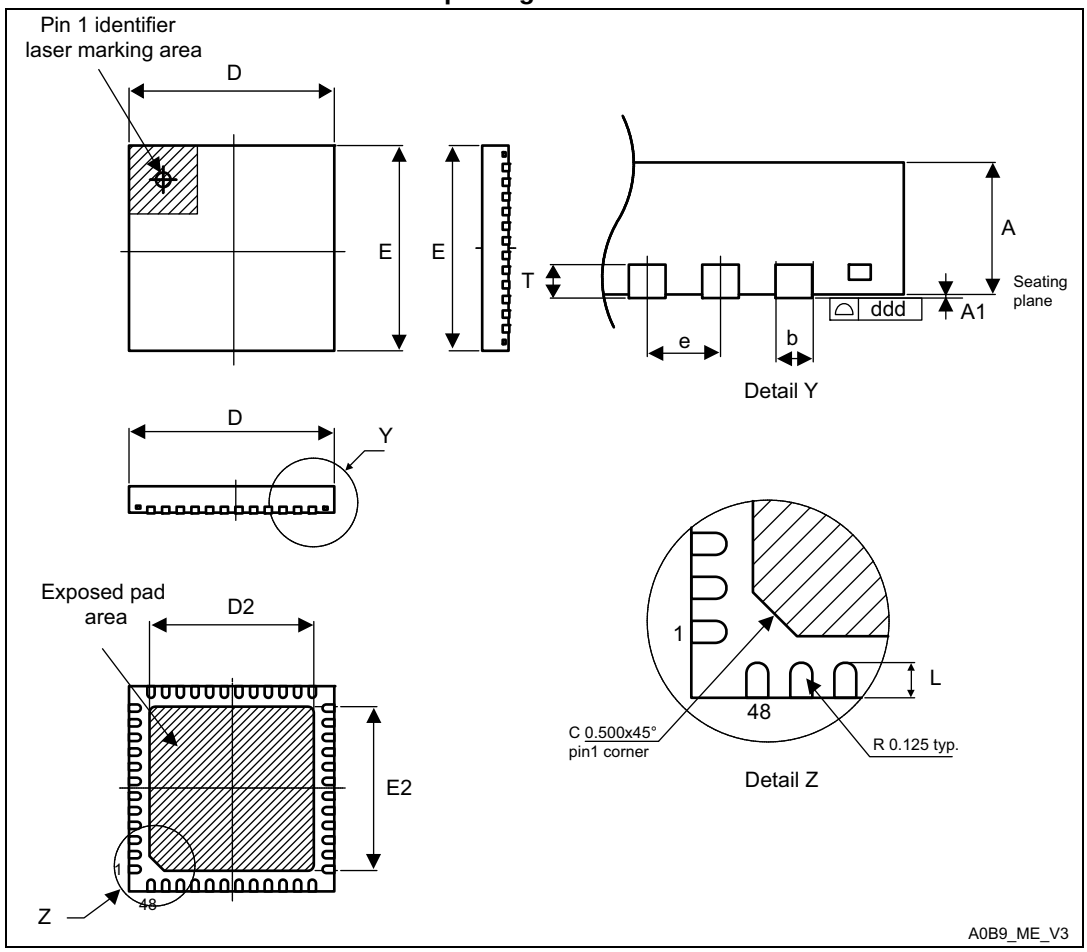
# 10 Package information

## 10.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at:*www.st.com*. ECOPACK® is an ST trademark.

## 10.2 UFQFPN48 package information

**Figure 31. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline**



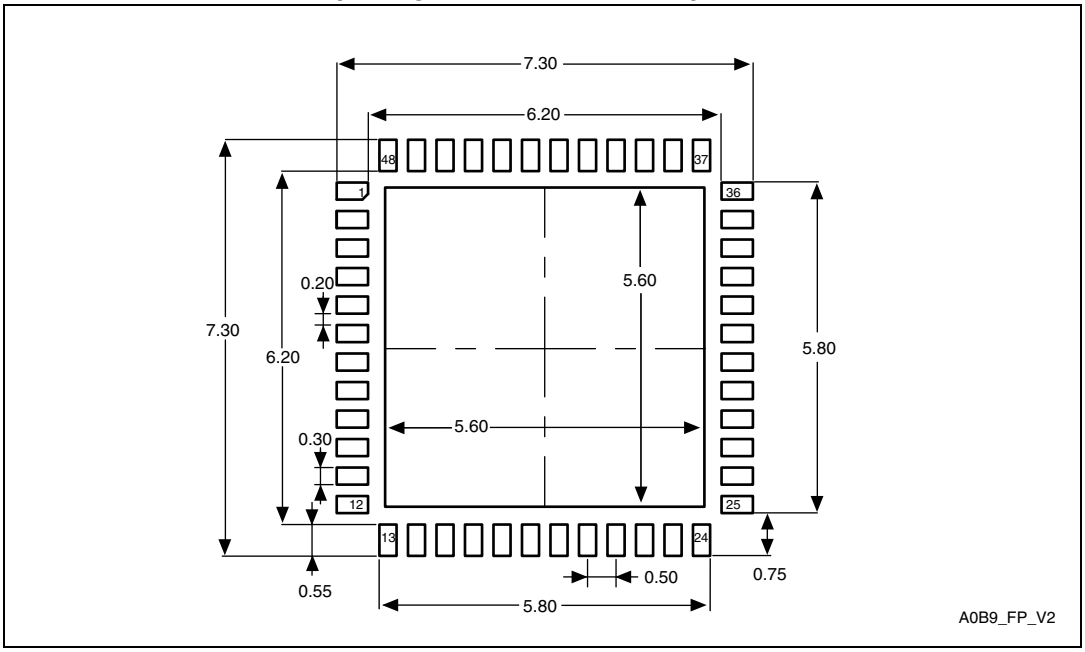

1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

**Table 41. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| D | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| E | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| D2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| E2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| T | - | 0.152 | - | - | 0.0060 | - |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 32. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint**

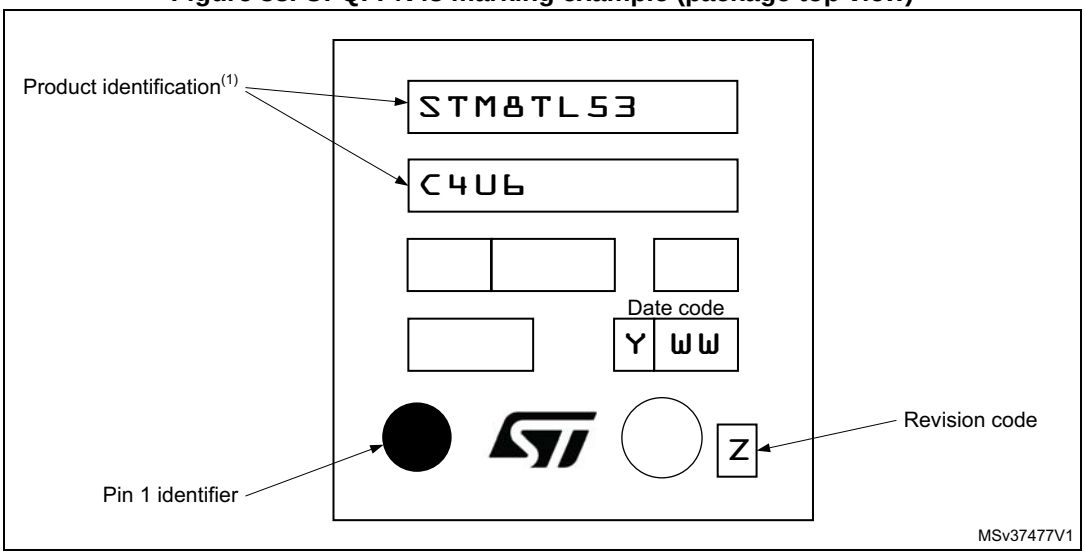



1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

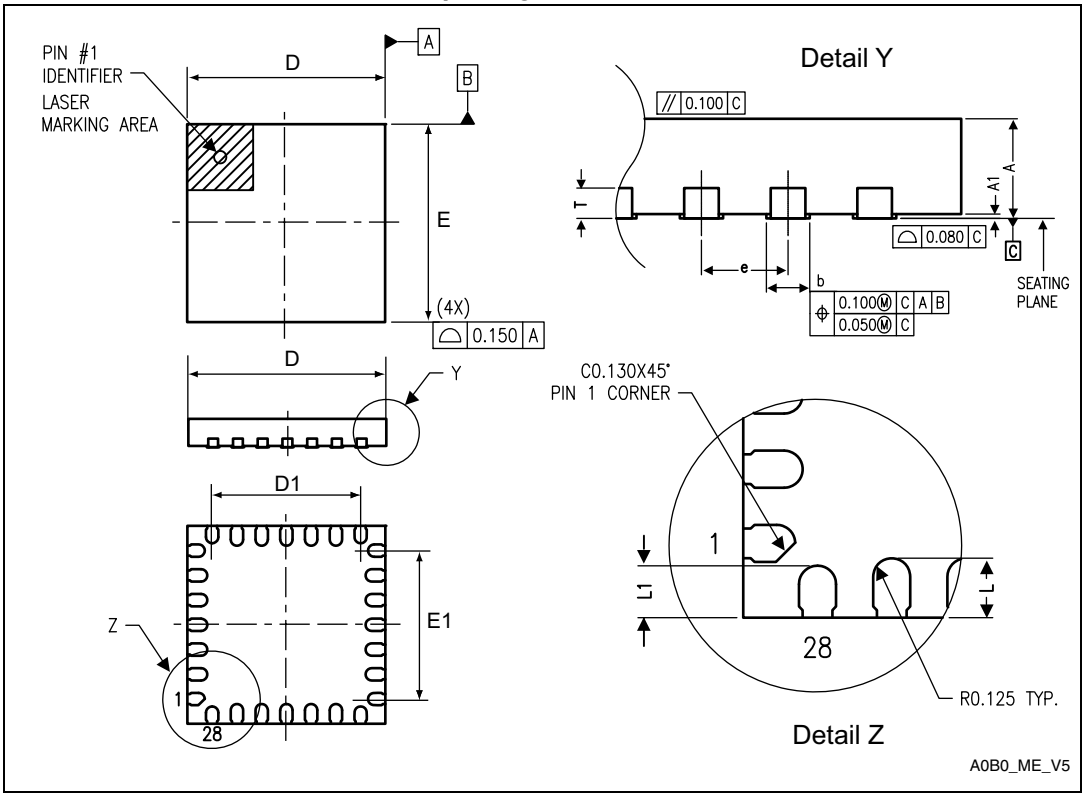
**Figure 33. UFQFPN48 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 10.3 UFQFPN28 package information

**Figure 34. UFQFPN28 - 28-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline**



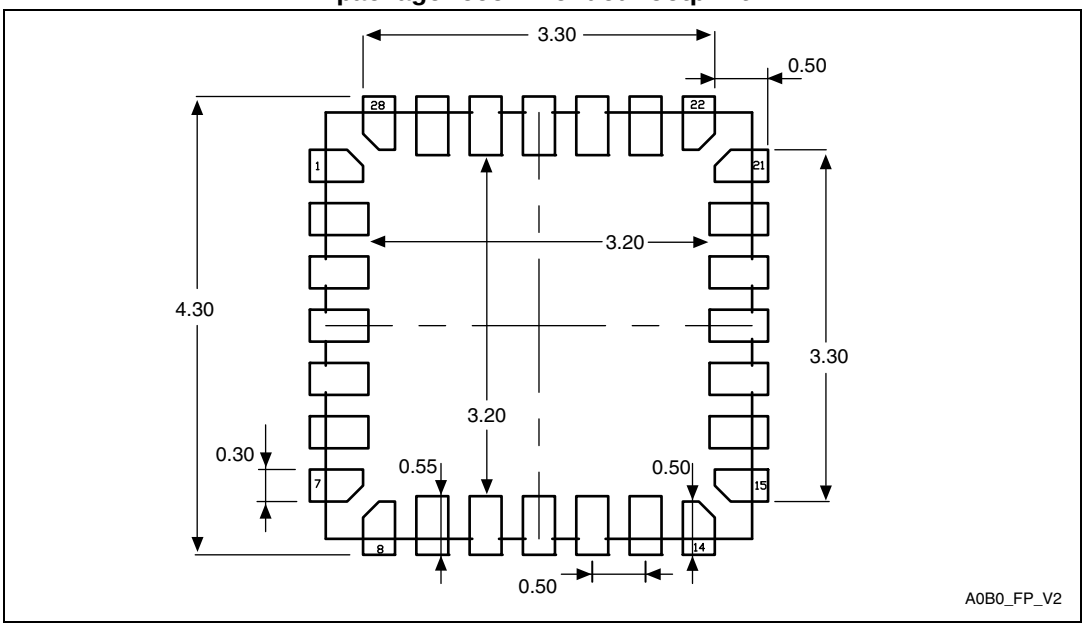

1. Drawing is not to scale.

**Table 42. UFQFPN28 - 28-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data(1)**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | - | 0.000 | 0.050 | - | 0.0000 | 0.0020 |
| D | 3.900 | 4.000 | 4.100 | 0.1535 | 0.1575 | 0.1614 |
| D1 | 2.900 | 3.000 | 3.100 | 0.1142 | 0.1181 | 0.1220 |
| E | 3.900 | 4.000 | 4.100 | 0.1535 | 0.1575 | 0.1614 |
| E1 | 2.900 | 3.000 | 3.100 | 0.1142 | 0.1181 | 0.1220 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| L1 | 0.250 | 0.350 | 0.450 | 0.0098 | 0.0138 | 0.0177 |
| T | - | 0.152 | - | - | 0.0060 | - |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 35. UFQFPN28 - 28-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint**

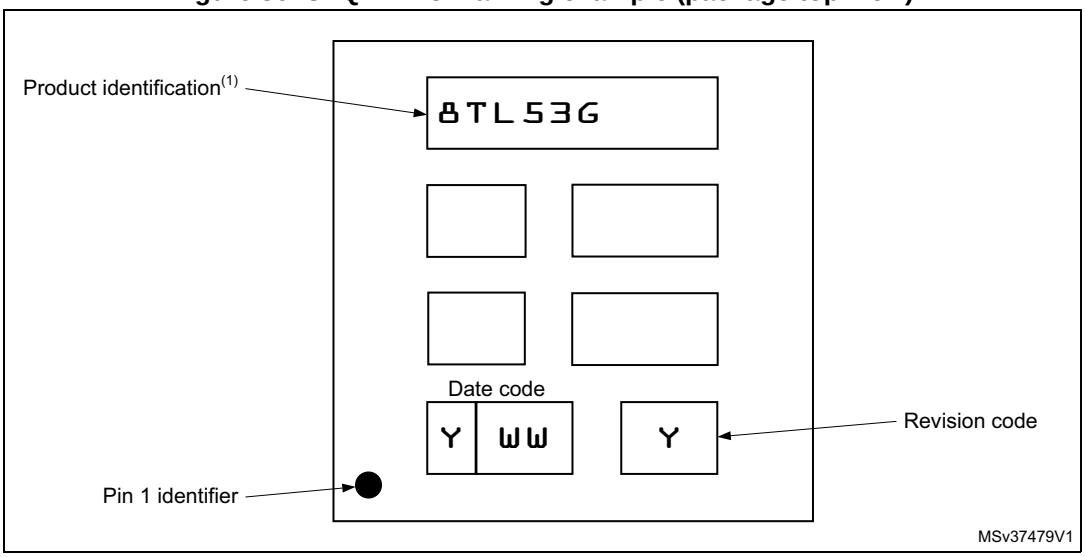



1. Dimensions are expressed in millimeters.

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 36. UFQFPN28 marking example (package top view)**

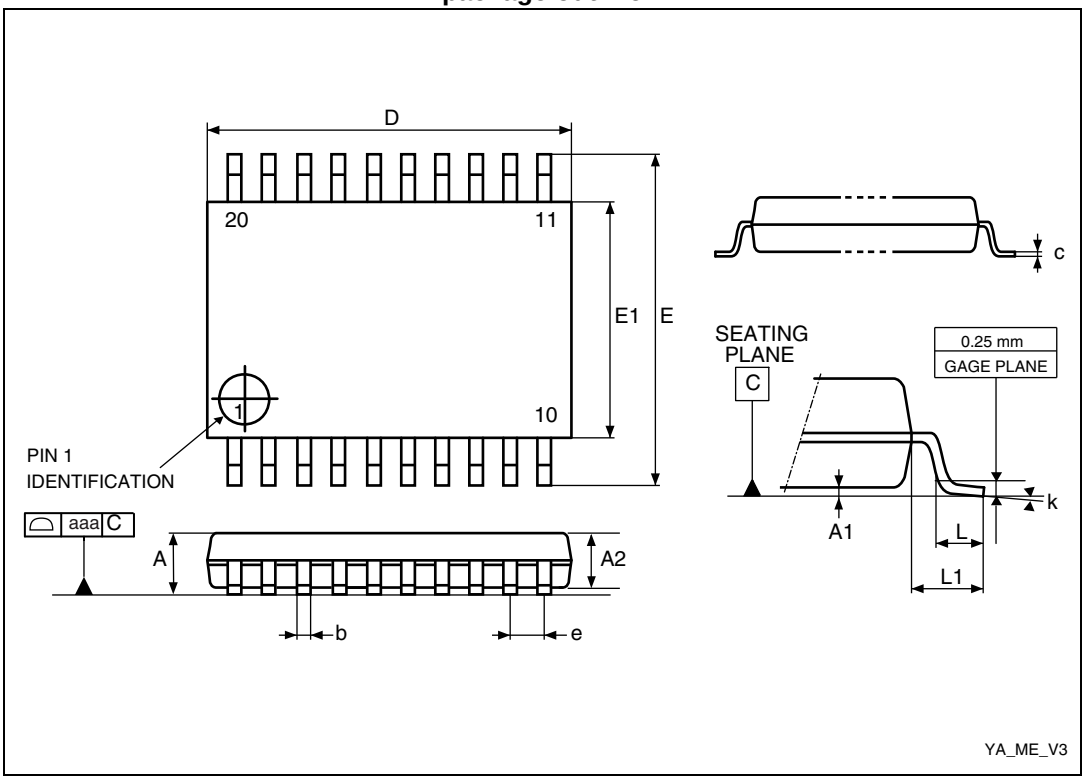



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering

samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 10.4 TSSOP20 package information

**Figure 37.TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package outline**




1. Drawing is not to scale.

**Table 43. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data**

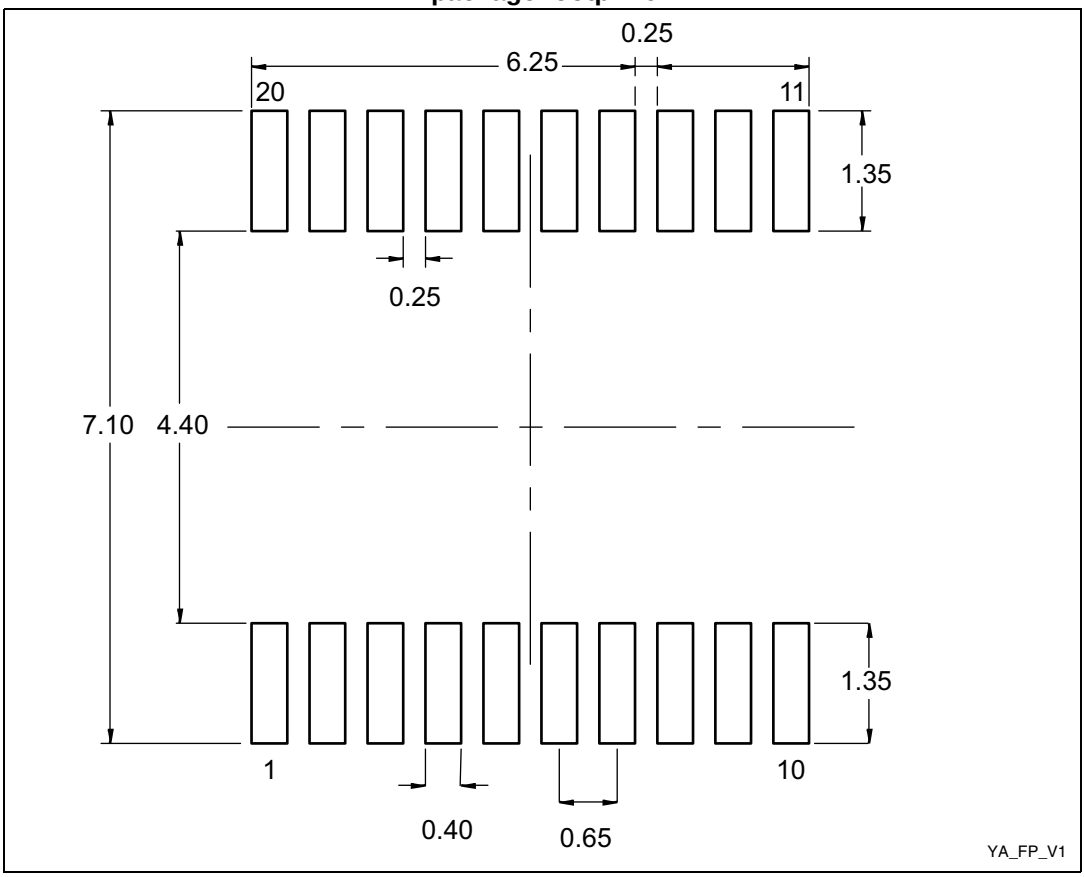
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 0.800 | 1.000 | 1.050 | 0.0315 | 0.0394 | 0.0413 |
| b | 0.190 | - | 0.300 | 0.0075 | - | 0.0118 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D[2] | 6.400 | 6.500 | 6.600 | 0.2520 | 0.2559 | 0.2598 |
| E | 6.200 | 6.400 | 6.600 | 0.2441 | 0.2520 | 0.2598 |
| E1[3] | 4.300 | 4.400 | 4.500 | 0.1693 | 0.1732 | 0.1772 |
| e | - | 0.650 | - | - | 0.0256 | - |

**Table 43. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | - | 8° | 0° | - | 8° |
| aaa | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

**Figure 38. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint**

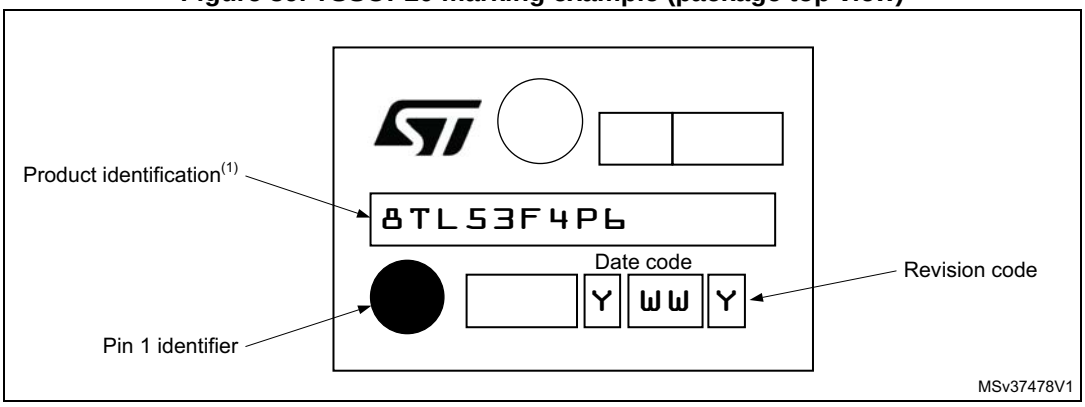



1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

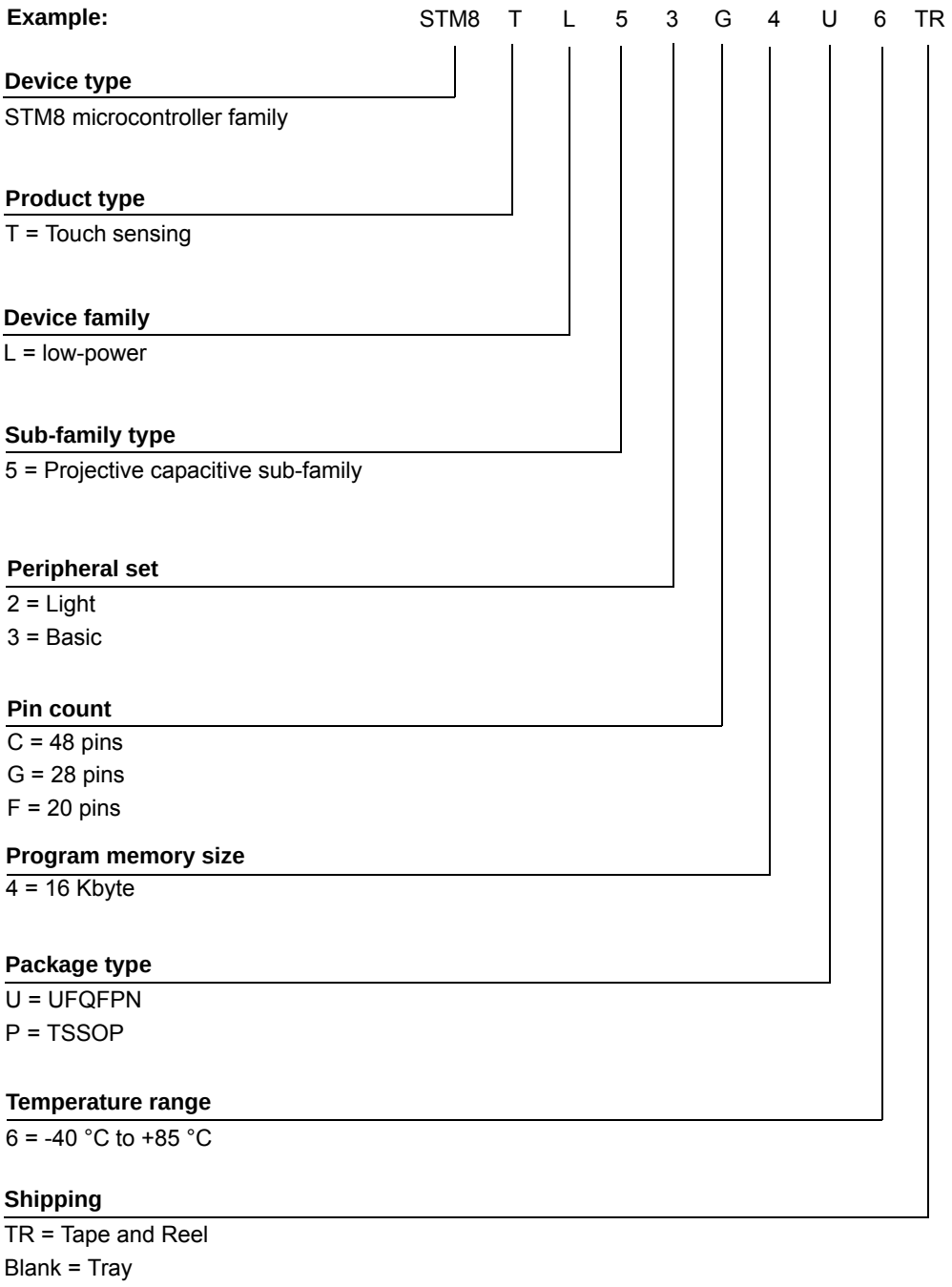
**Figure 39. TSSOP20 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

# 11 Part numbering

**Table 44. Ordering information scheme**




1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

# 12 STM8 development tools

Development tools for the STM8 microcontrollers include the very low-cost debugger and programmer tool ST-Link supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

## 12.1 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

### 12.1.1 STM8 toolset

***STM8 toolset*** with STVD integrated development environment and STVP programming software is available for free download at www.st.com. This package includes:

***ST Visual Develop (STVD)*** – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface

***ST Visual Programmer (STVP)*** – Easy-to-use, unlimited graphical interface allowing read, write and verify of your STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

### 12.1.2 STM-STUDIO

***STM-STUDIO*** helps debug and diagnose STM8 and STM32 applications while they are running by reading and displaying their variables in real-time. STM-STUDIO perfectly complements traditional debugging tools to fine tune applications. It is well suited for debugging applications which cannot be stopped, such as TouchSensing applications. Its easy-to-use, graphical interface features:

- Non-intrusive read on-the-fly variables from RAM while the application is running
- Parse DWARF debugging information in the ELF application executable file
- Possibility to log data into a file, and replay later (exhaustive record display, not real-time)
- 2 types of viewers:
  - Variable viewer: Real-time waveforms, oscilloscope-like graphs
  - TouchPoint viewer: Association of 2 variables, one on the X axis, one on the Y axis

### 12.1.3 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of your application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***IAR embedded workbench*** – The C compiler for STM8 which is included in the toolset is free for up to 8Kbytes of code. For more information, see www.iar.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows you to assemble and link your application source code.

## 12.2 Programming tools

During the development cycle, ST-Link provides in-circuit programming of the STM8 Flash microcontroller on your application board via the SWIM protocol.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

# 13 Revision history

**Table 45. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 14-Oct-2011 | 1 | Initial release |
| 04-Apr-2012 | 2 | Added STM8TL52G4, STM8TL52F4, STM8TL53F4 part numbers<br>Added *Figure 14*, *Figure 16*, *Figure 17*, *Figure 18*, *Figure 19*, *Figure 20*, *Figure 21*, *Figure 22*, *Figure 23*, *Figure 24*, *Figure 25*, *Figure 26*<br>Updated *Figure 31* and *Table 41*<br>Added TSSOP20 package |
| 06-Aug-2013 | 3 | Removed “STICE” references and edited the text in *Section 3.2: Development tools* and *Section 12: STM8 development tools*.<br>In *Table 7: General hardware register map*:<br>– changed the Reset status from “0x00” to “0x01” on “CLK_PCKENR2” row,<br>– split address block “0x00 5055 to 0x00 509F” into “0x00 5055 to 0x00 509D” with “Reserved, “0x00 509E” with “SYSCFG” and “0x00 509F” with “Reserved”,<br>– added a footnote to RST_SR Reset status value,<br>– updated CLK_CCOR Reset status value to “0x10”.<br>Updated description of OPT0 in *Table 11: Option byte description*.<br>Updated $V_{IN}$ Max values in *Table 13: Voltage characteristics*.<br>Added *Section 9.3.4: ProxSense Regulator Voltage*.<br>Removed $ACC_{HSI\_PXS}$ rows from *Table 25: HSI_PXS oscillator characteristics* and removed former *Figure 17 Typical HSI_PXS frequency vs. VDD*.<br>Added $t_{prog}$ and $I_{prog}$ Max. values to *Table 28: Flash program memory*.<br>Removed $V_{OL}$ row with Conditions $I_{IO}$=+20 mA and $V_{DD}$=3.0 V from *Table 31: I/O static characteristics*.<br>Updated “ProxSense I/O” Conditions and Min. values in *Table 32: Output driving current (high sink ports)*.<br>Added *Section 3.13: General purpose and basic timers*. |
| 07-Aug-2013 | 4 | Updated OPT0 default value in *Table 10: Option byte*. |
| 18-Mar-2015 | 5 | Updated:<br>– *Figure 27: SPI timing diagram - slave mode and CPHA = 0*,<br>– *Section 10.2: UFQFPN48 package information*,<br>– *Section 10.3: UFQFPN28 package information*,<br>– *Section 10.4: TSSOP20 package information*.<br>Added:<br>– *Figure 33: UFQFPN48 marking example (package top view)*,<br>– *Figure 36: UFQFPN28 marking example (package top view)*,<br>– *Figure 39: TSSOP20 marking example (package top view)*. |

**Table 45. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 28-May-2015 | 6 | Updated *Figure 27: SPI timing diagram - slave mode and CPHA = 0*. |
| 01-Jul-2015 | 7 | Added the footnotes about “D” and E1” dimensions below *Table 43: TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data*. |

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