MRF175GU
MRF175GV

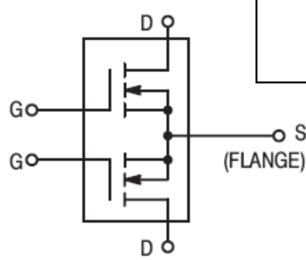
The RF MOSFET Line
200/150W, 500MHz, 28V

M/A-COM Products
Released - Rev. 07.07

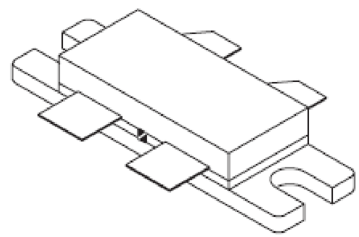
Designed for broadband commercial and military applications using push pull circuits at frequencies to 500 MHz. The high power, high gain and broadband performance of these devices makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

N–Channel enhancement mode

- Guaranteed performance
  - MRF175GV @ 28 V, 225 MHz (“V” Suffix)
    - Output power — 200 W
    - Power gain — 14 dB typ
    - Efficiency — 65% typ`
- 100% ruggedness tested at rated output power
- Low thermal resistance
- Low C_{rss} — 20 pF typ @ V_{DS} = 28 V



Product Image



CASE 375–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	26	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	400 2.27	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.5	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	µAdc

(continued)

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Visit www.macomtech.com for additional data sheets and product information.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 5.0 A)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	2.0	3.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	180	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	200	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	20	—	pF
FUNCTIONAL CHARACTERISTICS — MRF175GV (2) (Figure 1)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	12	14	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	η	55	65	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each side of device measured separately.
2. Measured in push–pull configuration.

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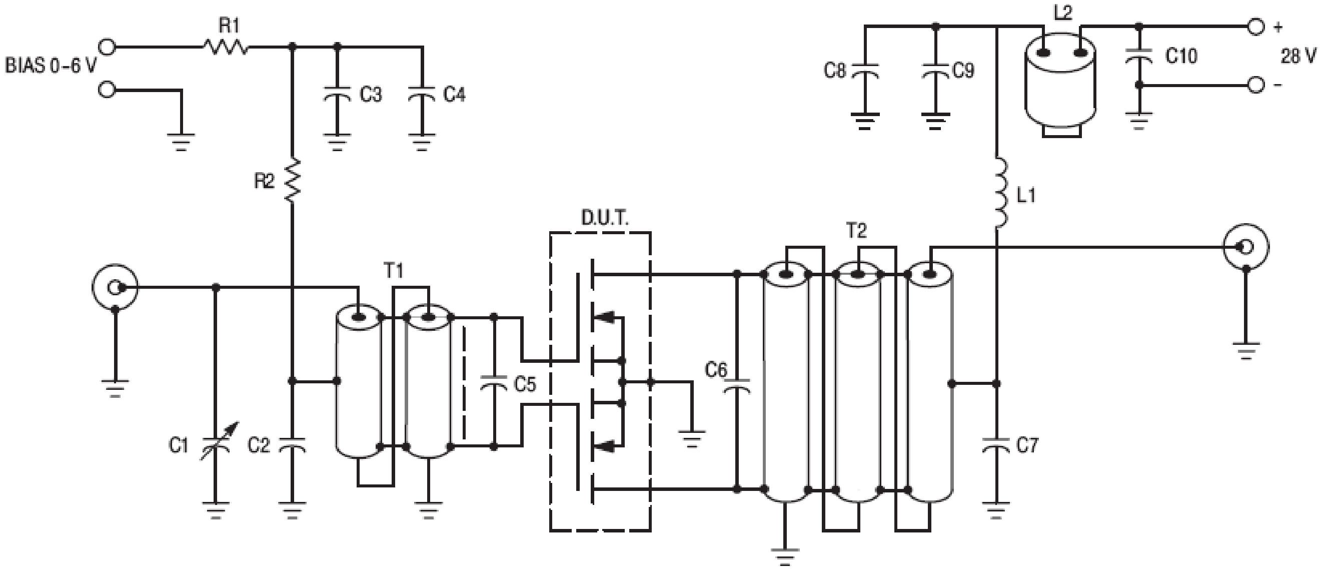


C1 — Arco 404, 8.0–60 pF
C2, C3, C7, C8 — 1000 pF Chip
C4, C9 — 0.1 µF Chip
C5 — 180 pF Chip
C6 — 100 pF and 130 pF Chips in Parallel
C10 — 0.47 µF Chip, Kemet 1215 or Equivalent
L1 — 10 Turns AWG #16 Enamel Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 µH Total Inductance

Board material — .062″ fiberglass (G10), Two sided, 1 oz. copper, $\varepsilon_r \cong 5$

Unless otherwise noted, all chip capacitors are ATC Type 100 or Equivalent.

R1 — 100 Ohms, 1/2 W
R2 — 1.0 k Ohm, 1/2 W
T1 — 4:1 Impedance Ratio RF Transformer. Can Be Made of 25 Ohm Semirigid Coax, 47–52 Mils O.D.
T2 — 1:9 Impedance Ratio RF Transformer. Can Be Made of 15–18 Ohms Semirigid Coax, 62–90 Mils O.D.

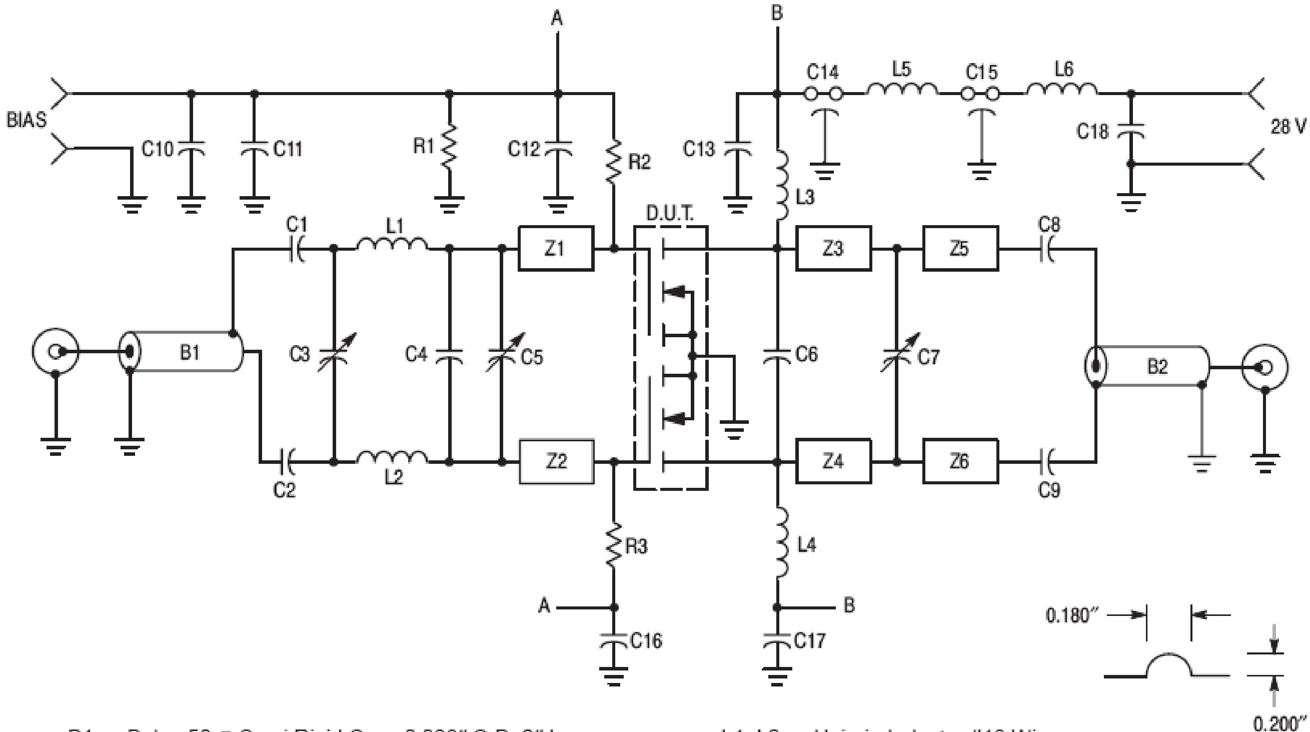
NOTE: For stability, the input transformer T1 should be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

Figure 1. 225 MHz Test Circuit

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS — MRF175GU (1) (Figure 2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	10	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTE:
1. Measured in push–pull configuration.



B1 — Balun 50 Ω Semi Rigid Coax 0.086″ O.D. 2″ Long
B2 — Balun 50 Ω Semi Rigid Coax 0.141″ O.D. 2″ Long
C1, C2, C8, C9 — 270 pF ATC Chip Cap
C3, C5, C7 — 1.0–20 pF Trimmer Cap
C4 — 15 pF ATC Chip Cap
C6 — 33 pF ATC Chip Cap
C10, C12, C13, C16, C17 — 0.01 µF Ceramic Cap
C11 — 1.0 µF 50 V Tantalum
C14, C15 — 680 pF Feedthru Cap
C18 — 20 µF 50 V Tantalum

L1, L2 — Hairpin Inductor #18 Wire
L3, L4 — 12 Turns #18 Enameled Wire 0.340″ I.D.
L5 — Ferroxcube VK200 20/4B
L6 — 3 Turns #16 Enameled Wire 0.340″ I.D.
R1 — 1.0 kΩ 1/4 W Resistor
R2, R3 — 10 kΩ 1/4 W Resistor
Z1, Z2 — Microstrip Line 0.400″ x 0.250″
Z3, Z4 — Microstrip Line 0.870″ x 0.250″
Z5, Z6 — Microstrip Line 0.500″ x 0.250″

Board material — 0.060″ Teflon–fiberglass, ε_r = 2.55, copper clad both sides, 2 oz. copper.

Figure 2. 400 MHz Test Circuit

TYPICAL CHARACTERISTICS

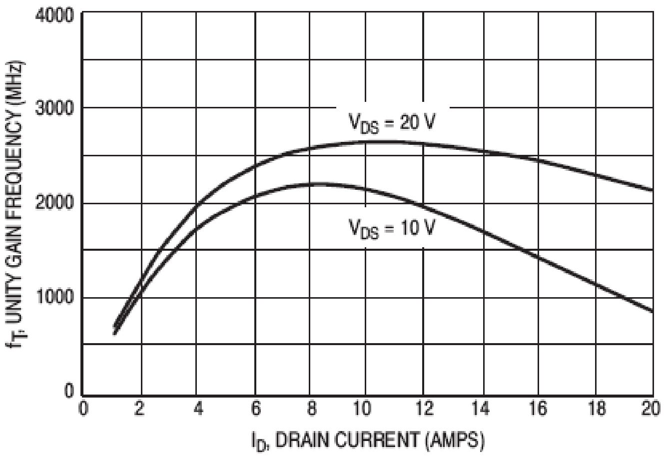


Figure 3. Common Source Unity Current Gain Frequency versus Drain Current

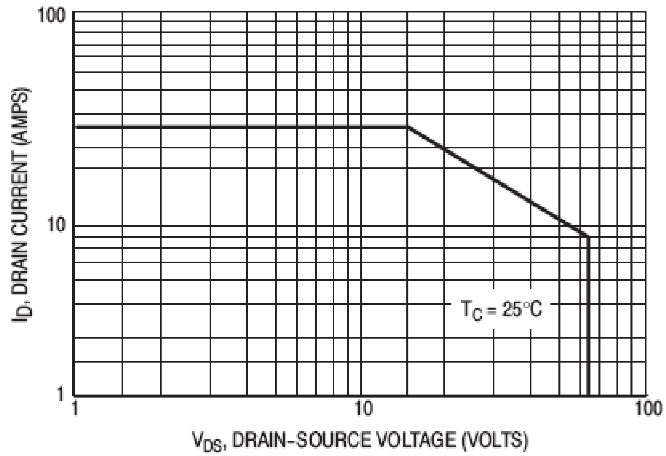


Figure 4. DC Safe Operating Area

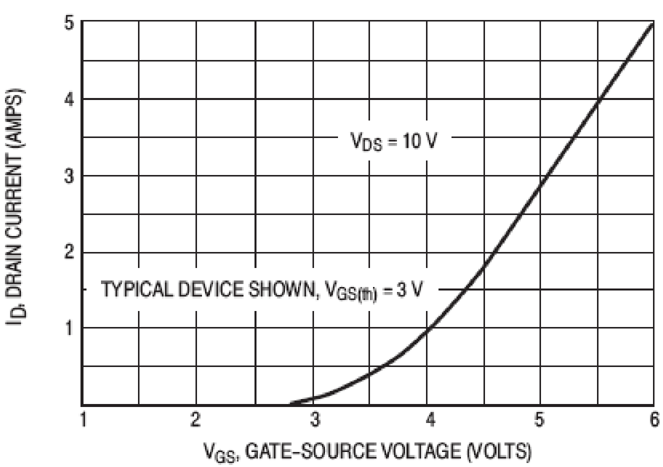


Figure 5. Drain Current versus Gate Voltage (Transfer Characteristics)

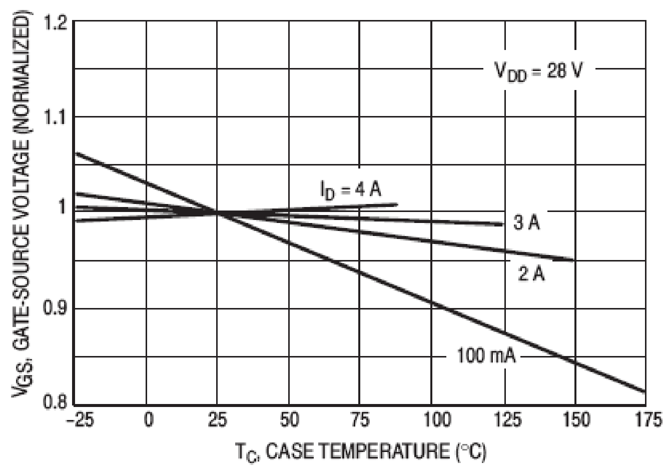


Figure 6. Gate–Source Voltage versus Case Temperature

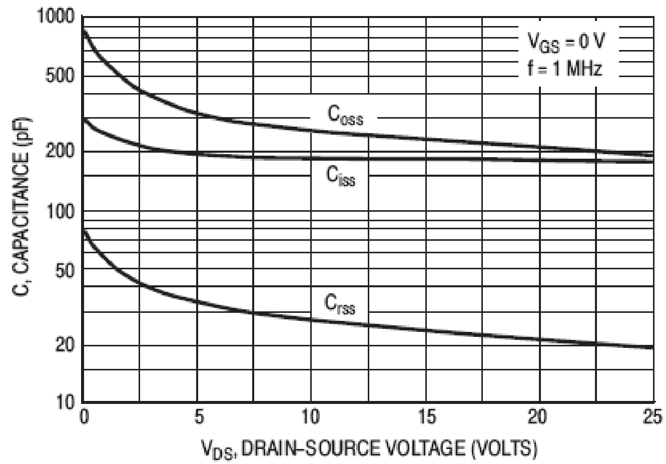


Figure 7. Capacitance versus Drain–Source Voltage*

* Data shown applies to each half of MRF175GU/GV.

TYPICAL CHARACTERISTICS

MRF175GV

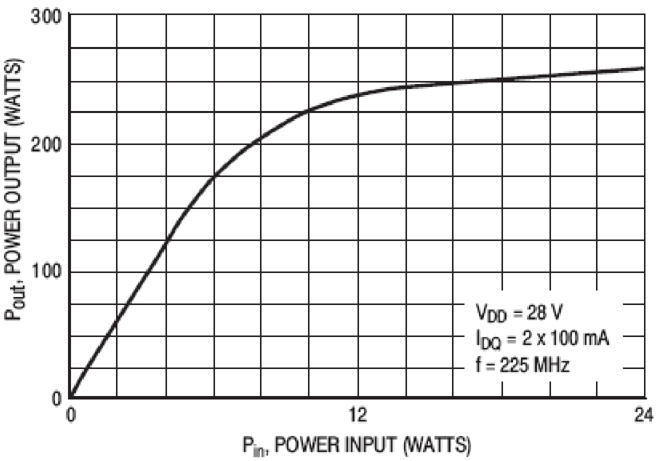


Figure 8. Power Input versus Power Output

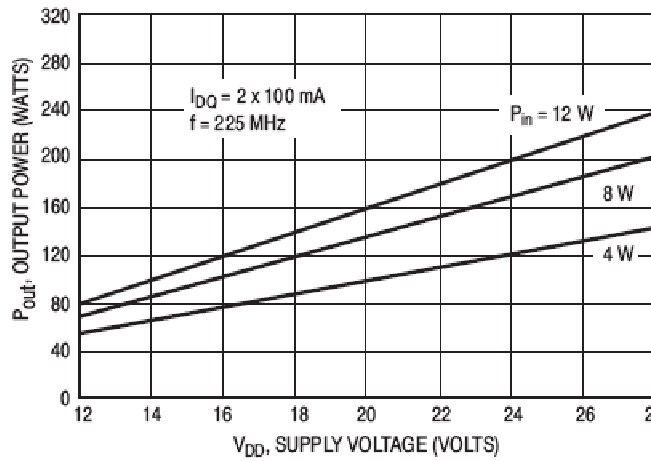


Figure 9. Output Power versus Supply Voltage

MRF175GU

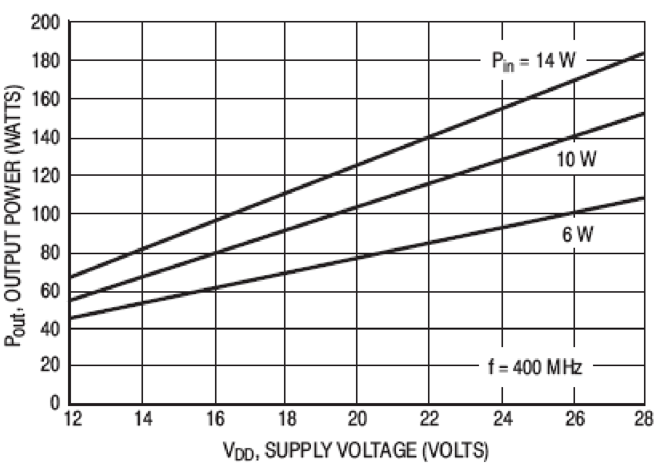


Figure 10. Output Power versus Supply Voltage

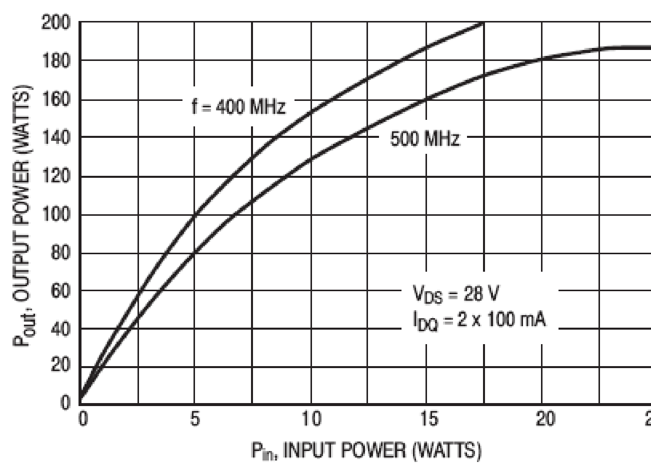


Figure 11. Output Power versus Input Power

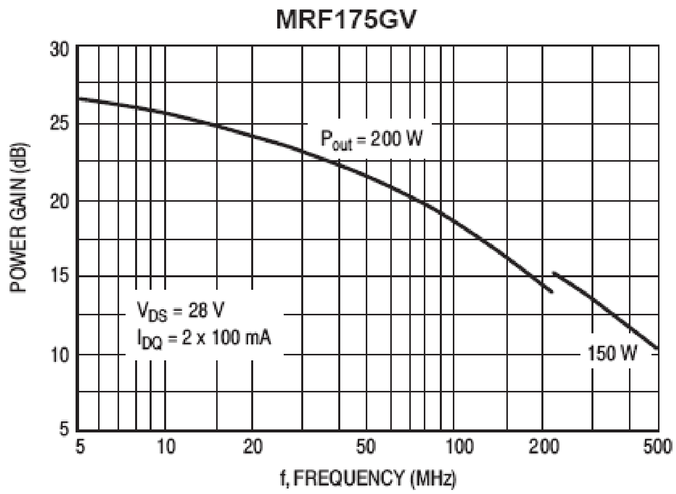


Figure 12. Power Gain versus Frequency

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
50	0.926	–174	5.43	81	0.009	12	0.861	–177
70	0.924	–176	3.85	76	0.009	6	0.869	–178
80	0.923	–176	3.35	73	0.008	18	0.864	–178
90	0.921	–177	2.94	70	0.008	17	0.871	–178
100	0.918	–178	2.57	68	0.008	17	0.875	–178
103	0.920	–178	2.52	67	0.007	23	0.871	–178
105	0.920	–178	2.47	67	0.008	20	0.875	–179
110	0.921	–178	2.32	65	0.008	21	0.877	–178
120	0.923	–179	2.08	63	0.005	27	0.862	–178
130	0.928	–179	1.93	61	0.008	34	0.883	–178
135	0.929	–180	1.86	60	0.007	22	0.887	–178
140	0.929	–180	1.77	59	0.009	27	0.887	–178
145	0.931	180	1.68	58	0.008	30	0.890	–178
150	0.931	180	1.63	57	0.007	39	0.894	–178
155	0.934	180	1.55	56	0.008	29	0.891	–178
160	0.936	180	1.48	55	0.007	35	0.889	–178
165	0.934	180	1.44	54	0.009	36	0.888	–178
170	0.936	179	1.40	53	0.008	38	0.891	–178
175	0.937	179	1.34	52	0.009	35	0.893	–178
180	0.941	179	1.29	51	0.009	40	0.894	–178
185	0.941	179	1.25	50	0.010	39	0.897	–178
190	0.939	179	1.20	49	0.009	49	0.901	–178
192	0.937	179	1.18	49	0.010	44	0.904	–178
195	0.935	179	1.15	48	0.010	44	0.903	–178
200	0.933	179	1.12	47	0.011	49	0.903	–179
205	0.923	178	1.09	47	0.012	46	0.906	–179
210	0.907	180	1.04	46	0.013	22	0.911	–179
215	0.930	–180	1.01	45	0.008	27	0.910	–179
220	0.933	180	0.99	45	0.008	39	0.912	–179
225	0.935	179	0.96	43	0.009	37	0.913	–179
230	0.932	179	0.92	43	0.009	39	0.915	–179
235	0.933	178	0.90	42	0.009	43	0.917	–180
240	0.935	178	0.87	41	0.009	46	0.918	–180
245	0.936	178	0.85	40	0.009	56	0.920	–180
250	0.935	178	0.82	39	0.010	47	0.921	180
275	0.948	176	0.72	36	0.009	55	0.928	180
300	0.966	175	0.64	33	0.010	59	0.932	179
325	0.969	175	0.57	30	0.012	66	0.935	178
350	0.957	175	0.51	27	0.013	60	0.939	178
375	0.939	174	0.45	25	0.015	80	0.941	177

Table 1. Common Source S–Parameters (V_{DS} = 28 V, I_D = 4.5 A) (continued)

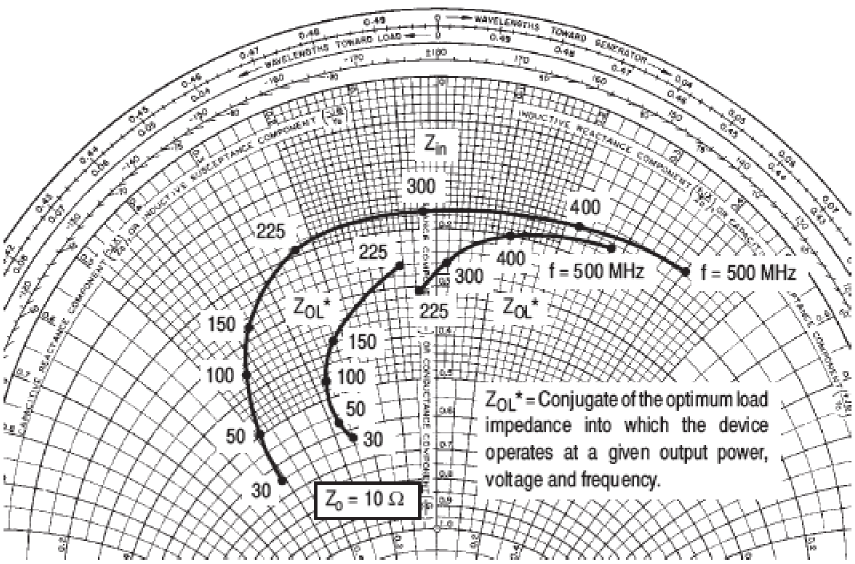
f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
400	0.943	172	0.41	23	0.017	75	0.946	176
405	0.945	172	0.40	22	0.016	71	0.946	176
410	0.948	171	0.40	22	0.016	68	0.944	176
415	0.956	171	0.39	21	0.017	74	0.949	176
420	0.963	171	0.38	21	0.018	72	0.946	176
425	0.966	171	0.37	20	0.018	70	0.947	176
430	0.968	170	0.37	20	0.019	72	0.948	176
435	0.970	170	0.36	19	0.019	75	0.949	175
440	0.971	170	0.36	19	0.019	73	0.952	175
445	0.978	169	0.32	17	0.017	71	0.965	177
450	0.978	169	0.31	17	0.019	70	0.964	177
455	0.977	170	0.31	17	0.019	73	0.965	177
460	0.978	170	0.31	16	0.019	70	0.967	177
465	0.977	169	0.30	16	0.020	73	0.963	177
470	0.973	169	0.29	15	0.021	71	0.966	177
475	0.973	169	0.29	15	0.021	72	0.967	177
480	0.970	169	0.28	15	0.022	71	0.967	177
485	0.964	169	0.28	14	0.022	74	0.963	176
490	0.960	169	0.28	14	0.022	73	0.965	176
495	0.957	169	0.27	14	0.023	71	0.963	176
500	0.957	169	0.27	13	0.023	71	0.963	176
505	0.951	168	0.26	13	0.023	70	0.966	176
510	0.948	168	0.26	13	0.022	68	0.965	176
515	0.943	167	0.25	13	0.022	72	0.966	175

Table 1. Common Source S–Parameters (V_{DS} = 28 V, I_D = 4.5 A) (continued)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
520	0.940	167	0.25	12	0.021	68	0.966	175
525	0.940	167	0.25	12	0.022	74	0.968	175
530	0.943	166	0.24	11	0.022	67	0.965	175
535	0.944	166	0.24	11	0.022	69	0.964	174
540	0.945	165	0.23	11	0.022	69	0.965	174
545	0.951	165	0.23	11	0.023	70	0.969	174
550	0.952	164	0.23	10	0.023	72	0.969	174
555	0.956	164	0.23	10	0.023	70	0.969	174
560	0.958	164	0.22	10	0.025	70	0.968	174
565	0.962	164	0.22	9	0.024	70	0.969	174
570	0.963	164	0.22	9	0.024	71	0.972	174
575	0.970	164	0.21	9	0.024	70	0.972	174
600	0.973	164	0.20	8	0.029	71	0.973	173
625	0.955	164	0.19	8	0.030	69	0.970	172
650	0.933	162	0.17	7	0.031	69	0.966	171
675	0.928	160	0.16	6	0.034	69	0.969	170
700	0.946	158	0.15	6	0.034	67	0.973	169
750	0.952	158	0.14	4	0.040	67	0.969	168
800	0.907	155	0.13	5	0.044	65	0.962	166
850	0.928	151	0.12	5	0.049	55	0.963	164
900	0.915	152	0.11	4	0.049	52	0.955	163
950	0.869	148	0.11	4	0.053	49	0.941	161
1000	0.902	146	0.11	4	0.055	44	0.943	159

Table 1. Common Source S–Parameters (V_{DS} = 28 V, I_D = 4.5 A) (continued)

INPUT AND OUTPUT IMPEDANCE



V_{DD} = 28 V, I_{DQ} = 2 x 100 mA

f MHz	Z_{in} OHMS	Z_{OL}* OHMS
(P_{out} = 150 W)		
225	1.95 – j2.30	3.10 – j0.25
300	1.75 – j0.20	2.60 + j0.20
400	1.60 + j2.20	2.00 + j1.20
500	1.35 + j4.00	1.70 + j2.70
(P_{out} = 200 W)		
30	6.50 – j5.10	6.30 – j2.50
50	5.00 – j4.80	5.75 – j2.75
100	3.60 – j4.20	4.60 – j2.65
150	2.80 – j3.60	2.60 – j2.20
225	1.95 – j2.30	2.60 – j0.60

NOTE: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 13. Series Equivalent Input/Output Impedance

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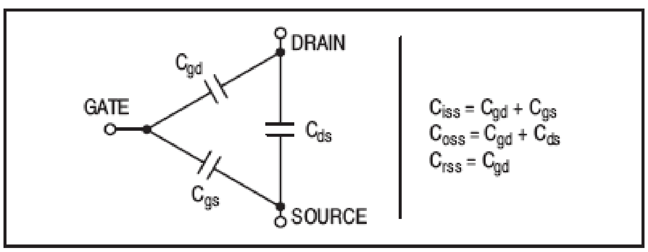
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zerovolts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



The C_{iss} givenin the electrical characteristics table was measured using method 2 above. It should be noted that C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the highertemperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain
current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.
Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.
Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.
Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.
Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

DESIGN CONSIDERATIONS

The MRF175G is a RF power N–channel enhancement mode field–effect transistor (FETs) designed for HF, VHF and

RF POWER MOSFET CONSIDERATIONS

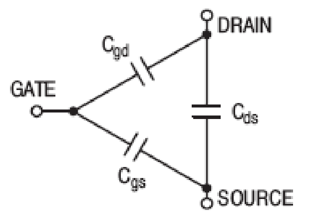
MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.

2. Positive voltage of the drain in respect to source and zerovolts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

The C_{iss} givenin the electrical characteristics table was measured using method 2 above. It should be noted that C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes. Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

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HANDLING CONSIDERATIONS

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DESIGN CONSIDERATIONS

The MRF175G is a RF power N–channel enhancement mode field–effect transistor (FETs) designed for HF, VHF andUHF power amplifier applications. M/A-COM RF MOSFETs feature a vertical structure with a planar design. M/A-

COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

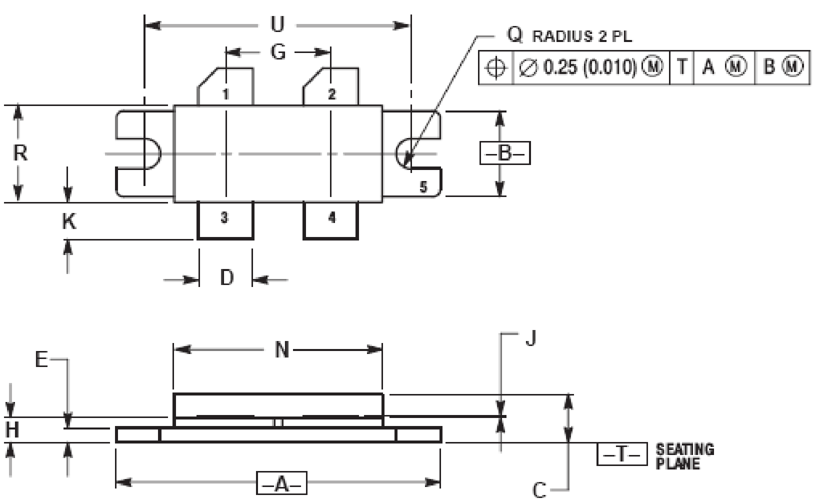
DC BIAS

The MRF175G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF175G was characterized at I_{DQ} = 100 mA, each side, which is the suggested minimumvalue of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters. The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

Power output of the MRF175G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.330	1.350	33.79	34.29
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.430	0.440	10.92	11.18
H	0.102	0.112	2.59	2.84
J	0.004	0.006	0.11	0.15
K	0.185	0.215	4.83	5.33
N	0.845	0.875	21.46	22.23
Q	0.060	0.070	1.52	1.78
R	0.390	0.410	9.91	10.41
U	1.100 BSC		27.94 BSC	

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375–04
ISSUE D