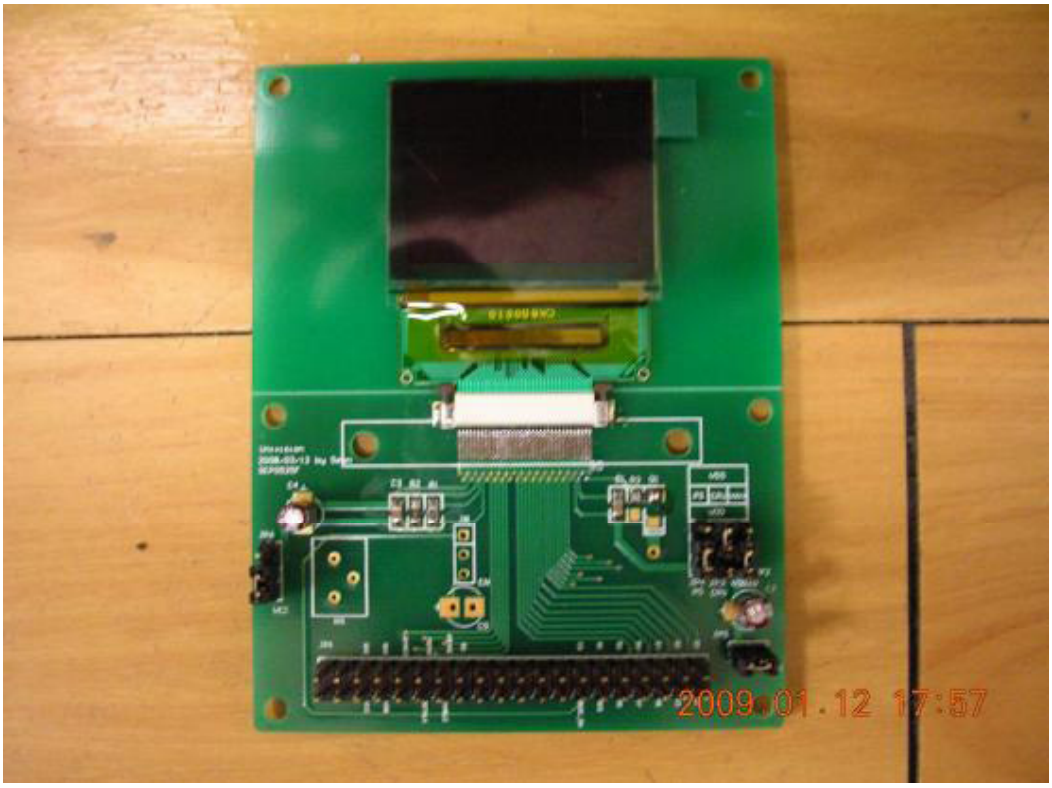
DENSITRON DISPLAYS

OLED DISPLAY MODULE

Application Notes

PRODUCT NUMBER	DD-160128FC-1A/2A with EVK board



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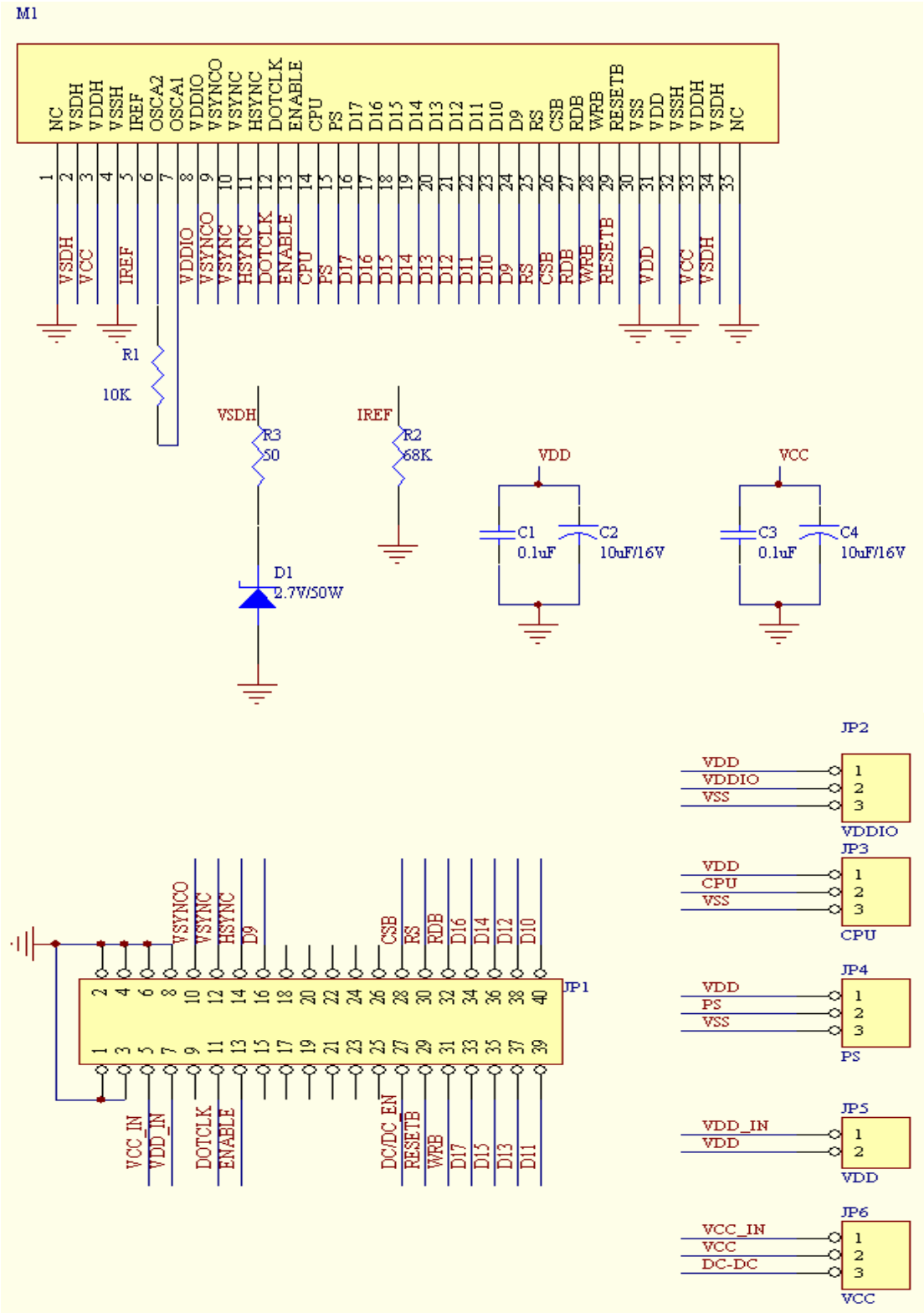
REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	30 Sep 06			First Issue	
B	13 Jan 09			Second Issue	

1 EVK Schematic



Symbol Definition

D17-D9：These pins are 9-bit bi-directional data bus to be connected to the MCU's data bus.

D17-D10： These are for command and data inputs (8bit parallel interface).

CSB：These pins are CSB pins for master and slave driver IC. This pin is the chip select input. The chip is enabled for MCU communication only when CSB is pulled low.

CPU： Selects the CPU type.
Low: 80-series CPU
High: 68-Series CPU

PS： Selects parallel/Serial interface type.
Low: serial
High: parallel.

RDB： For an 80-system bus interface, read strobe signal(active low).
For a 68-system bus interface, bus enable strobe (active high).
When using SPI, fix it to VDD or VSS level.

WRB：For an 80-system bus interface, write strobe signal (active low).
For a 68-system bus interface, read/write select.
Low: Write
High: Read.
When using SPI, fix it to VDD or VSS level.

RESB：Reset SEPS525F(active low).

VCC ：External Column Driving Power Supply.
VDD ：Logic power supply.
VSS ：Power supply ground.

HV：External Column Driving Power Supply.

LV：Logic power supply.

GND：Power supply ground.

Note1: Please ground the unused data pins
Note2: If you do not use RGB Interface, please ground VSYNC, HSYNC, Enable, DOTCLK and floating VSYNCO.
Note3: If you do not use VDDIO, please connect it to LV (VDD).

2 Timing characteristics

80-Series MPU parallel Interface (write timing)

(VDD = 2.8V, Ta = 25˚C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tAH8	-	5	-	ns	CSB
Address setup timing	tAS8		5		ns	RS
System cycle timing	tCYC8	-	100	-	ns	WRB
Write “L” pulse width	tWRLW8		45		ns	
Write “H” pulse width	tWRHW8		45		ns	
Data setup timing	tDS8	-	30	-	ns	DB[17:0]
Data hold timing	tDH8		10		ns	

All the timing reference is 10% and 90% of VDD

Table 1 80-Series MPU Parallel Interface Timing Characteristics (Write)

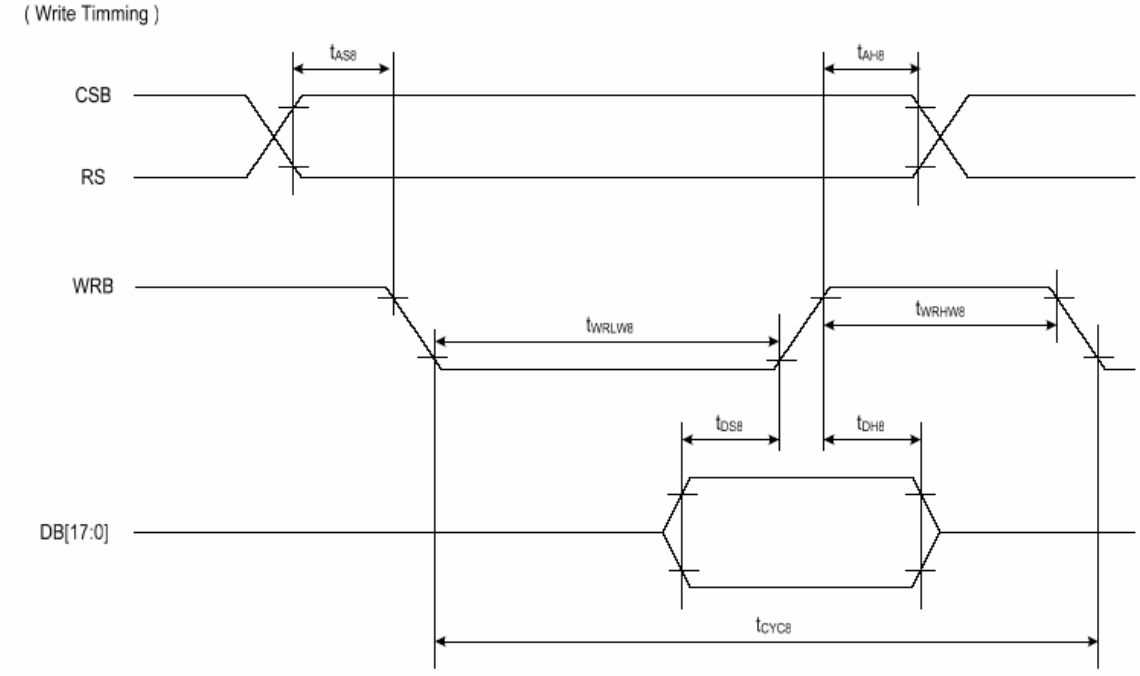


Figure 1 80-Series MPU parallel Interface Timing Diagram (Write)

80-Series MPU parallel Interface (Read timing)

(VDD = 2.8V, Ta = 25˚C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tAH8	-	5	-	ns	CSB
Address setup timing	tAS8		5		ns	RS
System cycle timing	tCYC8	-	200	-	ns	RDB
Read "L" pulse width	tWRLW8		90		ns	
Read "H" pulse width	tWRHW8		90		ns	
Data setup timing	tDS8	CL = 15 pF	-	60	ns	DB[17:0]
Data hold timing	tDH8		0		ns	

All the timing reference is 10% and 90% of VDD

Table 2 80-Series MPU Parallel Interface Timing Characteristics (Read)

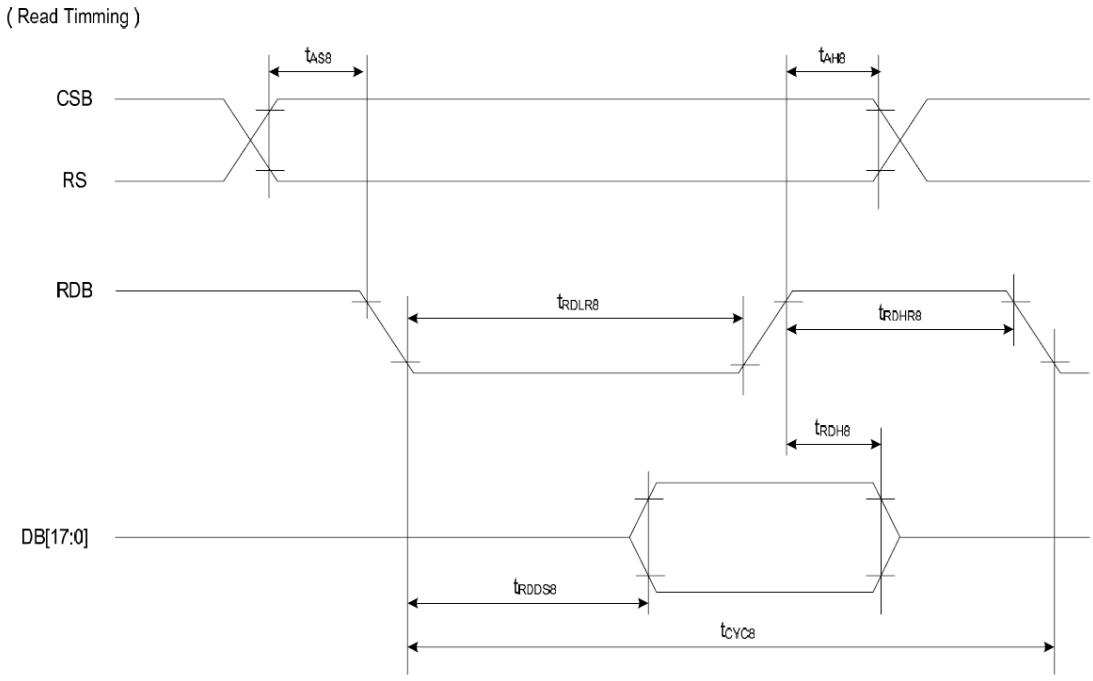


Figure 2 80-Series MPU parallel Interface Timing Diagram (Read)

6800-Series MPU parallel Interface (write timing)

(VDD = 2.8V, Ta = 25˚C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tAH8	-	5	-	ns	CSB
Address setup timing	tAS8		5		ns	RS
System cycle timing	tCYC8	-	100	-	ns	E
Write “L” pulse width	tWRLW8		45		ns	
Write “H” pulse width	tWRHW8		45		ns	
Data setup timing	tDS8		40	-	ns	DB[17:0]
Data hold timing	tDH8		10		ns	

All the timing reference is 10% and 90% of VDD

Table 3 6800-Series MPU Parallel Interface Timing Characteristics (Write)

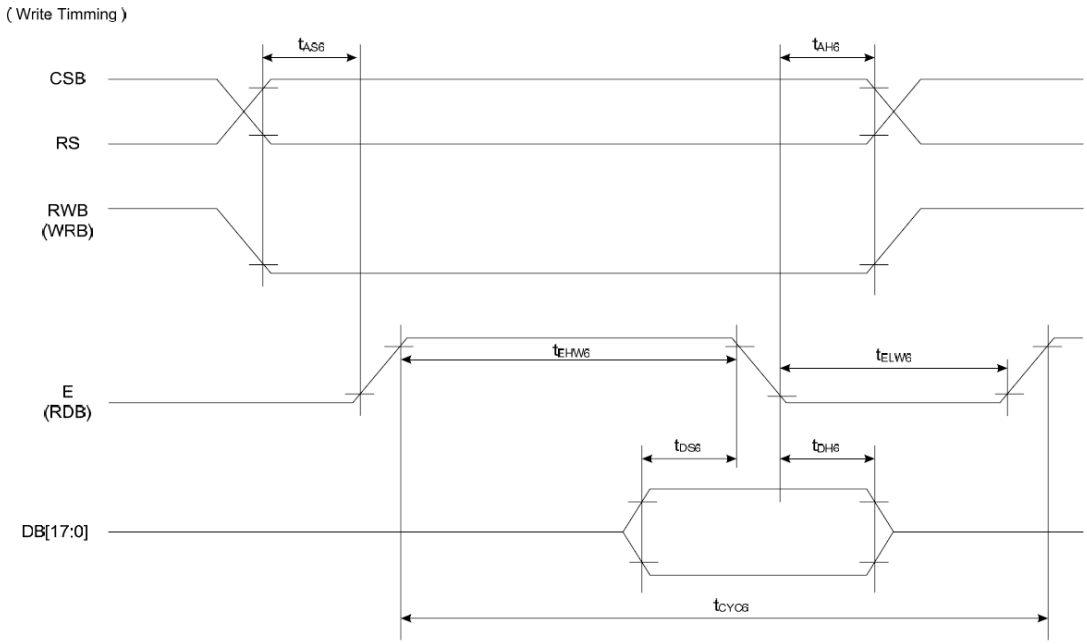


Figure 3 6800-Series MPU parallel Interface Timing Diagram (Write)

68-Series MPU parallel Interface (Read timing)

(VDD = 2.8V, Ta = 25˚C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tAH8	-	10	-	ns	CSB
Address setup timing	tAS8		10		ns	RS
System cycle timing	tCYC8	-	200	-	ns	E
Read “L” pulse width	tWRLW8		90		ns	
Read “H” pulse width	tWRHW8		90		ns	
Data setup timing	tDS8	CL = 15 pF	0	70	ns	DB[17:0]
Data hold timing	tDH8				ns	

All the timing reference is 10% and 90% of VDD

Table 4 80-Series MPU Parallel Interface Timing Characteristics (Read)

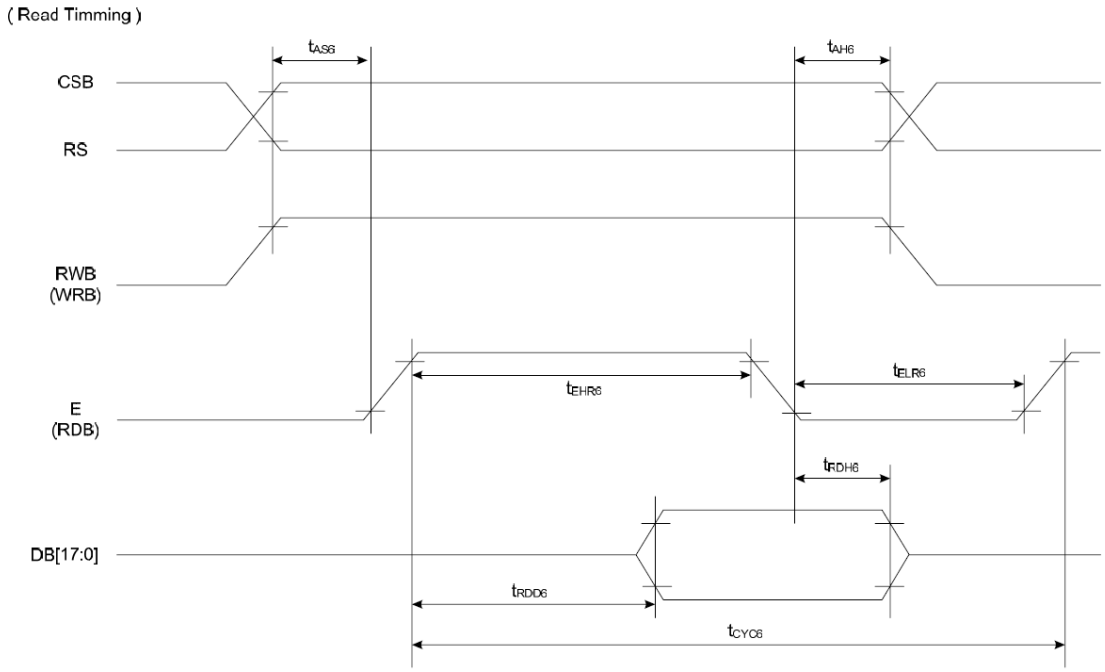


Figure 4 6800-Series MPU parallel Interface Timing Diagram (Read)

SPI Interface

(VDD = 2.8V, Ta = 25˚C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Serial clock cycle	tCYCS	-	60	-	ns	SCL
SCL "H" pulse width	tSHW		25		ns	
SCL "L" pulse width	tSLW		25		ns	
Data setup timing	tDSS	-	25	-	ns	SDI
Data hold timing	tDHS		25		ns	
CSB□SCL timing	tCSS	-	25	-	ns	CSB
CSB□hold timing	tCSH				ns	

All the timing reference is 10% and 90% of VDD

Table 5 SPI Interface Timing Characteristics

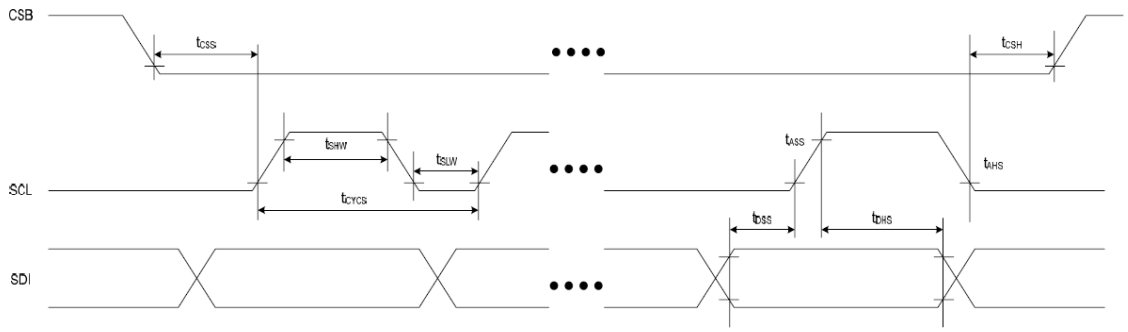
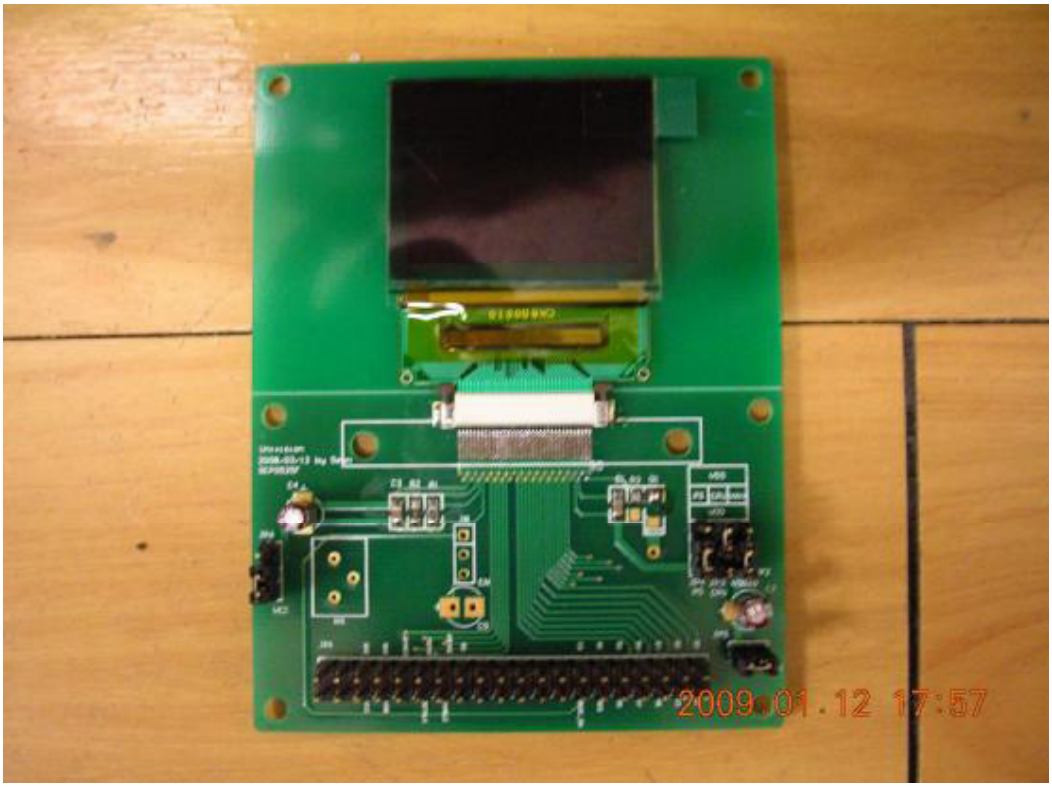


Figure 5 SPI Interface Timing Characteristics

3 Connection Between OLED and EVK

Figure 6 EVK PCB and DD-160128FC-1A/2A Module

Figure 7 DD-160128FC-1A/2A and EVK assembled (Top view)



The SEPS525F is a COF type package, which means that the connect pads are on the top of the display connector. When the EVK and display are assembled, finally push the locking pad to hold the display in place, see Figure 6 and Figure 7.
User can use wires to connect the EVK with the system. The example is shown below in figure 8;

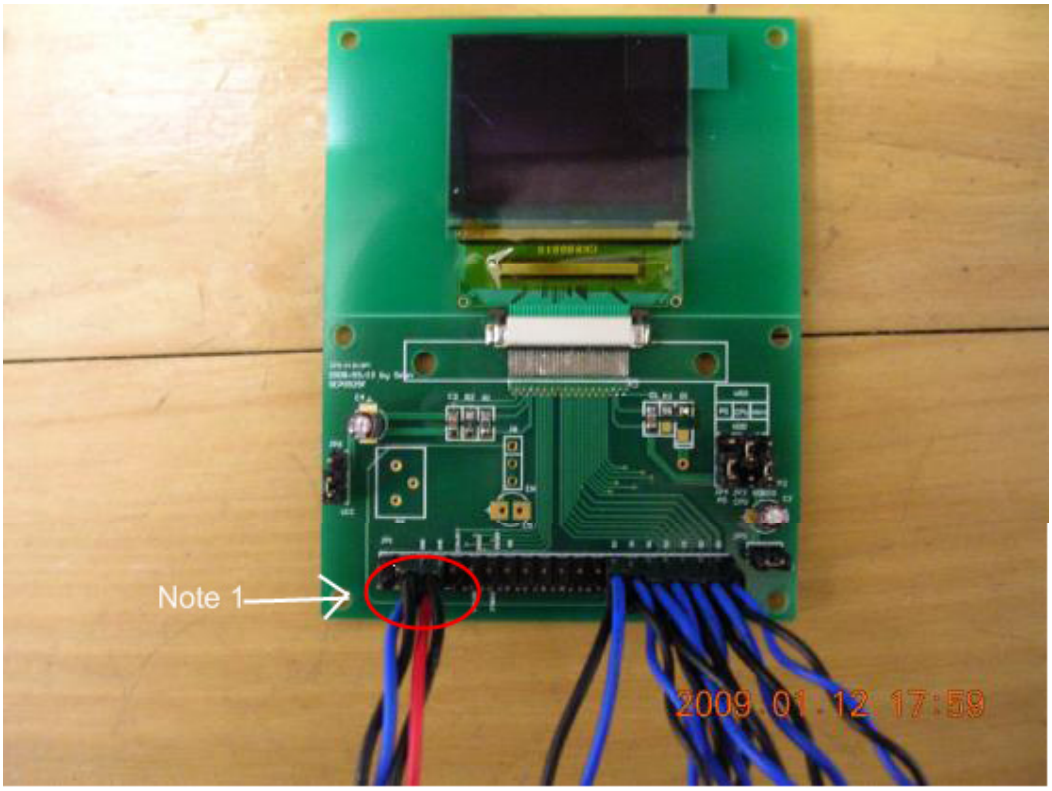


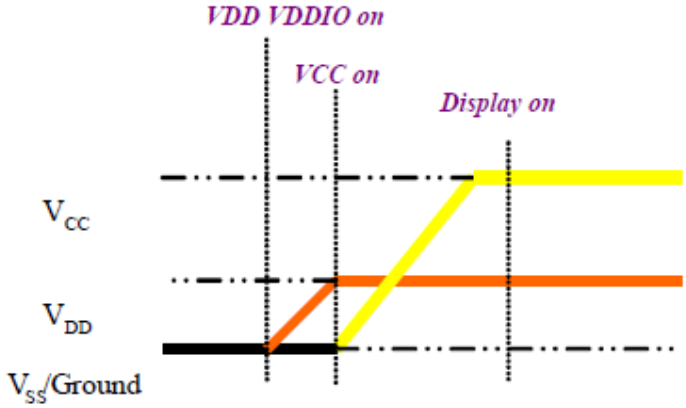
Figure 8 control MCU (not supplied) connected with EVK

Note 1：It is the external most positive voltage supply. In this sample it is connected to power supply.

6. Power down and Power up Sequence

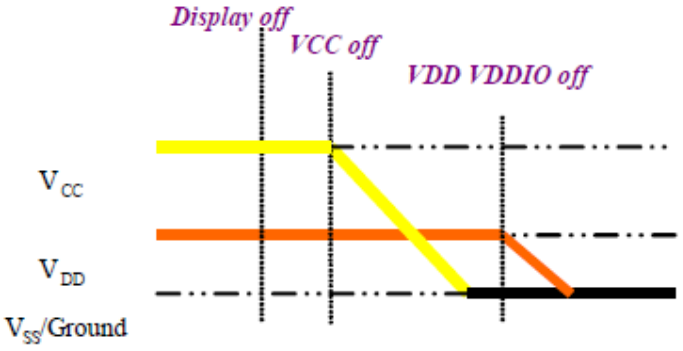
To protect OLED panel and to extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

Power up Sequence:



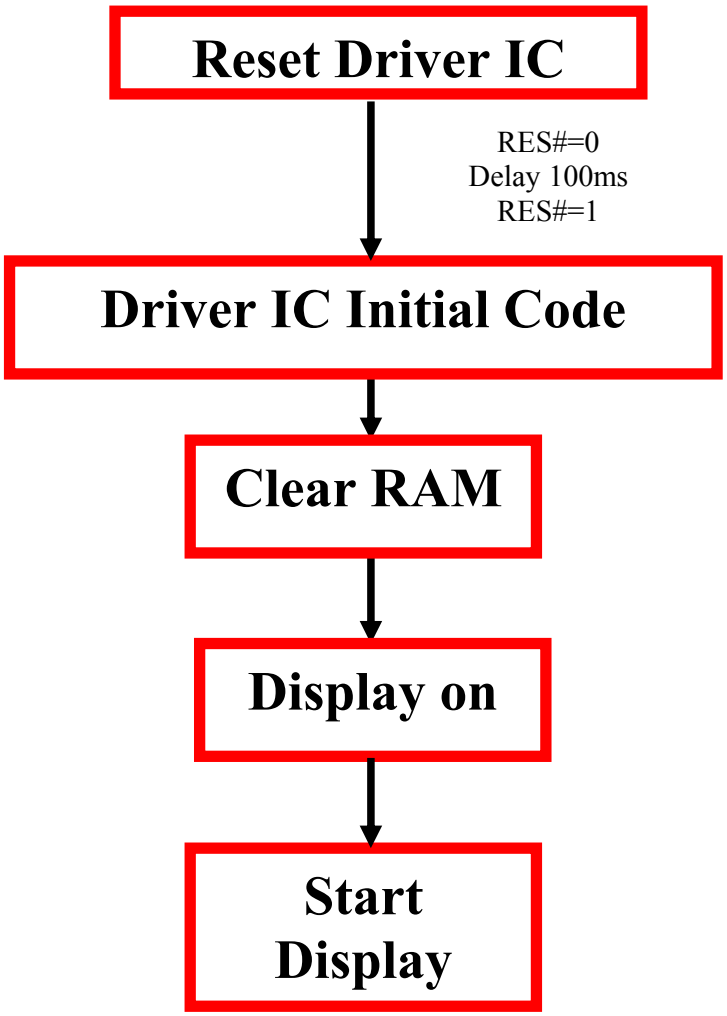
1. Power up VDD and VDDIO
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(when V_{DD} is stable)
7. Send Display on command

Power down Sequence:



1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
4. Power down VDD and VDDIO

4 How to use the DD-160128FC-1A/2A



4.1 Recommended Initial code for 80 interface

```
write_c(0x06); // Display off
write_d(0x00);
write_c(0x02); // OSC_CTL
write_d(0x01);
write_c(0x03); // CLOC_DIV
write_d(0x30); // 115Hz
write_c(0x04); // REDUCE_CURRENT
write_d(0x00);
write_c(0x80); // IREF
```

```
write_d(0x00);
write_c(0x08); // PRECHARGE_TIME_R
write_d(0x01);
write_c(0x09); // PRECHARGE_TIME_G
write_d(0x01);
write_c(0x0a); // PRECHARGE_TIME_B
write_d(0x02);
write_c(0x0b); // PRECHARGE_CURRENT_R
write_d(0x0C);
write_c(0x0C); // PRECHARGE_CURRENT_G
write_d(0x19);
write_c(0x0d); // PRECHARGE_CURRENT_B
write_d(0x15);
write_c(0x10); // DRIVING_CURRENT_R
write_d(0x32);
write_c(0x11); // DRIVING_CURRENT_G
write_d(0x27);
write_c(0x12); // DRIVING_CURRENT_B
write_d(0x2B);
write_c(0x13); // DISPLAY_MODE_SET
write_d(0x00);
write_c(0x14); // RGB_IF
write_d(0x21);
write_c(0x15); // RGB_POL
write_d(0x00);
write_c(0x16); // MEMORY_WRITE_MODE
write_d(0x76);
write_c(0x17); // MX1_ADDR
write_d(0x00);
write_c(0x18); // MX2_ADDR
write_d(0x9f);
write_c(0x19); // MY1_ADDR
write_d(0x00);
write_c(0x1a); // MY2_ADDR
write_d(0x7f);
write_c(0x20); // MEMORY_ACCESSPOINTER X
write_d(0x00);
write_c(0x21); // MEMORY_ACCESSPOINTER X
write_d(0x00);
write_c(0x28); // DUTY
write_d(0x7f);
write_c(0x29); // DISPLAY START LINE
write_d(0x00);
write_c(0x2e); // D1_DDRAM_FAC
write_d(0x00);
write_c(0x2f); // D1_DDRAM_FAR
write_d(0x00);
write_c(0x31); // D2_DDRAM_FAC
write_d(0x00);
write_c(0x32); // D2_DDRAM_FAR
write_d(0x00);
write_c(0x33); // SCR1_FX1
write_d(0x00);
write_c(0x34); // SCR1_FX2
write_d(0x9f);
write_c(0x35); // SCR1_FY1
write_d(0x00);
write_c(0x36); // SCR1_FY1
```

```
write_d(0x7f);
write_c(0x06); // Display on
write_d(0x01);
```

Sub Function for 80 Interface

```
void write_c(unsigned char out_command)
{
RS=0;
CS=0;
WR=0;
P1=out_command;
WR=1;
CS=1;
RS=1;
}
void write_d(unsigned char out_data)
{
RS=1;
CS=0;
WR=0;
P1=out_data;
WR=1;
CS=1;
}
void White_pattern()
{
write_c(0x20); // MEMORY_ACCESSPOINTER X
write_d(0x00);
write_c(0x21); // MEMORY_ACCESSPOINTER X
write_d(0x00);
write_c(0x22);
  for(i=0;i<128;i++)
  {
      for(j=0;j<160;j++)
      {
      write_d(0xfc);
      write_d(0xfc);
      write_d(0xfc);
      }
   }
 }
```

Recommended Initial Code and Sub Function

Note：1.For 80 series CPU interface.

2. For 8bits Ttiple Transfer 262K support.

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