

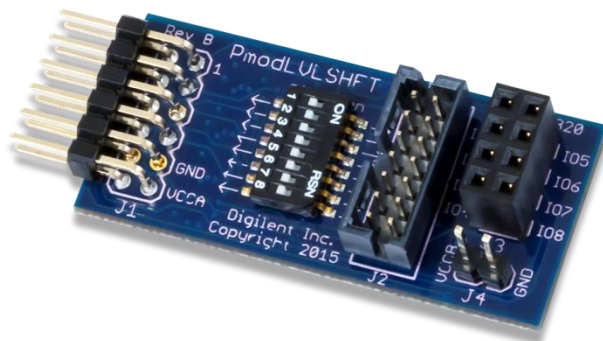
## PmodLVLSHFT™ Reference Manual

Revised April 12, 2016

This manual applies to the PmodLVLSHFT rev. B

### Overview

The Digilent PmodLVLSHFT is a digital logic level shifter. This module is ideal for users who want to supply logic signals following a 3.3V CMOS standard but have an alternate logic level output that is used for other applications such as JTAG programming.



*The PmodLVLSHFT.*

- Digital logic level shifter
- Translate logic signals between two user supplied voltage levels
- 2x7 JTAG header
- 8 miniature switches to dictate logic level conversion
- Voltage range between 1.8V and 5.5V
- Small PCB size for flexible designs 1.8 in × 0.8 in (4.6 cm × 2.0 cm)
- 12-pin Pmod port with GPIO interface

## 1 Functional Description

The PmodLVLSHFT translates logic signals between two user supplied voltage levels. Users can use a small object such as a pen or a screwdriver to adjust the switches for the direction of the voltage translation.

## 2 Interfacing with the Pmod

The PmodLVLSHFT communicates with the host board via GPIO. Users can supply any form of digital signals to either end of the Pmod and have them translated to the other voltage level. Switches are provided to indicate the direction of the voltage translation. A switch pushed to the left side (green) towards the pin header translates voltages from VCCB to VCCA; a switch on the right side (yellow) towards the JTAG header translates from VCCA to VCCB.

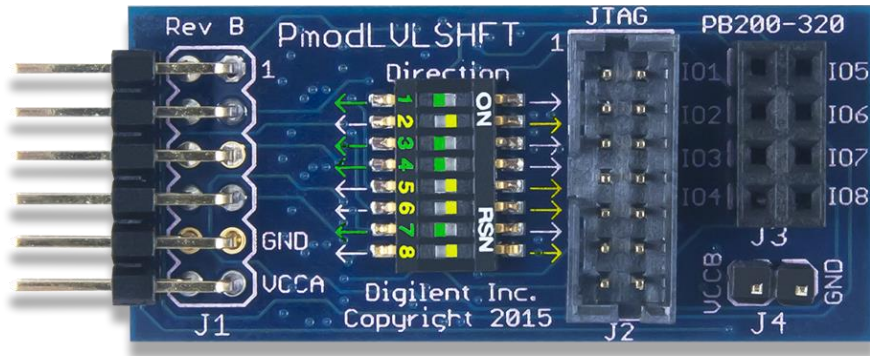


Figure 1. Switches indicating the voltage direction.

A pinout table for the PmodLVLSHFT is provided below:

Header J1			JTAG Header J2			Header J3		
Pin	Signal	Description	Pin	Signal	Description	Pin	Signal	Description
1	AIO1/TMS	A1 & TMS JTAG pin	1	GND	Power Supply Ground	1	BIO1/TMS	B1 & TMS JTAG pin
2	AIO2/TDI	A2 & TDI JTAG pin	2	VCCB	Power Supply side B	2	BIO5/SRST	B5 & Signal Reset pin
3	AIO3/TDO	A3 & TDO JTAG pin	3	GND	Power Supply Ground	3	BIO2/TDI	B2 & TDI JTAG pin
4	AIO4/TCK	A4 & TCK JTAG pin	4	BIO1/TMS	B1 & TMS JTAG pin	4	BIO6	I/O pin B6
5	GND	Power Supply Ground	5	GND	Power Supply Ground	5	BIO3/TDO	B3 & TDO JTAG pin
6	VCCA	Power Supply side A	6	BIO4/TCK	B4 & TCK JTAG pin	6	BIO7	I/O pin B7
7	AIO5	I/O pin A5	7	GND	Power Supply Ground	7	BIO4/TCK	B4 & TCK JTAG pin
8	AIO6	I/O pin A6	8	BIO3/TDO	B3 & TDO JTAG pin	8	BIO8	I/O pin B8
9	AIO7	I/O pin A7	9	GND	Power Supply Ground	Header J4		
10	AIO8	I/O pin A8	10	BIO2/TDI	B2 & TDI JTAG pin	Pin	Signal	Description
11	GND	Power Supply Ground	11	GND	Power Supply Ground	1	VCCB	Power Supply side B
12	VCCA	Power Supply side A	12	(NC)	Not Connected	2	GND	Power Supply Ground
			13	GND	Power Supply Ground			
			14	SRST	Signal Reset			

Table 1. Pin descriptions for the PmodLVLSHFT.

**Note\*** Headers J2 and J3 follow the JTAG pin numbering convention as opposed to the Pmod header numbering convention

Any external power applied to the PmodLVLSHFT must be within 1.8V and 5.5V.

### 3 Physical Dimensions

The pins on the pin header are spaced 100 mil apart. The PCB is 1.75 inches long on the sides parallel to the pins on the pin header and 0.8 inches long on the sides perpendicular to the pin header.

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