Intel® LXT312A/LXT315A

Low Power T1 PCM Repeaters/Transceivers

Datasheet

The LXT312A and LXT315A are integrated repeater/transceiver circuits for T1 carrier systems. The LXT312A is a dual repeater/transceiver and the LXT315A is a single repeater/transceiver.

The LXT312A and LXT315A are designed to operate as regenerative repeaters/transceivers for 1.544 Mbps data rate PCM lines. Each includes all circuits required for a regenerative repeater/transceiver system including the equalization network, automatic line build-out (ALBO), and a state-of-the-art analog/digital clock extraction network tuned by an external crystal.

The key feature of the LXT312A family is that it requires only a crystal and a minimum of other components to complete a repeater/transceiver design. Compared with traditional tuned coil-type repeaters/transceivers, they offer significant savings in component and labor costs, along with reduced voltage drop/power consumption, and improved reliability. To ensure performance for all loop lengths, the LXT312A and LXT315A are 100% AC/DC tested using inputs generated by Intel's proprietary transmission line and network simulator.

The LXT312A and LXT315A are advanced CMOS devices which require only a single 5-volt power supply.

Product Features

- Integrated repeater/transceiver circuit on a single CMOS chip
- On-chip equalization network
- On-chip ALBO
- Low power consumption
- No tuning coil
- On-chip Loopback
- Recovered Clock Output
- 0 to 36 dB dynamic range
- -11 dB interference margin
- Compatible with CB113/TA24 specifications
- Single 5 V CMOS technology
- Available in 16-pin PDIP and 44-pin PLCC

Order Number: 249071-003
12-Jan-2006

Datasheet

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Revision History

LXT312A/LXT315A Repeater/Transceiver - Revision 003 Revision Date: 12-Jan-2006	
Page Number	**Description**
8	Modified Figure 2, “LXT312A / LXT315A Pin Assignments and Package Markings” .
20	Added Section 6.1, “Top Label Markings”.
22	Added Section 7.0, “Product Ordering Information”.

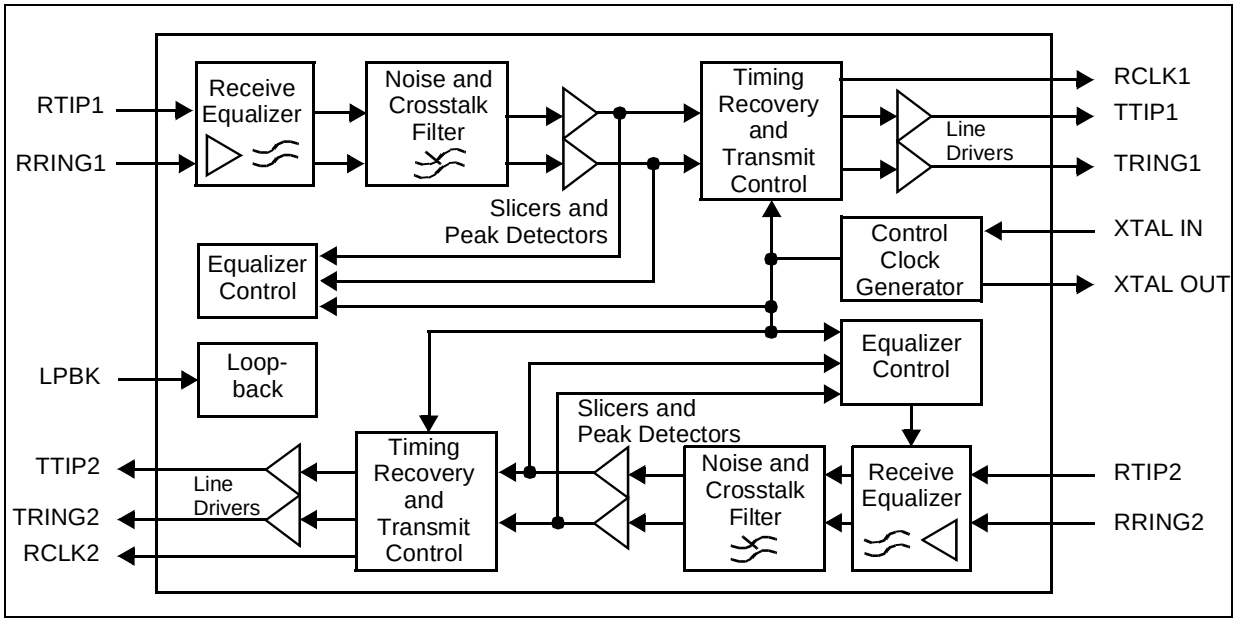
LXT312A/LXT315A Repeater/Transceiver - Revision 002 Revision Date: July 2003	
Page Number	**Description**
Front Page	Removed first sentence, “This data sheet also applies to the LXT312/LXT315 products.”
5	Added new chapter title, Chapter 1.0, “Block Diagram”.
6	Removed from Figure 2, “LXT312A/LXT315A Pin Assignments and Package Markings”, the package drawings for the LXT312PE and LXT315PE. Changed text from LXT312NE to LXT312A. Changed text from LXT315NE to LXT315A.
6	In Table 2, “Intel® LXT312A / LXT315A Signal Descriptions”, removed the ‘PLCC’ column. Changed text for first footnote and removed second footnote.
10	In Figure 3, “Typical T1 Dual Repeater/Transceiver Application”, changed text from LXT31
17	In Chapter 6.0, “Mechanical Specifications”, changed title of Figure 14, “LXT312NE / LXT315NE Package Specifications” to “LXT312A / LXT315A Package Specifications”.
-	In Chapter 6.0, “Mechanical Specifications”, removed Figure 15, “LXT312PE / LXT315PE Package Specifications”.

LXT312A/LXT315A Repeater/Transceiver - Revision 001 Revision Date: January 2001	
-	Initial Release

1.0 Block Diagram

Figure 1 is a block diagram of the LXT312A/LXT315A.

Figure 1. LXT312A / LXT315A Block Diagram



2.0 Pin Assignments and Signal Descriptions

Table 1 lists the top-side markings for the LXT312A/315A transceivers.

Table 1. LXT312A / LXT315A Repeater/Transceiver Package Top-Side Markings

Marking	Location of Marking	Definition
Part Number	Center of package	Number of the unique identifier for this product family
Revision Number	To the right of the part number	Two-digit number of particular silicon revision, also known as a 'stepping'. (For information on specific silicon steppings, see specification update documents for the LXT312A/LXT315A repeater/ transceiver.)
Lot Number	Directly underneath part number	A lot (that is, 'batch') number
FPO Number	Directly underneath lot number	The Finish Process Order number

Figure 2. LXT312A / LXT315A Pin Assignments and Package Markings

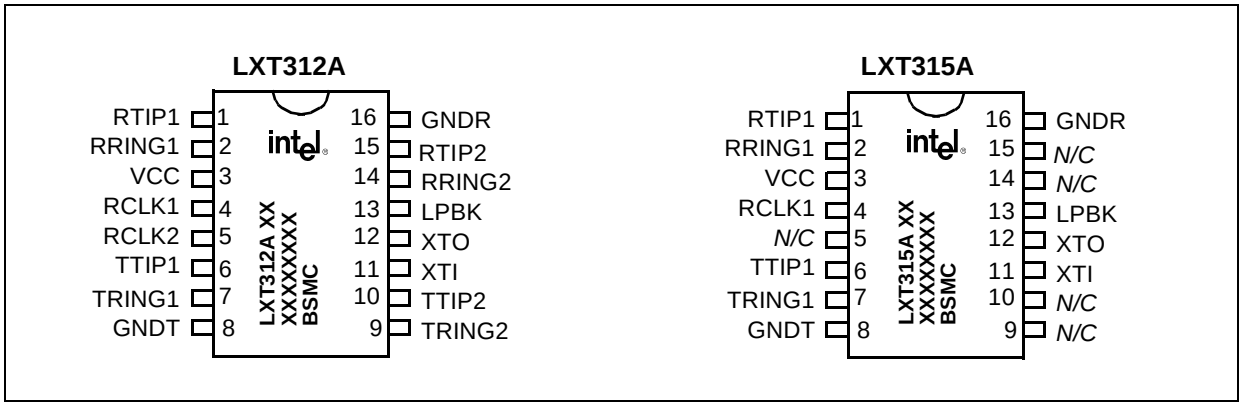


Table 2. LXT312A / LXT315A Signal Descriptions (Sheet 1 of 2)

Pin	Symbol	I/O	Description
1 2	RTIP1 RRING1	I I	**Repeater Tip and Ring Inputs.** Tip and ring receive inputs for Channel 1.
3	VCC	–	**Power Supply.** Power supply input for all circuits. +5 V (±0.25 V).
4	RCLK1	O	**Recovered Clock.** Clock output recovered from Channel 1 receive input.
5[1]	RCLK2	O	**Recovered Clock.** On the LXT312A dual repeater/transceiver, this is the recovered clock output for Channel 2.
6 7	TTIP1 TRING1	O O	**Repeater Tip and Ring Outputs.** Open-drain output drivers for Channel 1.
1. On the LXT312A and LXT315A single repeater/transceiver, these pins are not connected (N/C).			

Table 2. LXT312A / LXT315A Signal Descriptions (Sheet 2 of 2)

Pin	Symbol	I/O	Description
8	GNDT	–	**Transmit Ground.** Ground return for transmit circuits.
9[1] 10[1]	TRING2 TTIP2	O O	**Side 2 Ring and Tip Outputs.** On the LXT312A dual repeater/transceiver, these are open-drain output drivers for Channel 2.
11 12	XTI XTO	I O	**Crystal Oscillator Pins.** A 6.176-MHz crystal should be connected across these two pins. For alternative timing references, refer to Application Information.
13	LPBK	I	**Loopback Control.** On the LXT312A, this pin controls Loopback Selection: Low = No Loopback. High = Loopback side 1 data to side 2. ***On LXT315A single repeater/transceiver, this pin must be connected to GND.***
14[1] 15[1]	RRING2 RTIP2	I I	**Side 2 Ring and Tip Inputs.** On the LXT312A repeater/transceiver, these are tip and ring receive inputs for Channel 2.
16	GNDR	–	**Receive Ground.** Ground return for receive circuits.

1. On the LXT312A and LXT315A single repeater/transceiver, these pins are not connected (N/C).

3.0 Functional Description

3.1 Introduction

PCM signals are attenuated and dispersed in time as they travel down a transmission line. Repeaters/transceivers are required to amplify, reshape, regenerate, and retime the PCM signal, then retransmit it.

The LXT312A and LXT315A each contain all the circuits required to build a complete PCM repeater/transceiver. The operational range of the repeaters/transceivers is 0 to 36 dB of cable loss at 772 kHz (equal to 6300 feet of 22 gauge pulp-insulated cable between repeaters).

3.2 Receive Function

The signal is received through a 1:1 transformer at RTIP and RRING and equalized for up to 36 dB of cable loss. The receive equalizer uses a proprietary on-chip adaptive filter technique which is equivalent to a 3-port ALBO equalizer design. The monolithic structure of the filter and the absence of external components provide excellent ISI and dispersion elimination, and accurate data transfer over temperature.

Receiver noise immunity is optimized by a proprietary crosstalk elimination filter which eliminates the unnecessary high-frequency components of the received signal.

The equalized signal is full wave rectified and used to generate information for the timing recovery circuit. This circuit uses a mixed analog/digital technique to provide a low-jitter PLL similar to a tuned tank with excellent jitter tracking ability. But unlike a tuned tank, the free running frequency of the PLL clock is accurately controlled by the external reference crystal. No adjustment is required. Refer to Table 3 for crystal specifications.

Recovered clock signals are available on the RCLK pins for applications that require bit stream synchronization.

3.3 Transmit Function

Recovered data is re-synchronized to the recovered clock signal by the timing recovery and transmit control section. The data is then retransmitted to the network via two open-drain, high-voltage transistors.

3.4 Loopback Function (LXT312A Only)

The LXT312A includes a loopback function for network diagnostics. With the LPBK pin Low, the repeater/transceiver operates in the normal mode. When the LPBK pin is pulled High, the data is looped back from side 1 to side 2.

4.0 Application Information

Figure 3 shows a typical T1 dual repeater/transceiver application using an LXT312A repeater/transceiver with standard PCB edge connectors. It includes a jumper-selectable shorting option (dashed lines at connector pins 2 and 7) for the fault location circuitry. Table 3 lists the specifications for the crystal used with the LXT312A or LXT315A repeater.

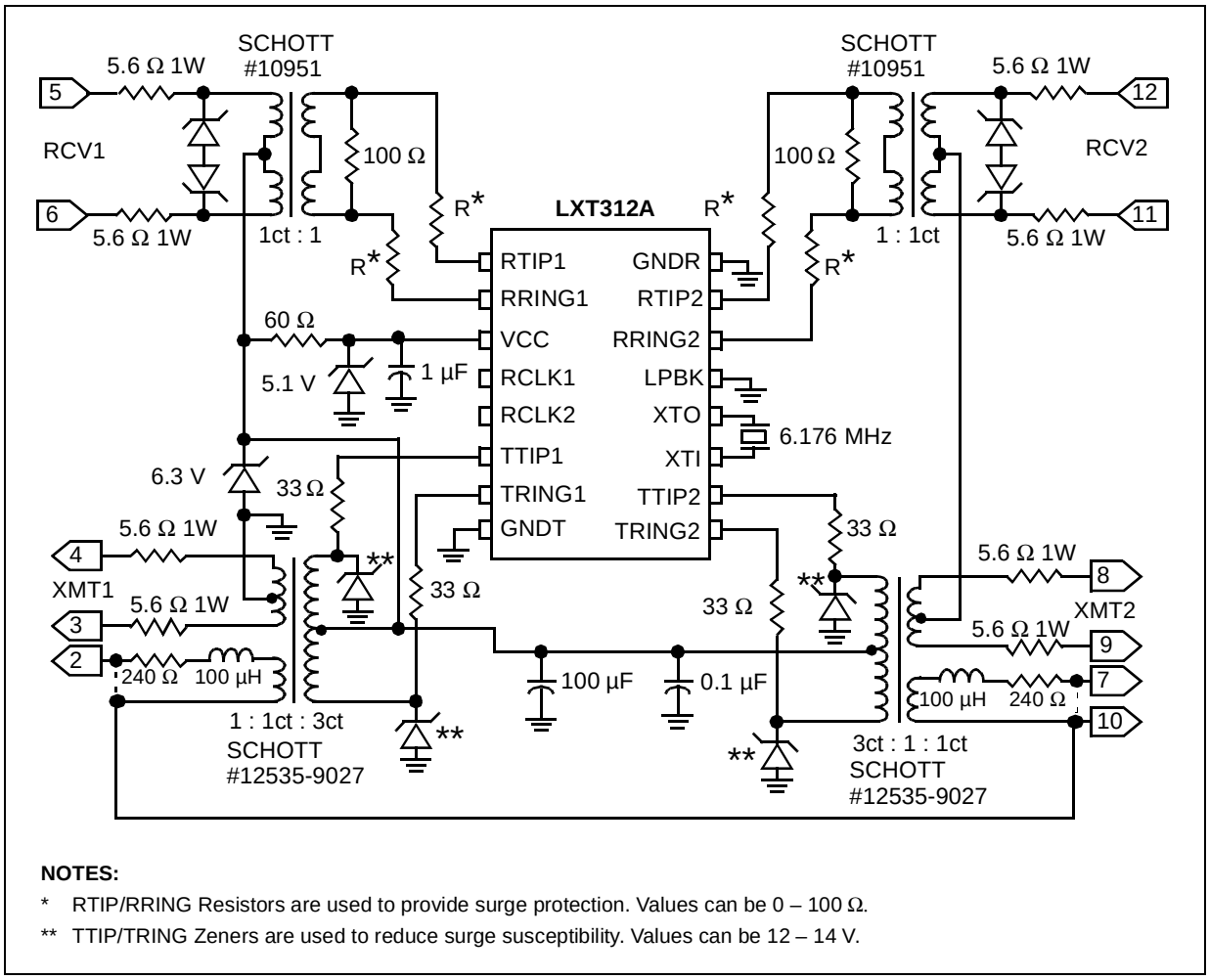
For applications where a crystal is not appropriate, a 1.544 MHz or 6.176 MHz, CMOS-level (High ≥ 4.5V, Low ≤ 0.5V) oscillator may be connected to XTI. In this situation, XTO must be tied to VCC and GND via a voltage divider as shown in Figure 4.

Table 3. Crystal Specifications

Parameter	Specification
Frequency	6.176 MHz
Frequency tolerance[1]	± 50 ppm
Effective series resistance	40 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental

1. @ 25 °C, C Load = 10 pF and from -40 °C to +85 °C (Ref 25 °C reading).

Figure 3. Typical T1 Dual Repeater/Transceiver Application

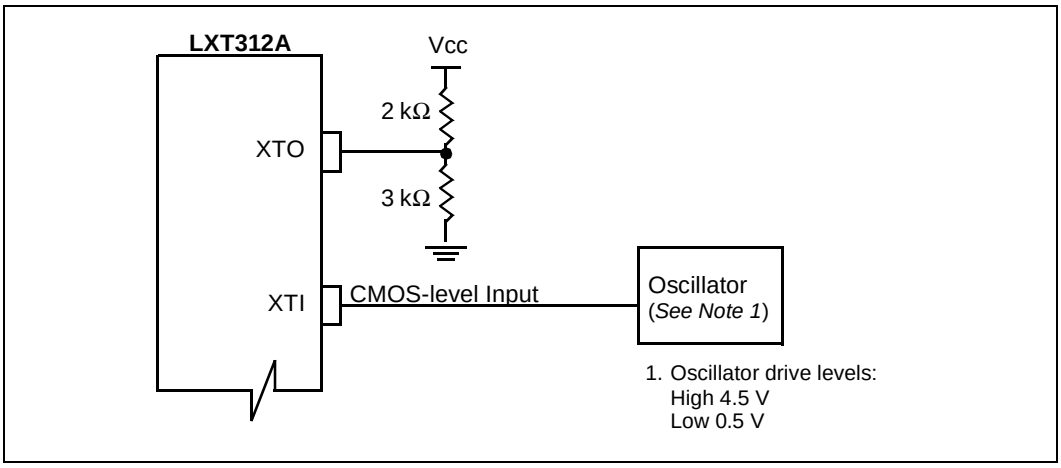


NOTES:

* RTIP/RRING Resistors are used to provide surge protection. Values can be 0 – 100 Ω.

** TTIP/TRING Zeners are used to reduce surge susceptibility. Values can be 12 – 14 V.

Figure 4. Alternate Timing Reference Circuitry



5.0 Test Specifications and Test Setups

5.1 Test Specifications

Note: Minimum and maximum values in Table 4 through Table 7 and Figure 5 through Figure 13 represent the performance specifications of the LXT312A/315A repeaters/transceivers and are guaranteed by test except, as noted, by design.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Unit
Supply voltage (min to max)	V_{CC}	-0.3 V to +6 V
Driver voltage	V_{OH}	18 V
Receiver current	I_{CC}	100 mA
Operating temperature (min to max)	T_{OP}	-40 °C to +85 °C
Storage temperature (min to max)	T_{ST}	-65 °C to +150 °C
Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.		

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	-40	—	85	° C

Table 6. Electrical Characteristics - Over Recommended Range

Parameter		Symbol	Min	Typ[1]	Max	Unit
Interference margin		SNR	-11	–	–	dB
Receiver dynamic range		–	-36	–	0	dB
Digital outputs - low	(I_{OL} = 1.6 mA	V_{OL}	–	–	0.4	V
	(I_{OL} = 10 µA)	V_{OL}	–	0.2	–	V
Digital outputs - high	(I_{OH} = 0.4 mA	V_{OH}	2.4	–	–	V
	(I_{OH} < 10 µA)	V_{OH}	–	4.5	–	V
Digital inputs - high		V_{IH}	2.0	–	–	V
Digital inputs - low		V_{IL}	–	–	0.8	V

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

Table 6. Electrical Characteristics - Over Recommended Range

Parameter		Symbol	Min	Typ[1]	Max	Unit
Supply current (from VCC supply)[2]	All zeros	I_{CC}	–	15	22	mA
	All ones	I_{CC}	–	–	23	mA
Driver leakage current (V_{DVR} = 18 V)		I_{LL}	–	–	150	µA
Driver pulse amplitude (Driver output I_O = 20 mA)		A_P	0.65	–	0.95	V

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

Figure 5. Digital Timing Characteristics

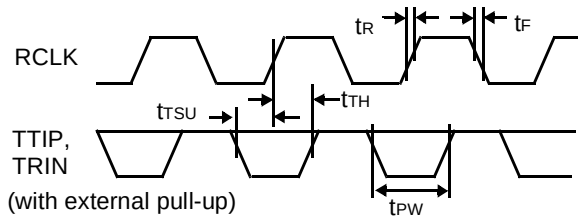


Table 7. Digital Timing Characteristics - Over Recommended Range

Parameter	Symbol	Min	Typ[1]	Max	Unit
Driver pulse width	t_{PW}	299	324	349	ns
Driver pulse imbalance	–	–	–	15	ns
Rise and fall time (any digital output[2])	t_R / t_F	–	–	18	ns
Setup time - TTIP/TRING to RCLK	t_{TSU}	90	–	–	ns
Hold time - TTIP/TRING from RCLK	t_{TH}	90	–	–	ns

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

5.2 Test Setups

Both the LXT312A and LXT315A are fully tested (100% AC and DC parameters) using inputs generated by Intel's proprietary transmission line and network simulator. Device testing includes receiver jitter tolerance, jitter transfer and interference margin, and receiver immunity to Gaussian and 60 Hz noise. Specifications and bench test setups are shown in Figure 6 through Figure 13.

5.2.1 Receiver Jitter Tolerance Testing

Receiver jitter tolerance meets the template shown in Figure 6, when operated at line losses from 0 to 36 dB. Figure 8 shows the setup used for jitter tolerance testing.

5.2.2 Receiver Jitter Transfer Testing

Receiver jitter transfer meets the template shown in Figure 7, when operated with line losses from 0 to 36 dB and input jitter amplitude of 0.15 UI peak-to-peak. Jitter gain at a given frequency is defined as the difference between intrinsic jitter and additive jitter at the measurement frequency, divided by the amplitude of the input jitter. Figure 9 shows the setup used for jitter transfer testing.

Figure 6. Receiver Jitter Tolerance Template

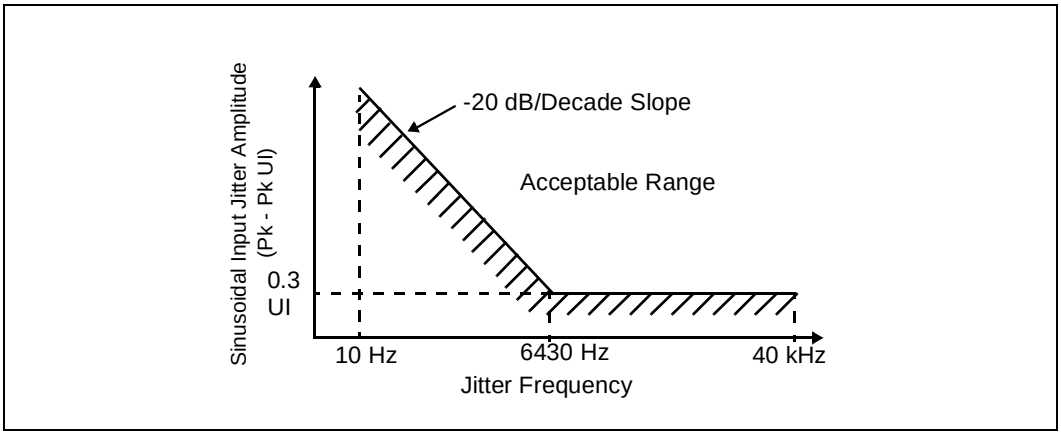


Figure 7. Receiver Jitter Transfer Template

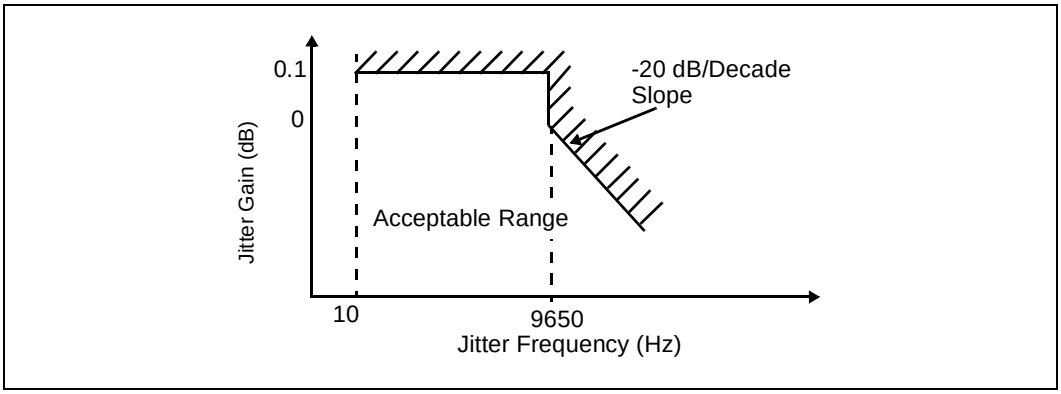


Figure 8. Receiver Jitter Tolerance Test Setup

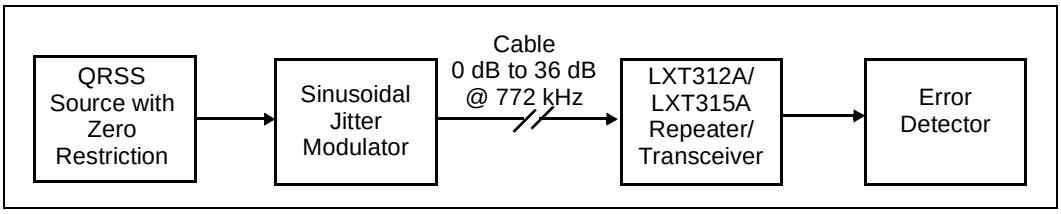
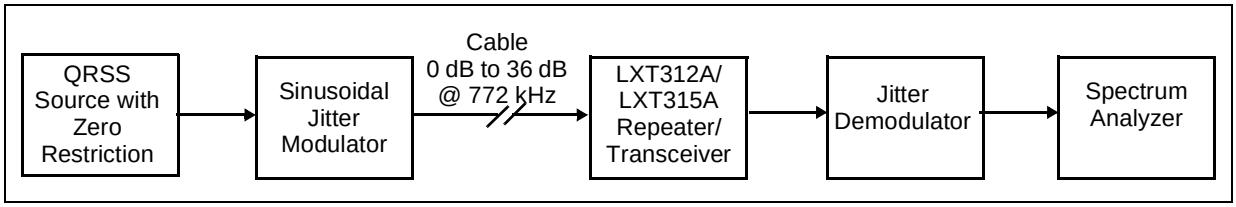


Figure 9. Receiver Jitter Transfer Test Setup



5.2.3 Interference Margin Testing

The LXT312A and LXT315A receiver noise interference margin is specified at a minimum of -11 dB for line losses from 0 dB to 36 dB. The test setup used to measure noise margin is shown in Figure 10.

5.2.4 Gaussian Noise Immunity Testing

Receiver immunity to Gaussian noise is specified at a maximum BER of 10^{-7} for a quasi-random T1 signal at 1.544 MHz (±130 ppm). The receiver must be immune to noise power expressed as Np = -(L + 4.7) dBm, where L corresponds to the line loss and is valid for 0 to 36 dB.

Figure 11 shows the setup used to test Gaussian noise immunity. The noise source is Gaussian to at least 6 sigma and filtered to simulate expected noise in a binder group (per AT&T TA #24/CB113).

5.2.5 60 Hz Pulse Modulation Immunity Testing

Receiver immunity to 60 Hz pulse amplitude modulation is specified using the Gaussian noise source described in the previous paragraph on Gaussian noise immunity. Pulse amplitude modulation is specified between 10% and 30% of the nominal amplitude (see AT&T TA #24/ CB113 for details on the modulation envelope). Figure 12 shows the setup used for testing receiver immunity to 60 Hz pulse amplitude modulation. The following data reflect noise power for 10^{-7} BER at each modulation level, where L corresponds to the line loss and is valid for 0 to 36 dB:

Modulation Level	Noise Power
10%	Np = -(L + 5.7) dBm
20%	Np = -(L + 6.7) dBm
30%	Np = -(L + 8.7) dBm

5.2.6 Receiver Timing Recovery Testing

Receiver timing recovery phase shift modulation for repetitive 8-bit patterns is specified at less than 0.07 UI. This is tested using any two out of 35 possible 8-bit patterns and measuring the change in output pulse timing from one pattern to the other (see AT&T TA #24/CB113 for details on patterns). The switching rate from one pattern to the other is specified at between 300 Hz and 500 Hz. See Figure 13 for the setup used to test receiver timing recovery phase shift modulation.

Figure 10. Receiver Noise Interference Margin Test Setup

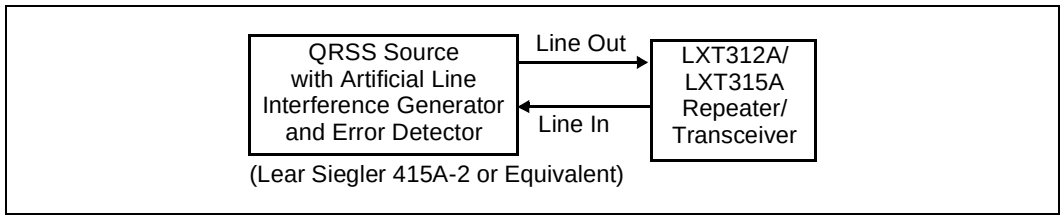


Figure 11. Receiver Gaussian Noise Immunity Test Setup

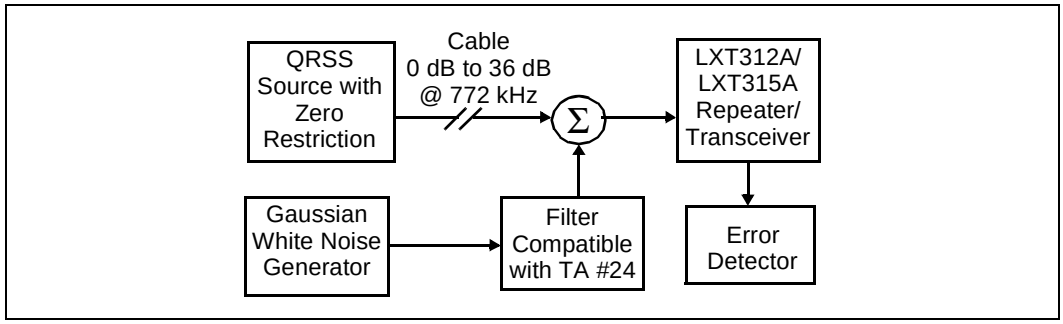


Figure 12. Receiver 60 Hz Pulse Amplitude Modulation Immunity Test Setup

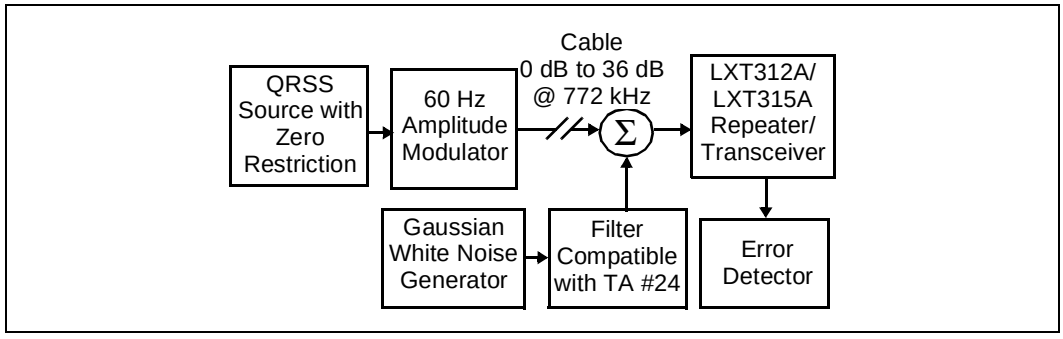
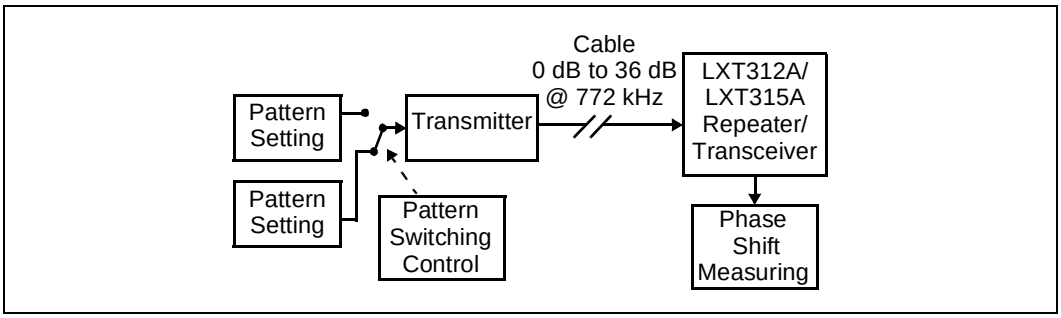


Figure 13. Receiver Timing Recovery Phase Shift Modulation Test Setup

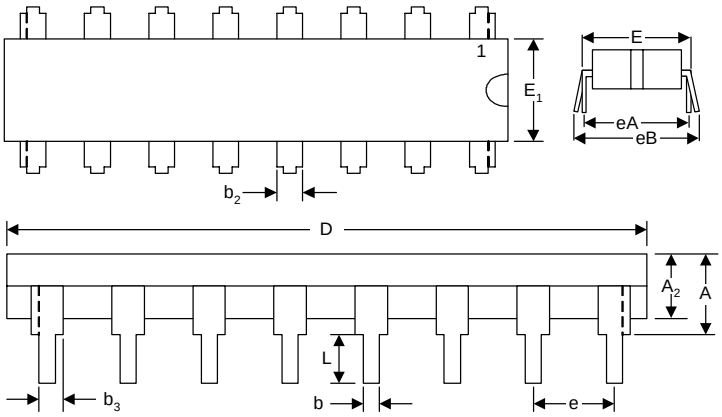


6.0 Mechanical Specifications

Figure 14. LXT312A / LXT315A Package Specifications

16-Pin Plastic Dual In-Line Package

- Part Number LXT312A and LXT315A
- Extended Temperature Range (-40 °C to +85 °C)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.210	–	5.334
A2	0.115	0.195	2.921	4.953
b	0.014	0.022	0.356	0.559
b2	0.045	0.070	1.143	1.778
b3	0.030	0.045	0.762	1.143
D	0.735	0.775	18.669	19.685
E	0.300	0.325	7.620	8.255
E1	0.240	0.280	6.096	7.112
e	0.100 BSC (Nominal)		2.540 BSC (Nominal)	
eA	0.300 BSC (Nominal)		7.620 BSC (Nominal)	
eB	–	0.430	–	10.922
L	0.115	0.150	2.921	3.810
1. BSC: Basic Spacing between Centers				

6.1 Top Label Markings

Figure 15 shows a sample PDIP non-RoHS package for the LXT312A Transceiver.

Notes:

1. In contrast to the Pb-Free (RoHS-compliant) PDIP package, the non-RoHS-compliant package does not have the “e3” symbol in the last line of the package label.
2. Further information regarding RoHS and lead-free components can be obtained from your local Intel representative.
   For general information, see http://www.intel.com/technology/silicon/leadfree.htm.

Figure 15. Sample PDIP Non-RoHS Package - Intel® PDLXT312ANE Transceiver

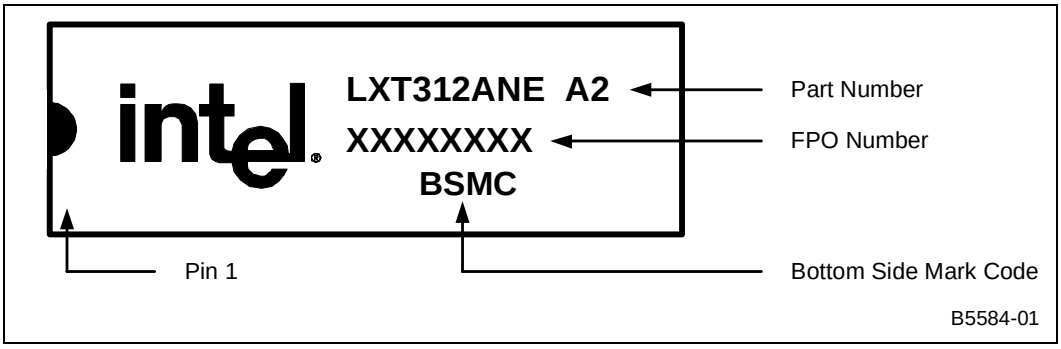


Figure 16 shows a sample Pb-Free (RoHS-compliant) PDIP package for the LXT312A Transceiver.

Figure 16. Sample PDIP RoHS Package - Intel® UCLXT312ANE Transceiver

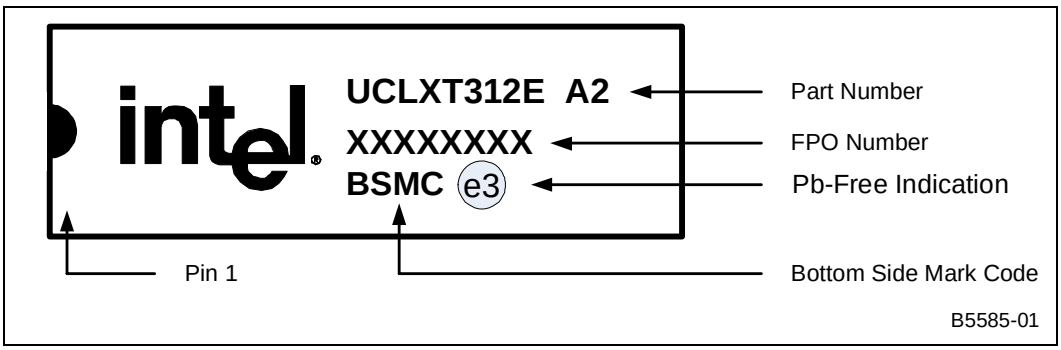


Figure 17 shows a sample PDIP non-RoHS package for the LXT315A Transceiver.

Note: In contrast to the Pb-Free (RoHS-compliant) PDIP package, the non-RoHS-compliant package does not have the “e3” symbol in the last line of the package label. .

Figure 17. Sample PDIP Non-RoHS Package - Intel® PDLXT315ANE Transceiver

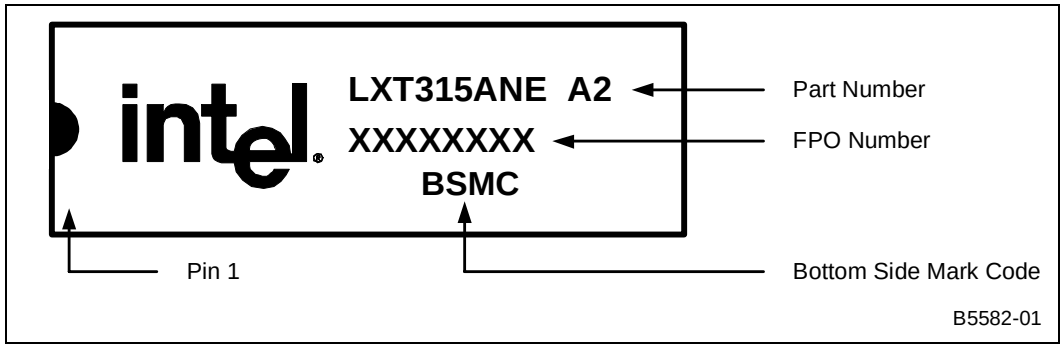
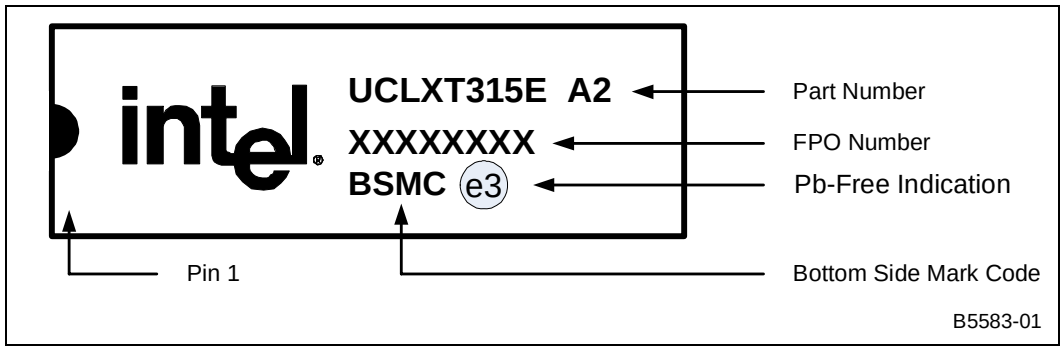


Figure 18 shows a sample PDIP RoHS package for the LXT315A Transceiver.

Figure 18. Sample PDIP RoHS Package - Intel® UCLXT315ANE Transceiver



7.0 Product Ordering Information

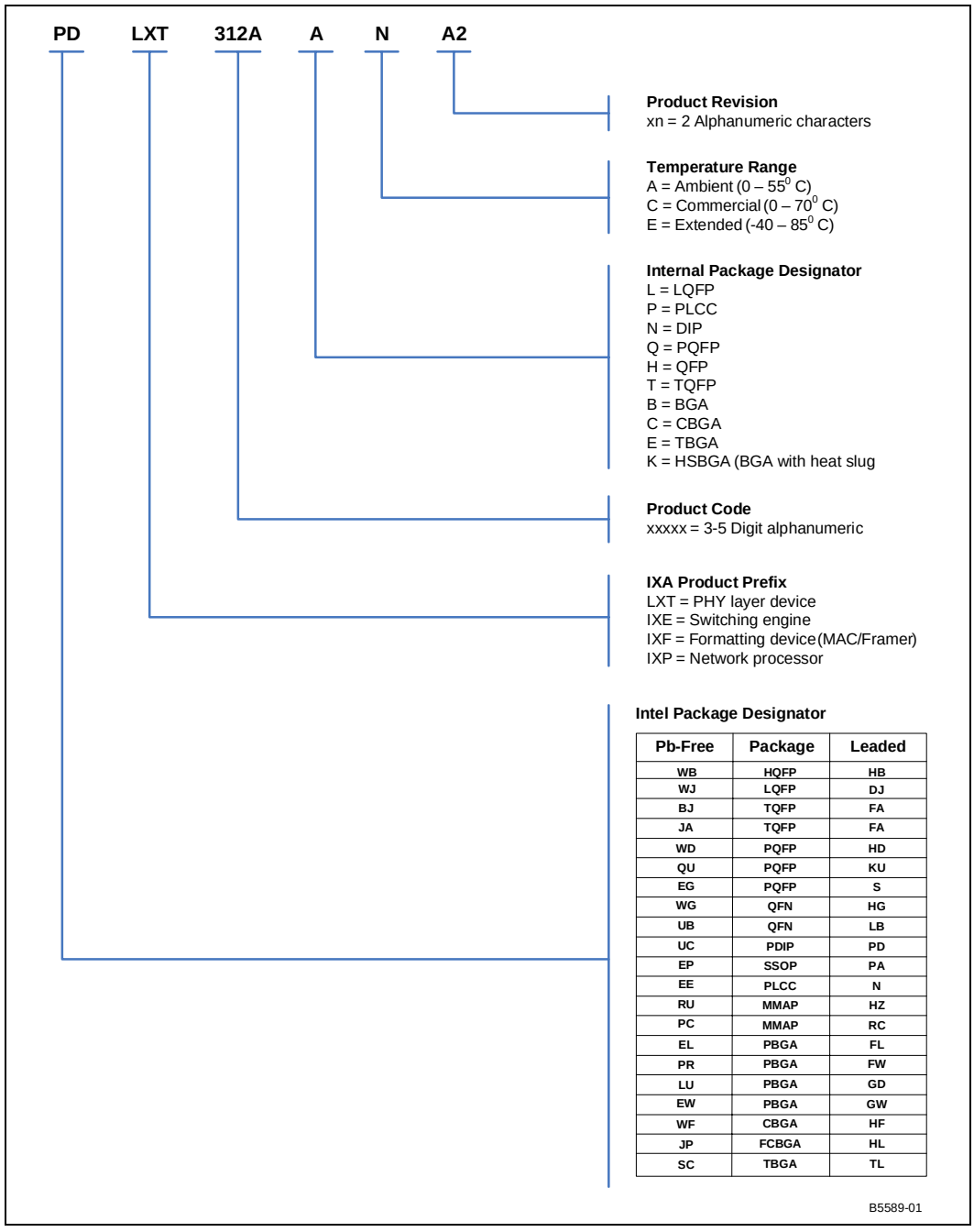
Table 8 lists product ordering information for the LXT312A/LXT315A Transceivers.

Table 8. Product Ordering Information

Product Number	Revision	Package Type	Pin Count	RoHS Compliant	Figure
PDLXT312ANE.A2	A2	PDIP	16	No	Figure 15, “Sample PDIP Non-RoHS Package - Intel® PDLXT312ANE Transceiver”
UCLXT312ANE.A2	A2	PDIP	16	Yes	Figure 16, “Sample PDIP RoHS Package - Intel® UCLXT312ANE Transceiver”
PDLXT315ANE.A2	A2	PDIP	16	No	Figure 17, “Sample PDIP Non-RoHS Package - Intel® PDLXT315ANE Transceiver”
UCLXT315ANE.A2	A2	PDIP	16	Yes	Figure 18, “Sample PDIP RoHS Package - Intel® UCLXT315ANE Transceiver”

Figure 19 shows an order matrix with sample information on how to order a LXT312A/LXT315A product.

Figure 19. Ordering Information Matrix – Sample



Pb-Free	Package	Leaded
WB	HQFP	HB
WJ	LQFP	DJ
BJ	TQFP	FA
JA	TQFP	FA
WD	PQFP	HD
QU	PQFP	KU
EG	PQFP	S
WG	QFN	HG
UB	QFN	LB
UC	PDIP	PD
EP	SSOP	PA
EE	PLCC	N
RU	MMAP	HZ
PC	MMAP	RC
EL	PBGA	FL
PR	PBGA	FW
LU	PBGA	GD
EW	PBGA	GW
WF	CBGA	HF
JP	FCBGA	HL
SC	TBGA	TL

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