



Atmel ATmega88/168 Automotive

Appendix A - Atmel ATmega88/168 Automotive Specification at 150°C

DATASHEET

Description

This document contains information specific to devices operating at temperatures up to 150°C. Only deviations are covered in this appendix, all other information can be found in the complete Automotive datasheet. The complete Automotive datasheet can be found on www.atmel.com

1. Electrical Characteristics

1.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Test Conditions | Unit |
|--|----------------------|------|
| Operating Temperature | -55 to +150 | °C |
| Storage Temperature | -65 to +175 | °C |
| Voltage on any Pin except $\overline{\text{RESET}}$ with respect to Ground | -0.5 to $V_{CC}+0.5$ | V |
| Voltage on $\overline{\text{RESET}}$ with respect to Ground | -0.5 to +13.0 | V |
| Maximum Operating Voltage | 6.0 | V |
| DC Current per I/O Pin | 30 | mA |
| DC Current V_{CC} and GND | 200.0 | |

1.2 DC Characteristics

$T_A = -40^\circ\text{C}$ to $+150^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 5.5V (unless otherwise noted)

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|-----------|-------------------|------|--------------------|------|
| Input Low Voltage, except XTAL1 and $\overline{\text{RESET}}$ pin | $V_{CC} = 2.7\text{V}$ to 5.5V | V_{IL} | -0.5 | | $+0.3V_{CC}^{(1)}$ | V |
| Input High Voltage, except XTAL1 and $\overline{\text{RESET}}$ pins | $V_{CC} = 2.7\text{V}$ to 5.5V | V_{IH} | $0.6V_{CC}^{(2)}$ | | $V_{CC} + 0.5$ | V |
| Input Low Voltage, XTAL1 pin | $V_{CC} = 2.7\text{V}$ to 5.5V | V_{IL1} | -0.5 | | $+0.1V_{CC}^{(2)}$ | V |
| Input High Voltage, XTAL1 pin | $V_{CC} = 2.7\text{V}$ to 5.5V | V_{IH1} | $0.7V_{CC}^{(2)}$ | | $V_{CC} + 0.5$ | V |
| Input Low Voltage, $\overline{\text{RESET}}$ pin | $V_{CC} = 2.7\text{V}$ to 5.5V | V_{IL2} | -0.5 | | $+0.2V_{CC}^{(1)}$ | V |
| Input High Voltage, $\overline{\text{RESET}}$ pin | $V_{CC} = 2.7\text{V}$ to 5.5V | V_{IH2} | $0.9V_{CC}^{(2)}$ | | $V_{CC} + 0.5$ | V |

- Notes:
- “Max” means the highest value where the pin is guaranteed to be read as low
 - “Min” means the lowest value where the pin is guaranteed to be read as high
 - Although each I/O port can sink more than the test conditions (20mA at $V_{CC} = 5\text{V}$) under steady state conditions (non-transient), the following must be observed:
 - The sum of all IOL, for all ports, should not exceed 400mA.
 - The sum of all IOL, for ports C0 - C5, should not exceed 200mA.
 - The sum of all IOL, for ports C6, D0 - D4, should not exceed 300mA.
 - The sum of all IOL, for ports B0 - B7, D5 - D7, should not exceed 300mA.
 If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
 - Although each I/O port can source more than the test conditions (20mA at $V_{CC} = 5\text{V}$) under steady state conditions (non-transient), the following must be observed:
 - The sum of all IOH, for all ports, should not exceed 400mA.
 - The sum of all IOH, for ports C0 - C5, should not exceed 200mA.
 - The sum of all IOH, for ports C6, D0 - D4, should not exceed 300mA.
 - The sum of all IOH, for ports B0 - B7, D5 - D7, should not exceed 300mA.
 If IOH exceeds the test condition, VOH may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
 - Minimum V_{CC} for Power-down is 2.5V

1.2 DC Characteristics (Continued)

$T_A = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 5.5V (unless otherwise noted)

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|--|----------------------|-------------------|------|--------------------|------------------|
| Input Low Voltage, RESET pin as I/O | $V_{CC} = 2.7\text{V}$ to 5.5V | V_{IL3} | -0.5 | | $+0.3V_{CC}^{(1)}$ | V |
| Input High Voltage, RESET pin as I/O | $V_{CC} = 2.7\text{V}$ to 5.5V | V_{IH3} | $0.6V_{CC}^{(2)}$ | | $V_{CC} + 0.5$ | V |
| Output Low Voltage ⁽³⁾ , I/O pin except RESET | $I_{OL} = 20\text{mA}$, $V_{CC} = 5\text{V}$ $I_{OL} = 5\text{mA}$, $V_{CC} = 3\text{V}$ | V_{OL} | | | 0.8 0.5 | V |
| Output High Voltage ⁽⁴⁾ I/O pin except RESET | $I_{OH} = -20\text{mA}$, $V_{CC} = 5\text{V}$ $I_{OH} = -10\text{mA}$, $V_{CC} = 3\text{V}$ | V_{OH} | 4.0 2.2 | | | V |
| Input Leakage Current I/O Pin | $V_{CC} = 5.5\text{V}$, pin low (absolute value) | I_{IL} | | | 1 | μA |
| Input Leakage Current I/O Pin | $V_{CC} = 5.5\text{V}$, pin high (absolute value) | I_{IH} | | | 1 | μA |
| Reset Pull-up Resistor | | R_{RST} | 30 | | 60 | $\text{k}\Omega$ |
| I/O Pin Pull-up Resistor | | R_{PU} | 20 | | 50 | $\text{k}\Omega$ |
| Power Supply Current ⁽⁵⁾ | Active 4MHz, $V_{CC} = 3\text{V}$ Active 8MHz, $V_{CC} = 5\text{V}$ | I_{CC} | | | 8 16 | mA |
| | Active 16MHz, $V_{CC} = 5\text{V}$ | | | | 25 | mA |
| | Idle 4MHz, $V_{CC} = 3\text{V}$ Idle 8MHz, $V_{CC} = 5\text{V}$ | $I_{CC\text{ IDLE}}$ | | | 6 12 | mA |
| | Idle 16MHz, $V_{CC} = 5\text{V}$ | | | | 14 | mA |
| Power-down mode | WDT enabled, $V_{CC} = 3\text{V}$ WDT enabled, $V_{CC} = 5\text{V}$ | $I_{CC\text{ PWD}}$ | | | 90 140 | μA |
| | WDT disabled, $V_{CC} = 3\text{V}$ WDT disabled, $V_{CC} = 5\text{V}$ | | | | 80 120 | μA |
| Analog Comparator Input Offset Voltage | $V_{CC} = 5\text{V}$ $V_{in} = V_{CC}/2$ | V_{ACIO} | | < 10 | 40 | mV |
| Analog Comparator Input Leakage Current | $V_{CC} = 5\text{V}$ $V_{in} = V_{CC}/2$ | I_{ACLK} | -50 | | +50 | nA |
| Analog Comparator Propagation Delay | $V_{CC} = 4.0\text{V}$ | t_{ACPD} | | 500 | | ns |

- Notes:
1. "Max" means the highest value where the pin is guaranteed to be read as low
 2. "Min" means the lowest value where the pin is guaranteed to be read as high
 3. Although each I/O port can sink more than the test conditions (20mA at $V_{CC} = 5\text{V}$) under steady state conditions (non-transient), the following must be observed:
 - 1] The sum of all IOL, for all ports, should not exceed 400mA.
 - 2] The sum of all IOL, for ports C0 - C5, should not exceed 200mA.
 - 3] The sum of all IOL, for ports C6, D0 - D4, should not exceed 300mA.
 - 4] The sum of all IOL, for ports B0 - B7, D5 - D7, should not exceed 300mA.
 If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
 4. Although each I/O port can source more than the test conditions (20mA at $V_{CC} = 5\text{V}$) under steady state conditions (non-transient), the following must be observed:
 - 1] The sum of all IOH, for all ports, should not exceed 400mA.
 - 2] The sum of all IOH, for ports C0 - C5, should not exceed 200mA.
 - 3] The sum of all IOH, for ports C6, D0 - D4, should not exceed 300mA.
 - 4] The sum of all IOH, for ports B0 - B7, D5 - D7, should not exceed 300mA.
 If IOH exceeds the test condition, VOH may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
 5. Minimum V_{CC} for Power-down is 2.5V

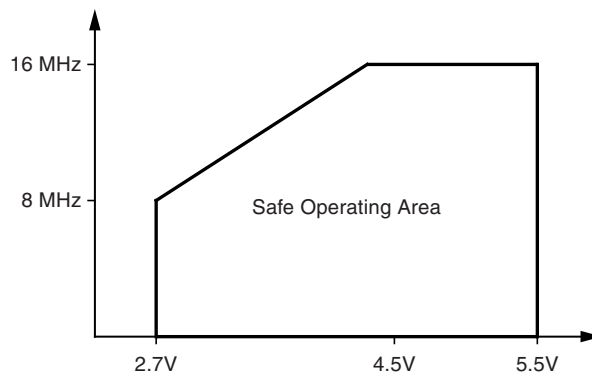
1.3 Memory Endurance

EEPROM endurance: 50,000 Write/Erase cycles.
Flash endurance: 10,000 Write/Erase cycles.

1.4 Maximum Speed versus V_{CC}

Maximum frequency is dependent on V_{CC} . As shown in Figure 1-1, the Maximum Frequency vs. V_{CC} curve is linear between $2.7V < V_{CC} < 4.5V$.

Figure 1-1. Maximum Frequency vs. V_{CC}



1.5 ADC Characteristics⁽¹⁾

$T_A = -40^{\circ}C$ to $+150^{\circ}C$, $V_{CC} = 4.5V$ to $5.5V$ (unless otherwise noted)

| Parameters | Test Conditions | Symbol | Min | Typ | Max | Unit |
|--|--|-----------|----------------|------|----------------|------------|
| Resolution | | | | 10 | | Bits |
| Absolute accuracy (Including INL, DNL, quantization error, gain and offset error) | $V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200kHz | | | 2 | 3.5 | LSB |
| | $V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200kHz Noise Reduction Mode | | | 2 | 3.5 | LSB |
| Integral Non-Linearity (INL) | $V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200kHz | | | 0.6 | 2.5 | LSB |
| Differential Non-Linearity (DNL) | $V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200kHz | | | 0.30 | 1.0 | LSB |
| Gain Error | $V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200kHz | | -3.5 | -1.3 | +3.5 | LSB |
| Offset Error | $V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200kHz | | | 1.8 | 3.5 | LSB |
| Conversion Time | Free Running Conversion | | 13 cycles | | | μs |
| Clock Frequency | | | 50 | | 200 | kHz |
| Analog Supply Voltage | | AV_{CC} | $V_{CC} - 0.3$ | | $V_{CC} + 0.3$ | V |
| Reference Voltage | | V_{REF} | 1.0 | | AV_{CC} | V |
| Input Voltage | | V_{IN} | GND | | V_{REF} | V |
| Input Bandwidth | | | | 38.5 | | kHz |
| Internal Voltage Reference | | V_{INT} | 1.0 | 1.1 | 1.2 | V |
| Reference Input Resistance | | R_{REF} | 25.6 | 32 | 38.4 | k Ω |
| Analog Input Resistance | | R_{AIN} | | 100 | | M Ω |

Note: 1. Based on standard voltage range (2.7V to 5.5V) characterization results. To be confirmed after actual silicon characterization.

2. ATmega88/168 Typical Characteristics

2.1 Active Supply Current

Figure 2-1. Active Supply Current versus Frequency (1MHz to 20MHz)

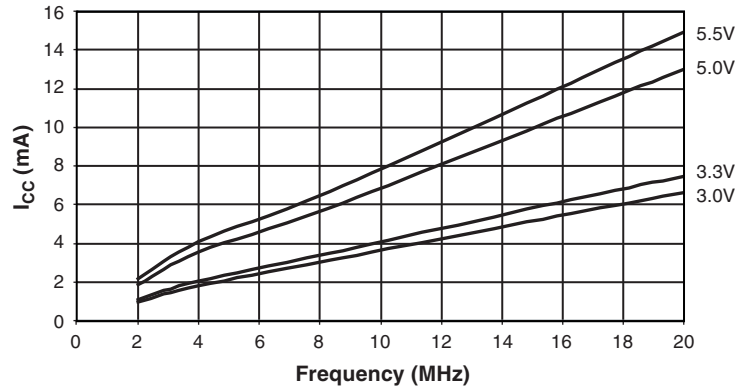
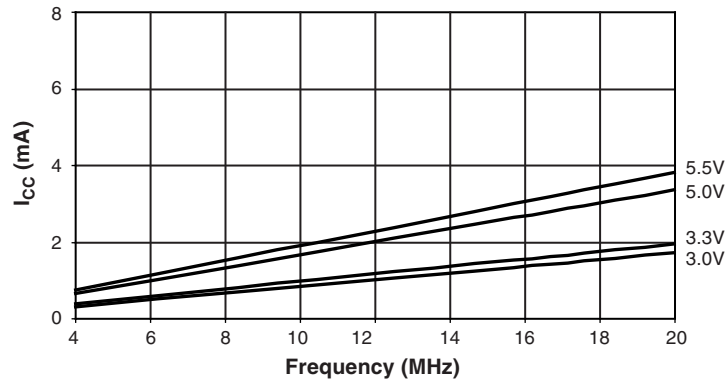


Figure 2-2. Idle Supply Current versus Frequency (1MHz to 20MHz)



2.2 Power-Down Supply Current

Figure 2-3. Power-down Supply Current versus V_{CC} (Watchdog Timer Disabled)

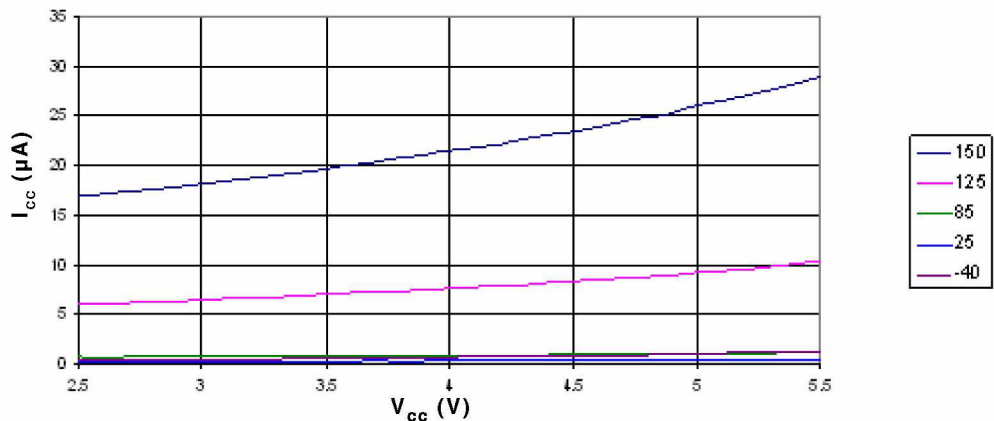
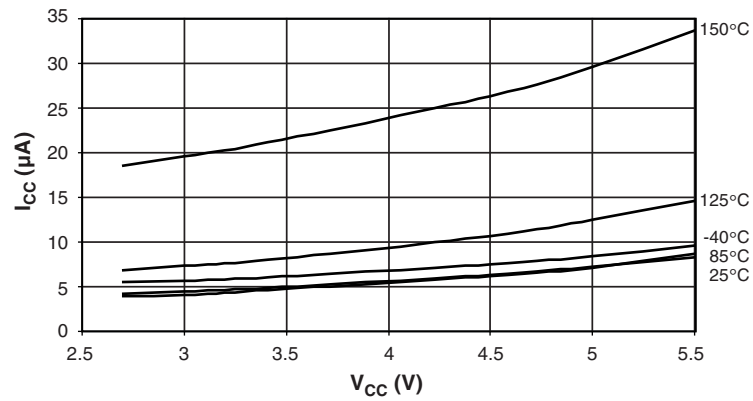


Figure 2-4. Power-down Supply Current versus V_{CC} (Watchdog Timer Enabled)



2.3 Pin Pull-up

Figure 2-5. I/O Pin Pull-up Resistor Current versus Input Voltage ($V_{CC} = 5V$)

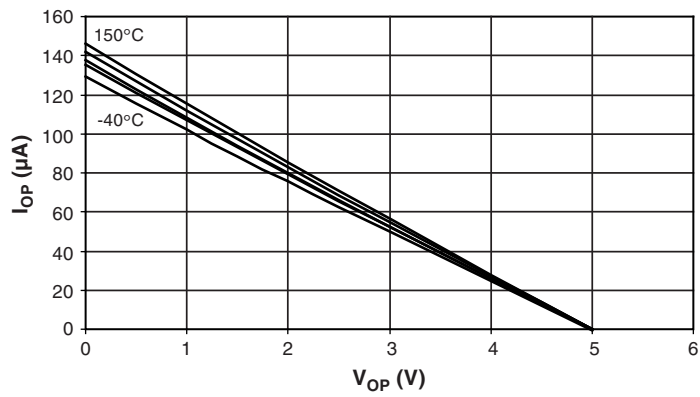


Figure 2-6. Output Low Voltage versus Output Low Current ($V_{CC} = 5V$)

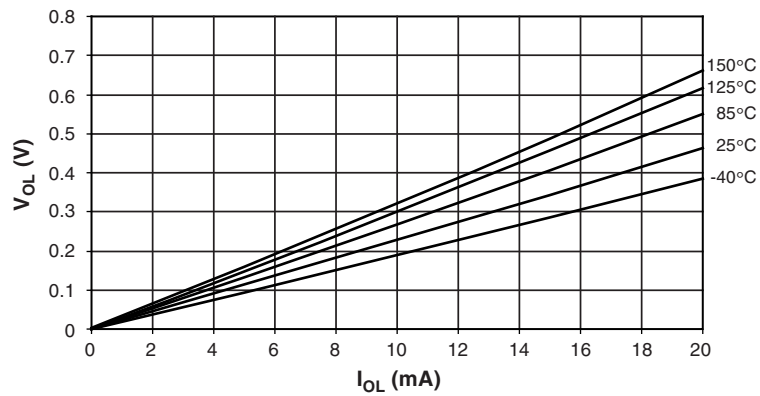


Figure 2-7. Output Low Voltage versus Output Low Current ($V_{CC} = 3V$)

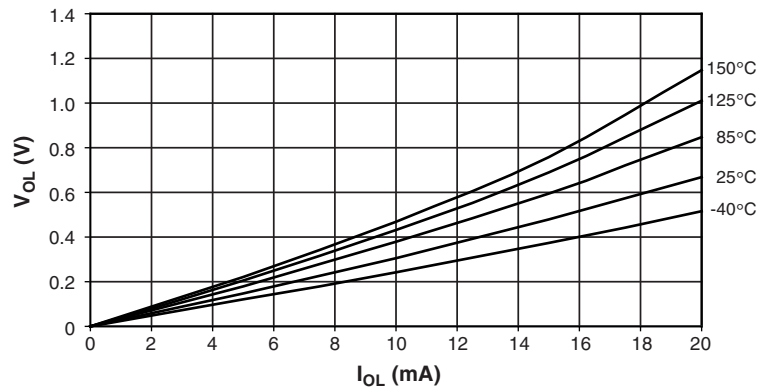


Figure 2-8. Output High Voltage versus Output High Current ($V_{CC} = 5V$)

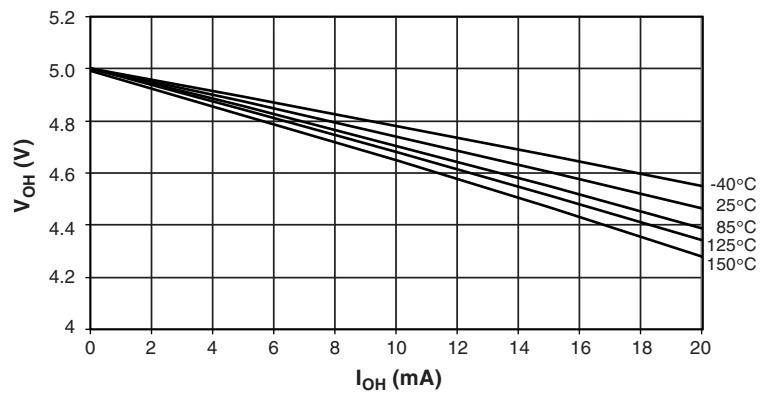


Figure 2-9. Output High Voltage versus Output High Current ($V_{CC} = 3V$)

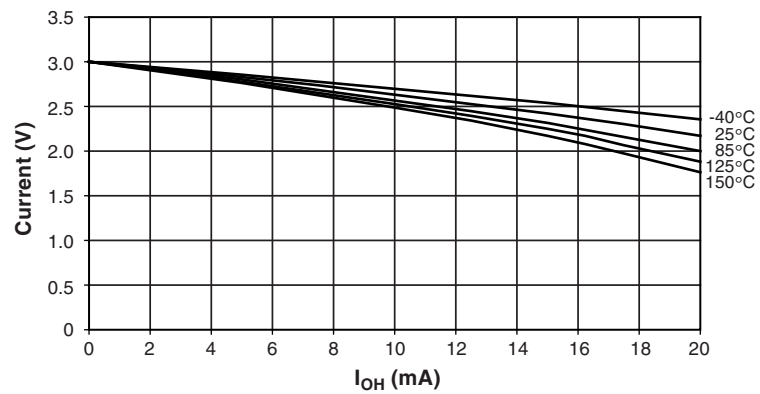
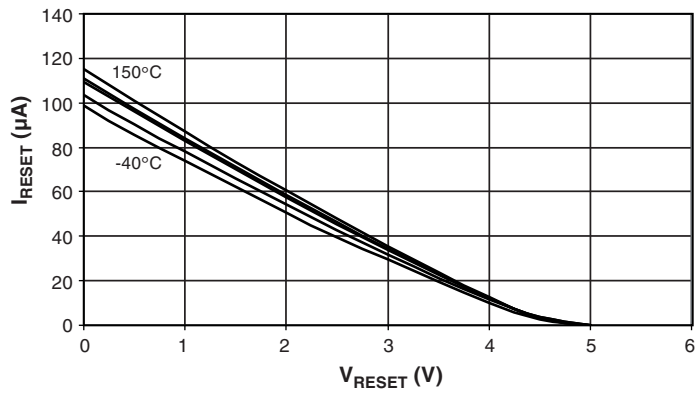


Figure 2-10. Reset Pull-up Resistor Current versus Reset Pin Voltage ($V_{CC} = 5V$)



2.4 Pin Thresholds and Hysteresis

Figure 2-11. I/O Pin Input Threshold versus V_{CC} (V_{IH} , I/O Pin Read as '1')

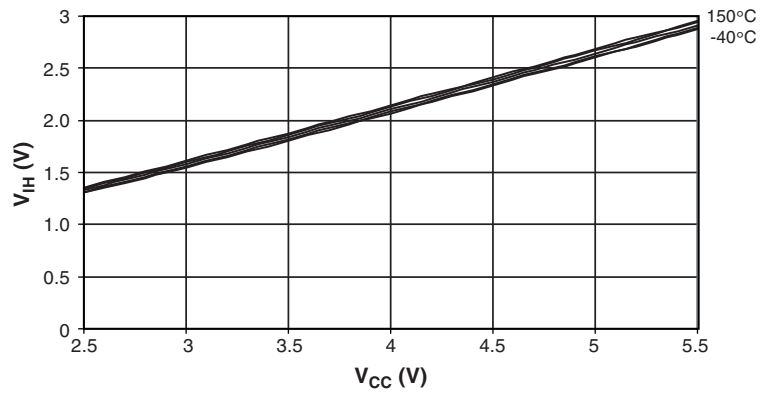


Figure 2-12. I/O Pin Input Threshold versus V_{CC} (V_{IL} , I/O Pin Read as '0')

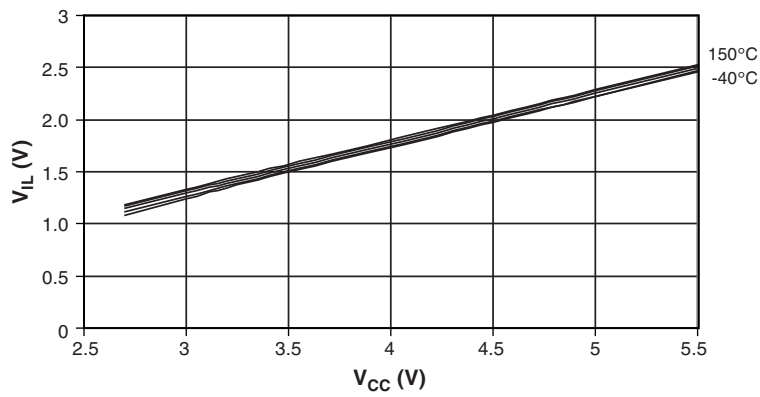


Figure 2-13. Reset Input Threshold Voltage versus V_{CC} (V_{IH} , Reset Pin Read as '1')

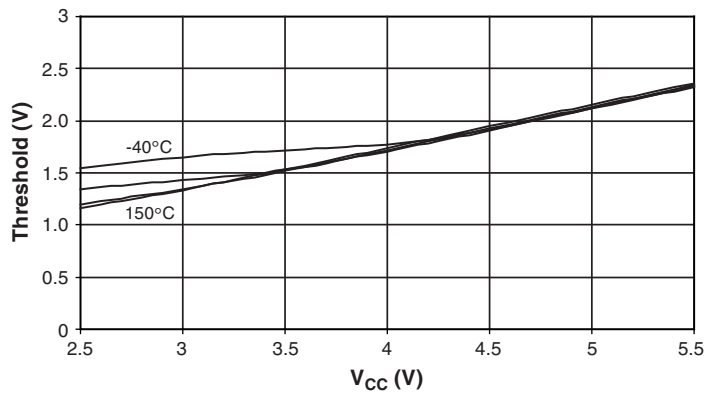
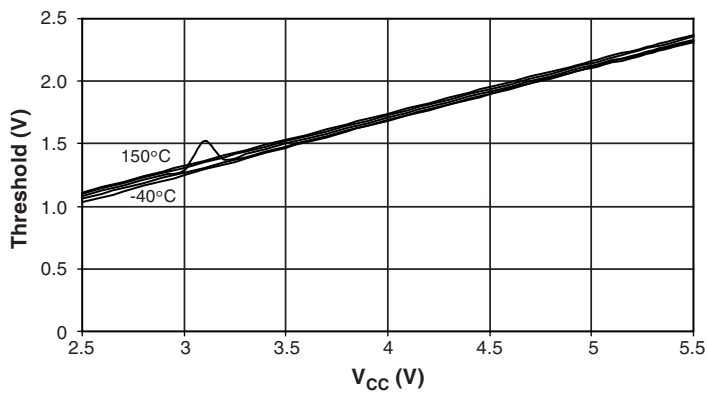


Figure 2-14. Reset Input Threshold Voltage versus V_{CC} (V_{IL} , Reset Pin Read as '0')



2.5 Internal Oscillator Speed

Figure 2-15. Watchdog Oscillator Frequency versus V_{CC}

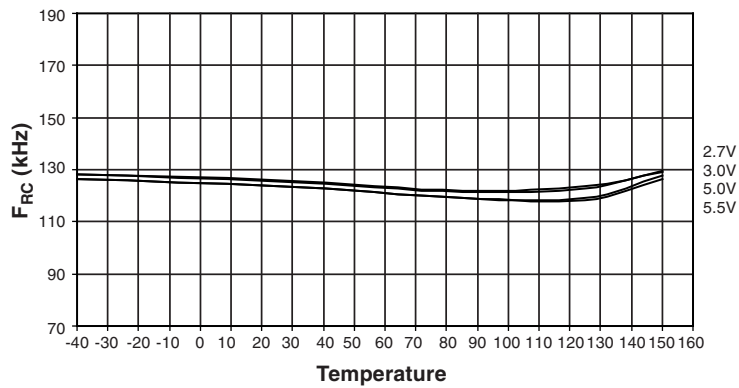


Figure 2-16. Calibrated 8MHz RC Oscillator Frequency versus Temperature

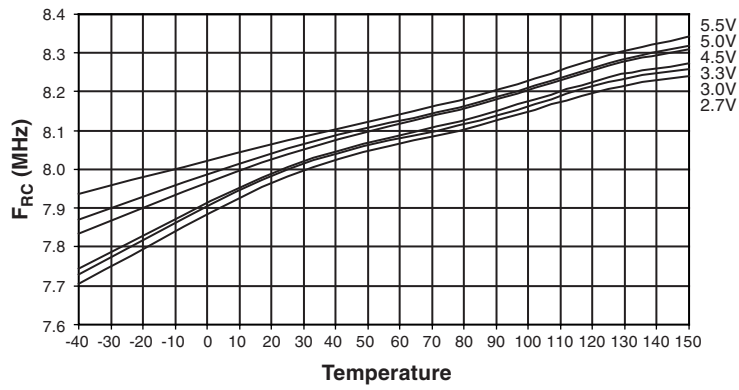


Figure 2-17. Calibrated 8MHz RC Oscillator Frequency versus V_{CC}

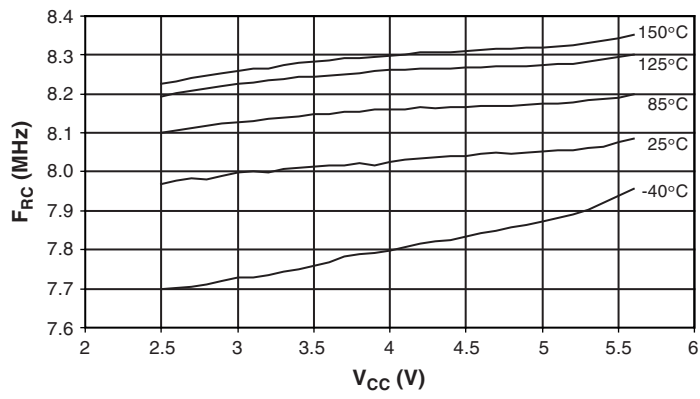
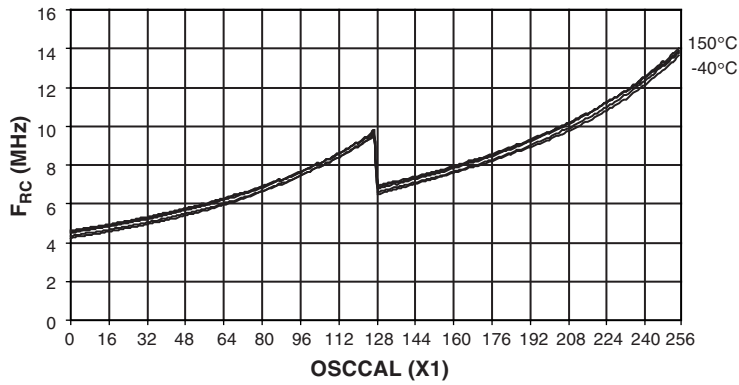


Figure 2-18. Calibrated 8MHz RC Oscillator Frequency versus OSCCAL Value



2.6 BOD Thresholds and Analog Comparator Offset

Figure 2-19. BOD Threshold versus Temperature (BODLEVEL is 4.0V)

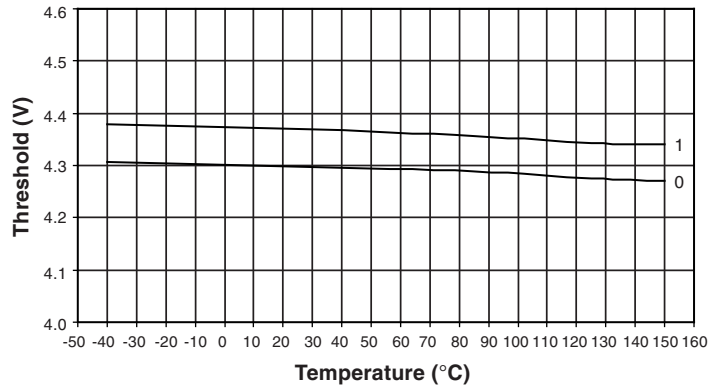


Figure 2-20. BOD Threshold versus Temperature (BODLEVEL is 2.7V)

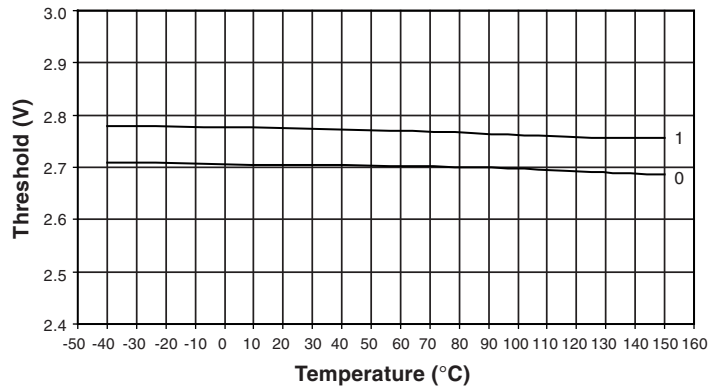
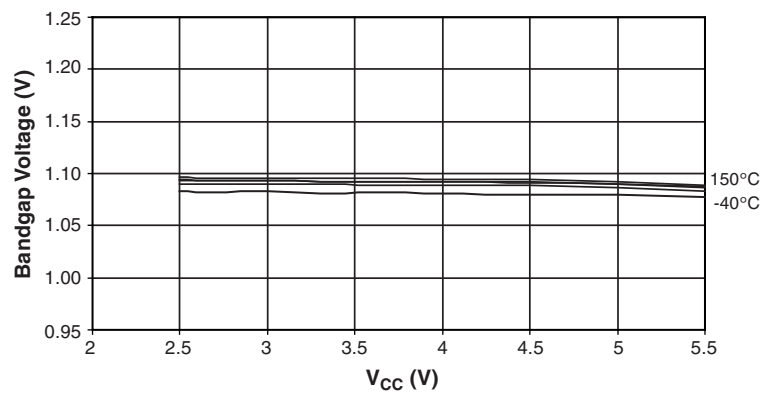


Figure 2-21. Bandgap Voltage versus V_{CC}



2.7 Peripheral Units

Figure 2-22. Analog to Digital Converter GAIN versus V_{CC}

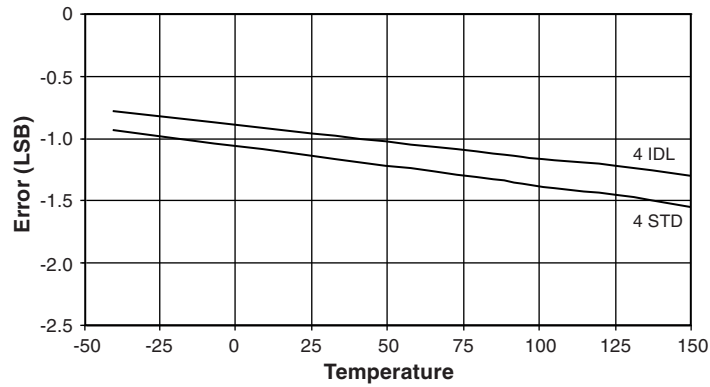


Figure 2-23. Analog to Digital Converter OFFSET versus V_{CC}

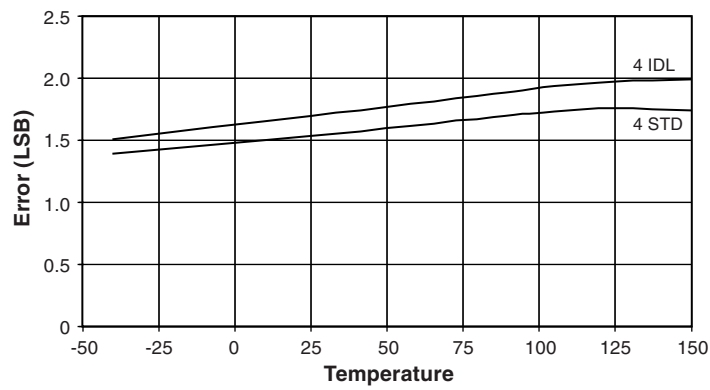


Figure 2-24. Analog to Digital Converter DNL versus V_{CC}

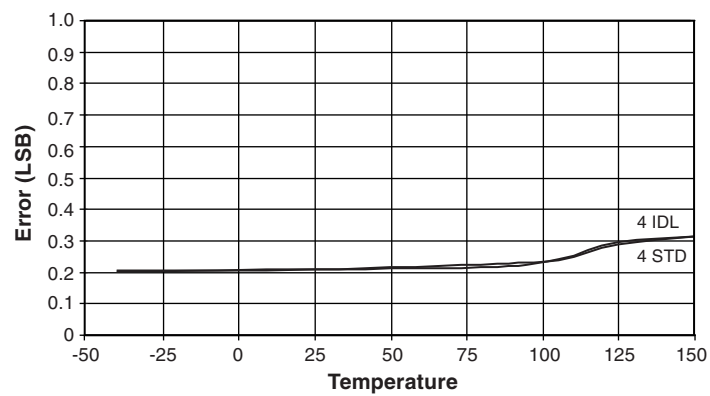
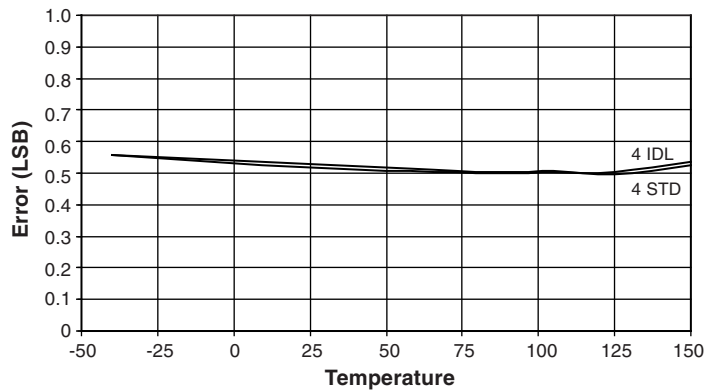


Figure 2-25. Analog to Digital Converter INL versus V_{CC}



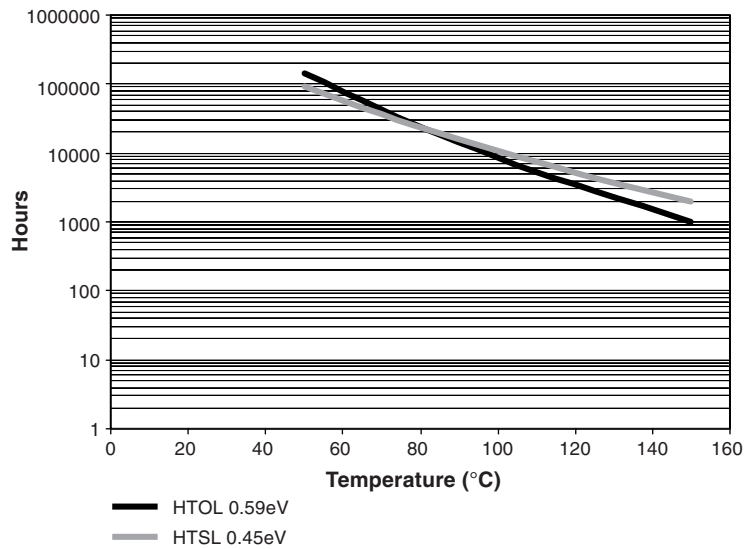
2.8 Grade 0 Qualification

The ATmega88/168 has been developed and manufactured according to the most stringent quality assurance requirements of ISO-TS-16949 and verified during product qualification as per AEC-Q100 grade 0.

AEC-Q100 qualification relies on temperature accelerated stress testing. High temperature field usage however may result in less significant stress test acceleration. In order to prevent the risk that ATmega88/168 lifetime would not satisfy the application end-of-life reliability requirements, Atmel® has extended the testing, whenever applicable (High Temperature Operating Life Test, High Temperature Storage Life, Data Retention, Thermal Cycles), far beyond the AEC-Q100 requirements. Thereby, Atmel verified the ATmega88/168 has a long safe lifetime period after the grade 0 qualification acceptance limits.

The valid domain calculation depends on the activation energy of the potential failure mechanism that is considered. Examples are given in Figure 2-26. Therefore any temperature mission profile which could exceed the AEC-Q100 equivalence domain shall be submitted to Atmel for a thorough reliability analysis

Figure 2-26. AEC-Q100 Lifetime Equivalence



3. Ordering Information

Table 3-1. ATmega88/168

| Speed (MHz) | Power Supply | Ordering Code | Package ⁽¹⁾ | Operation Range |
|-------------------|--------------|----------------|------------------------|----------------------------|
| 16 ⁽²⁾ | 2.7V to 5.5V | ATmega88-15MT2 | PN | Extended (–40°C to +150°C) |
| 16 ⁽²⁾ | 2.7V to 5.5V | ATmega88-15AD | MA | Extended (–40°C to +150°C) |
| 16 ⁽²⁾ | 2.7V to 5.5V | ATmega168-15MD | PN | Extended (–40°C to +150°C) |
| 16 ⁽²⁾ | 2.7V to 5.5V | ATmega168-15AD | MA | Extended (–40°C to +150°C) |

- Notes:
1. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 2. For Speed vs. V_{CC} , see complete datasheet.

4. Package Information

Table 4-1. Package Types

| Package Type | |
|--------------|---|
| PN | 32-pad, 5 × 5 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF): E2/D2 3.1 ±0.1mm |
| MA | 32 - Lead, 7mm × 7mm Body Size, 1.0mm Body Thickness 0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) |

Figure 4-1. PN

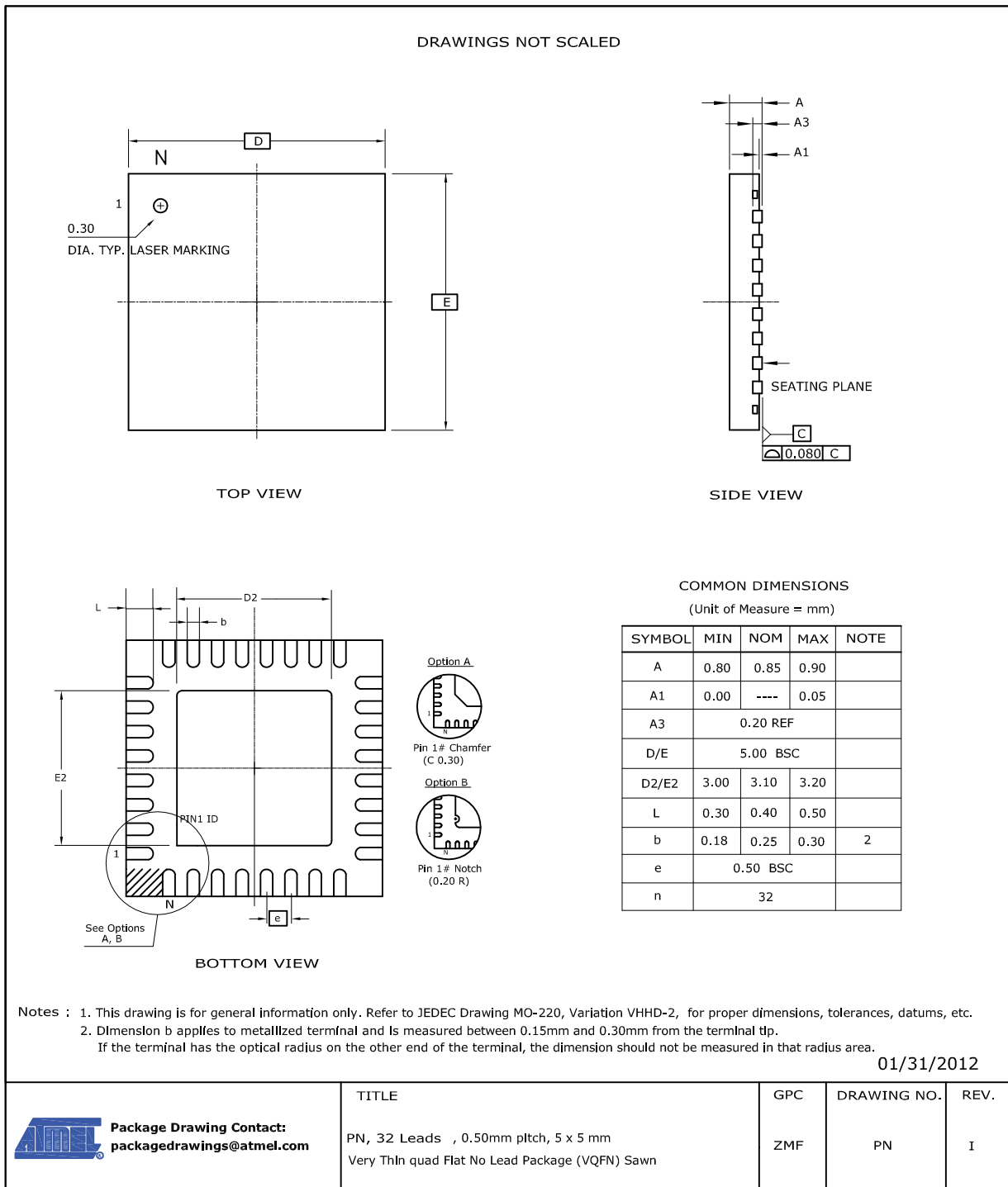
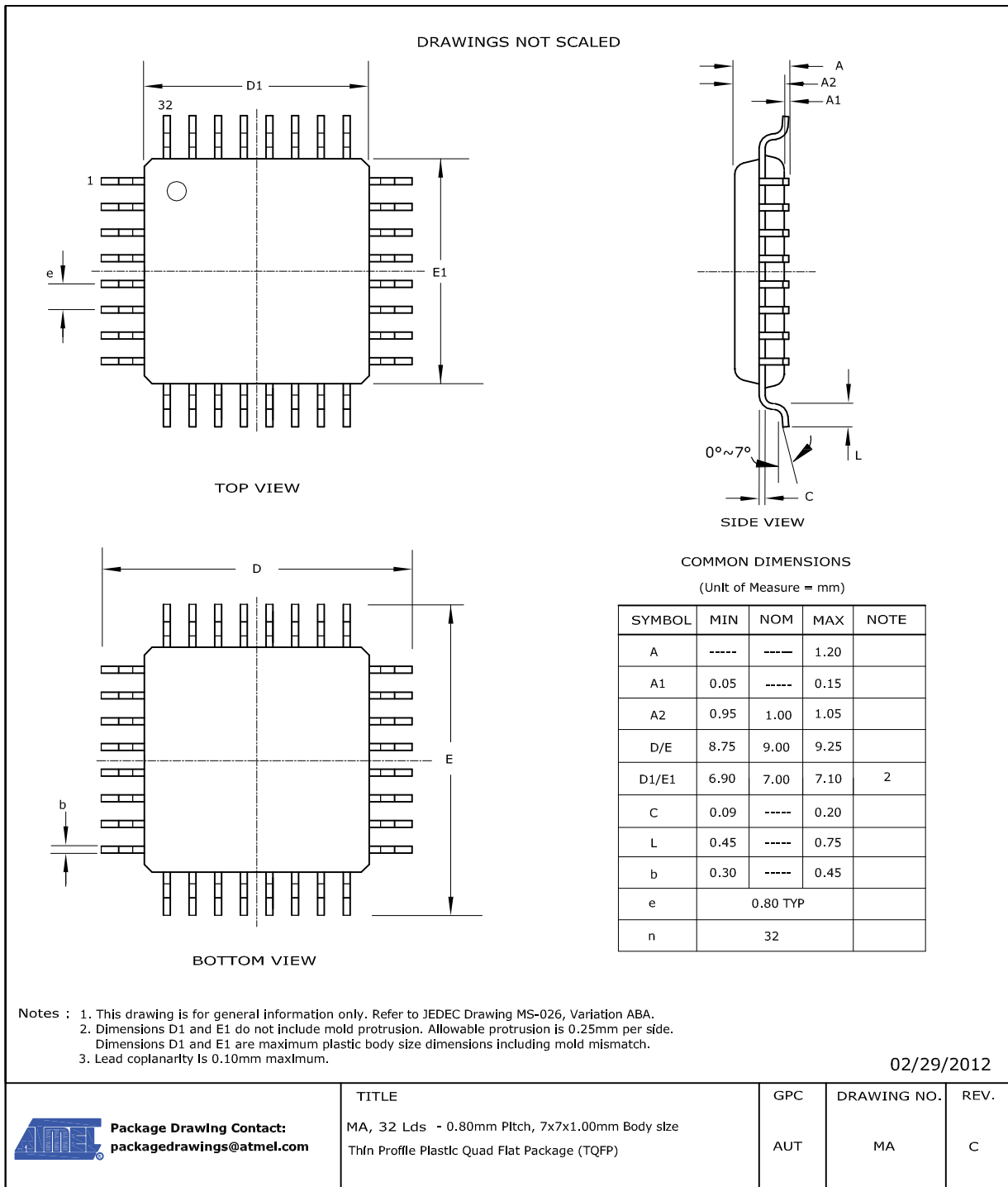


Figure 4-2. MA



5. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|-----------------|---|
| 7607I-AVR-03/12 | <ul style="list-style-type: none">• Section 4 “Package Information” on pages 15 to 16 changed |
| 7607H-AVR-02/10 | <ul style="list-style-type: none">• Table 4-1 “Package Types” on page 15 changed |
| 7607G-AVR-07/09 | <ul style="list-style-type: none">• Package MA updated |
| 7607F-AVR-01/08 | <ul style="list-style-type: none">• Added memory endurance. See Section 1.3 “Memory Endurance” on page 4 |
| 7607E-AVR-11/07 | <ul style="list-style-type: none">• Added ATmega168 product offering• Added MA package offering |
| 7607D-AVR-03/07 | <ul style="list-style-type: none">• Updated electrical characteristics• Removed Grade0 qualification section• Updated product part number in ordering information |
| 7607C-AVR-09/06 | <ul style="list-style-type: none">• Ordering and package information updated |
| 7607B-AVR-08/06 | <ul style="list-style-type: none">• Added typical characteristics |
| 7607A-AVR-01/06 | <ul style="list-style-type: none">• Document Creation |



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