

MPC5748G

MPC5748G Microcontroller Data Sheet

Features

- 2 x 160 MHz Power Architecture® e200Z4 Dual issue, 32-bit CPU
 - Single precision floating point operations
 - 8 KB instruction cache and 4 KB data cache
 - Variable length encoding (VLE) for significant code density improvements
- 1 x 80 MHz Power Architecture® e200Z2 Single issue, 32-bit CPU
 - Using variable length encoding (VLE) for significant code size footprint reduction
- End to end ECC
 - All bus masters, for example, cores generate single error correction, double error detection (SECDED) code for every bus transaction
 - SECDED covers 64-bit data and 29-bit address
- Memory interfaces
 - 6 MB on-chip flash supported with the flash controller
 - 3 x flash page buffers (3 port flash controller)
 - 768 KB on-chip SRAM across three RAM ports
- Clock interfaces
 - 8-40 MHz external crystal (FXOSC)
 - 16 MHz IRC (FIRC)
 - 128 KHz IRC (SIRC)
 - 32 KHz external crystal (SXOSC)
 - Clock Monitor Unit (CMU)
 - Frequency modulated phase-locked loop (FMPLL)
 - Real Time Counter (RTC)
- System Memory Protection Unit (SMPU) with up to 32 region descriptors and 16-byte region granularity
- 16 Semaphores to manage access to shared resource
- Interrupt controller (INTC) capable of routing interrupts to any CPU
- Multiple crossbar switch architecture for concurrent access to peripherals, flash, and RAM from multiple bus masters
- 32-channels eDMA controller with multiple transfer request sources using DMAMUX
- Boot Assist Flash (BAF) supports internal flash programming via a serial link (LIN / SCI)
- Analog
 - Two analog-to-digital converters (ADC), one 10-bit and one 12-bit
 - Three analogue comparators
 - Cross Trigger Unit to enable synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
- Communication
 - Four Deserial Peripheral Interface (DSPI)
 - Six Serial Peripheral interface (SPI)
 - 18 serial communication interface (LIN) modules
 - Eight enhanced FlexCAN3 with FD support
 - Four inter-IC communication interface (IIC)
 - One USB OTG Controller (USB_0) and One USB SPH Controller (USB_1) with ULPI Interface.
 - ENET complex (10/100 Ethernet) that supports Multi queue with AVB support, 1588, and MII/RMII
 - 2 x ENET with L2 switch
 - Secure Digital Hardware Controller (uSDHC)
 - Dual-channel FlexRay Controller
- Audio
 - 3 x Synchronous Audio Interface (SAI)
 - Fractional clock dividers (FCD) operating in conjunction with the SAIs
- Configurable I/O domains supporting FLEXCAN, LINFlex, Ethernet, USB, MLB, uSDHC and general I/O
- Supports wake-up from low power modes via the WKPU controller
- On-chip voltage regulator (VREG)
- Debug functionality
 - e200Z2 core: NDI per IEEE-ISTO 5001-2008 Class3+
 - e200Z4 core(s): NDI per IEEE-ISTO 5001-2008 Class 3+



- Timer
 - 16 Periodic Interrupt Timers (PITs)
 - Three System Timer Module (STM)
 - Four Software WatchDog Timers (SWT)
 - 96 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1) and 1149.7 (cJTAG)
- Security
 - Hardware Security Module (HSMv2)
 - Password and Device Security (PASS and TDM) supporting advanced censorship and life-cycle management
 - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
 - ISO26262 ASIL compliance
- Multiple operating modes
 - Includes enhanced low power operation

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1 Block diagram

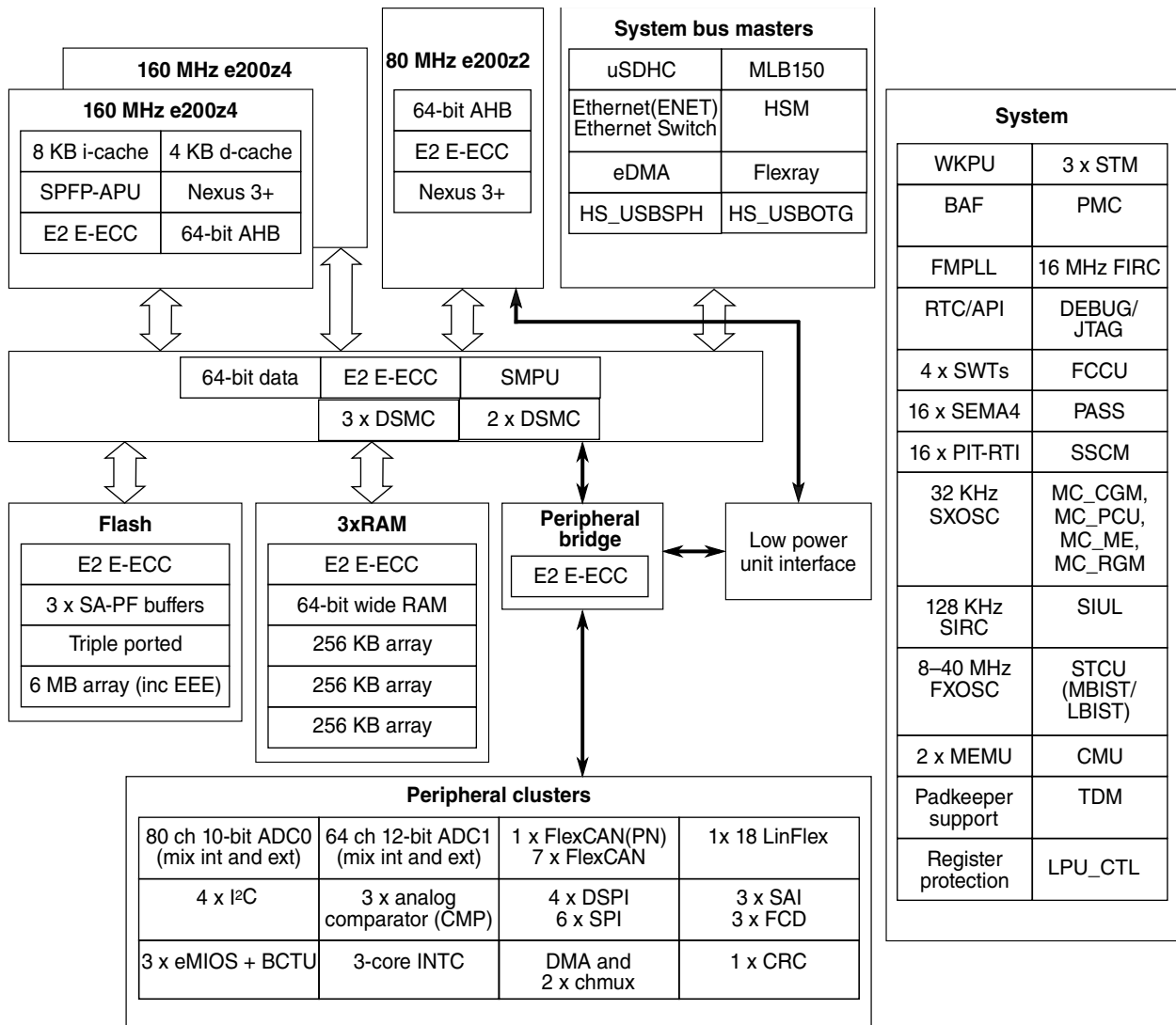


Figure 1. MPC5748G block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5748G family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest peripheral number (for example: STM_0) or memory address and end at the highest available peripheral number or memory address (for example: MPC574xC have 2 STM, ending with STM_1).

Table 1. MPC5748G Family Comparison¹

| Feature | MPC5747C | MPC5748C | MPC5746G | MPC5747G | MPC5748G |
|--|---|---------------------------|--|--|--|
| CPU | e200z4 e200z2 | e200z4 e200z2 | e200z4 e200z4 e200z2 | e200z4 e200z4 e200z2 | e200z4 e200z4 e200z2 |
| FPU | e200z4 | e200z4 | e200z4 e200z4 | e200z4 e200z4 | e200z4 e200z4 |
| Maximum Operating Frequency ² | 160MHz (z4) 80MHz (z2) | 160MHz (z4) 80MHz (z2) | 160MHz (z4) 160MHz (z4) 80MHz (z2) | 160MHz (z4) 160MHz (z4) 80MHz (z2) | 160MHz (z4) 160MHz (z4) 80MHz (z2) |
| Flash memory | 4 MB | 6 MB | 3 MB | 4 MB | 6 MB |
| EEPROM support | 32 KB to 128 KB emulated | | 32 KB to 192 KB emulated | | |
| RAM | 512 KB | 768 KB | | | |
| ECC | End to End | | | | |
| SMPU | 24 entry | | 32 entry | | |
| DMA | 32 channels | | | | |
| 10-bit ADC | 48 Standard channels 32 External channels | | | | |
| 12-bit ADC | 16 Precision channels 16 Standard channels 32 External channels | | | | |
| AnalogComparator | 3 | | | | |
| BCTU | Yes | | | | |
| SWT | 2 | | 4 | | |
| STM | 2 | | 3 | | |
| PIT-RTI | 16 channels PIT 1 channels RTI | | | | |
| RTC/API | Yes | | | | |
| Total Timer I/O ³ | 96 channels 16-bits | | | | |
| LINFlexD | 1 M/S, 15 M | | 1 M/S, 17 M | | |
| FlexCAN | 8 with optional CAN FD support | | | | |
| DSPI/SPI | 4 x DSPI 6 x SPI | | | | |

Table continues on the next page...

Table 1. MPC5748G Family Comparison¹ (continued)

| Feature | MPC5747C | MPC5748C | MPC5746G | MPC5747G | MPC5748G |
|--|----------|----------|---------------------------------------|----------|----------|
| I ² C | | | 4 | | |
| SAI/I ² S | | | 3 | | |
| FXOSC | | | 8 - 40 MHz | | |
| SXOSC | | | 32 KHz | | |
| FIRC | | | 16 MHz | | |
| SIRC | | | 128 KHz | | |
| FMPLL | | | Yes | | |
| LPU | | | Yes | | |
| FlexRay 2.1 (dual channel) | | | Yes, 128 MB | | |
| MLB150 | 0 | | | 1 | |
| USB 2.0 SPH | 0 | | | 1 | |
| USB 2.0 OTG | 0 | | | 1 | |
| SDHC | | | 1 | | |
| Ethernet (RMII, MII + 1588, Multi queue AVB support) | | | Up to 2 | | |
| 3 Port L2 Ethernet Switch | | | Optional | | |
| CRC | | | 1 | | |
| MEMU | | | 2 | | |
| STCU | | | 1 | | |
| HSM-v2 (security) | | | Optional | | |
| Censorship | | | Yes | | |
| FCCU | | | 1 | | |
| Safety level | | | Specific functions ASIL-B certifiable | | |
| User MBIST | | | Yes | | |
| User LBIST | | | Yes | | |
| I/O Retention in Standby | | | Yes | | |
| GPIO ⁴ | | | Up to 264 GPI and up to 246 GPIO | | |
| Debug | | | JTAGC, cJTAG | | |
| Nexus | | | Z4 N3+ Z2 N3+ | | |
| Packages | | | 176 LQFP-EP 256 BGA, 324 BGA | | |

1. Feature set dependent on selected peripheral multiplexing, table shows example. Peripheral availability is package dependent.
2. Based on 125°C ambient operating temperature and subject to full device characterisation.
3. Refer device datasheet and reference manual for information on to timer channel configuration and functions.
4. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device number: MPC5748G .

3.2 Ordering Information

| | | | | | | | | | | | | |
|---------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Example Code | P | PC | 57 | 4 | 8 | G | S | K0 | M | MJ | 6 | R |
| Qualification Status | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| Power Architecture | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| Automotive Platform | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| Core Version | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| Flash Size (core dependent) | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| Product | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| Optional fields | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| Fab and mask indicator | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| Temperature spec. | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| Package Code | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| CPU Frequency | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |
| R = Tape & Reel (blank if Tray) | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ | _____ |

| | | |
|---|--|---|
| <p>Qualification Status P = Engineering samples S = Automotive qualified</p> <p>PC = Power Architecture</p> <p>Automotive Platform 57 = Power Architecture in 55nm</p> <p>Core Version 4 = e200z4 Core Version (highest core version in the case of multiple cores)</p> <p>Flash Memory Size 6 = 3 MB 7 = 4 MB 8 = 6 MB</p> | <p>Product Version C = Body Control Feature Set G = Gateway Feature Set</p> <p>Optional fields Blank = Feature not available S = HSM (Security Module) F = CAN FD B = Both HSM and CAN FD T = HSM and 2nd Ethernet G = CAN FD and 2nd Ethernet H = HSM, CAN FD, and 2nd Ethernet</p> <p>Fab and mask version indicator K = TSMC Fab #(0,1,etc.) = Version of the maskset, like rev. 0=0N65H</p> <p>Temperature spec. C = -40.C to +85.C Ta V = -40.C to +105.C Ta M = -40.C to +125.C Ta</p> | <p>Package Code KU = 176 LQFP EP MJ = 256 MAPBGA MN = 324 MAPBGA</p> <p>CPU Frequency 2 = Each z4 operates up to 120 MHz 6 = Each z4 operates up to 160 MHz</p> <p>Shipping Method R = Tape and reel Blank = Tray</p> |
|---|--|---|

Note: Not all part number combinations are available as production product

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 2. Absolute maximum ratings

| Symbol | Parameter | Conditions ¹ | Min | Max | Unit |
|---|--|--|-------------|--|------|
| $V_{DD_HV_A}$, $V_{DD_HV_B}$, $V_{DD_HV_C}$ ² | 3.3 V - 5.5V input/output supply voltage | — | -0.3 | 6.0 | V |
| $V_{DD_HV_FLA}$ ^{3, 4} | 3.3 V flash supply voltage (when supplying from an external source in bypass mode) | — | -0.3 | 3.63 | V |
| $V_{DD_LP_DEC}$ ⁵ | Decoupling pin for low power regulators ⁶ | — | -0.3 | 1.32 | V |
| $V_{DD_HV_ADC1_REF}$ ⁷ | 3.3 V / 5.0 V ADC1 high reference voltage | — | -0.3 | 6 | V |
| $V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$ | 3.3 V to 5.5V ADC supply voltage | — | -0.3 | 6.0 | V |
| $V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$ | 3.3V to 5.5V ADC supply ground | — | -0.1 | 0.1 | V |
| V_{DD_LV} | Core logic supply voltage | — | -0.3 | 1.32 | V |
| V_{INA} | Voltage on analog pin with respect to ground (V_{SS_HV}) | — | -0.3 | Min ($V_{DD_HV_x}$, $V_{DD_HV_ADCx}$, $V_{DD_ADCx_REF}$) +0.3 | V |
| V_{IN} | Voltage on any digital pin with respect to ground (V_{SS_HV}) | Relative to $V_{DD_HV_A}$, $V_{DD_HV_B}$, $V_{DD_HV_C}$ | -0.3 | $V_{DD_HV_x} + 0.3$ | V |
| I_{INJPAD} | Injected input current on any pin during overload condition | Always | -5 | 5 | mA |
| I_{INJSUM} | Absolute sum of all injected input currents during overload condition | — | -50 | 50 | mA |
| T_{ramp} | Supply ramp rate | — | 0.5 V / min | 100V/ms | — |
| T_A ⁸ | Ambient temperature | — | -40 | 125 | °C |
| T_{STG} | Storage temperature | — | -55 | 165 | °C |

1. All voltages are referred to V_{SS_HV} unless otherwise specified

2. $V_{DD_HV_B}$ and $V_{DD_HV_C}$ are common together on the 176 LQFP-EP package.

3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
5. This pin should be decoupled with low ESR 1 μ F capacitor.
6. Not available for input voltage, only for decoupling internal regulators
7. 10-bit ADC does not have dedicated reference and its reference is double bonded to 10-bit ADC supply(VDD_HV_ADC0).
8. $T_J=150^{\circ}\text{C}$. Assumes $T_A=125^{\circ}\text{C}$
 - Assumes maximum θ_{JA} . See [Thermal attributes](#)

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 5V range, VDD_HV_FLA should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

Table 3. Recommended operating conditions (V_{DD_HV_x} = 3.3 V)

| Symbol | Parameter | Conditions ¹ | Min ² | Max | Unit |
|--|--------------------------------|-------------------------|---|-----|------|
| V _{DD_HV_A} V _{DD_HV_B} V _{DD_HV_C} | HV IO supply voltage | — | 3.15 | 3.6 | V |
| V _{DD_HV_FLA} ³ | HV flash supply voltage | — | 3.15 | 3.6 | V |
| V _{DD_HV_ADC1_REF} | HV ADC1 high reference voltage | — | 3.0 | 5.5 | V |
| V _{DD_HV_ADC0} V _{DD_HV_ADC1} | HV ADC supply voltage | — | max(V _{DD_HV_A} , V _{DD_HV_B} , V _{DD_HV_C}) - 0.05 | 3.6 | V |

Table continues on the next page...

Table 3. Recommended operating conditions ($V_{DD_HV_x} = 3.3\text{ V}$) (continued)

| Symbol | Parameter | Conditions ¹ | Min ² | Max | Unit |
|--|---|-------------------------------|------------------|------|------|
| $V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$ | HV ADC supply ground | — | -0.1 | 0.1 | V |
| V_{DD_LV} ^{4, 5} | Core supply voltage | — | 1.2 | 1.32 | V |
| $V_{IN1_CMP_REF}$ ^{6, 7} | Analog Comparator DAC reference voltage | — | 3.15 | 3.6 | V |
| I_{INJPAD} | Injected input current on any pin during overload condition | — | -3.0 | 3.0 | mA |
| T_A ⁸ | Ambient temperature under bias | $f_{CPU} \leq 160\text{ MHz}$ | -40 | 125 | °C |
| T_J | Junction temperature under bias | — | -40 | 150 | °C |

- All voltages are referred to V_{SS_HV} unless otherwise specified
- Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
- $V_{DD_HV_FLA}$ must be connected to $V_{DD_HV_A}$ when $V_{DD_HV_A} = 3.3\text{V}$
- Only applicable when supplying from external source.
- V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
- $V_{IN1_CMP_REF} \leq V_{DD_HV_A}$
- This supply is shorted $V_{DD_HV_A}$ on lower packages.
- $T_J = 150^\circ\text{C}$. Assumes $T_A = 125^\circ\text{C}$
 - Assumes maximum θ_{JA} . See [Thermal attributes](#)

NOTE

If $V_{DD_HV_A}$ is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. $V_{DD_HV_FLA}$ should not be supplied externally and should only have decoupling capacitor.

Table 4. Recommended operating conditions ($V_{DD_HV_x} = 5\text{ V}$)

| Symbol | Parameter | Conditions ¹ | Min ² | Max | Unit |
|---|---|-------------------------|---|------|------|
| $V_{DD_HV_A}$ $V_{DD_HV_B}$ $V_{DD_HV_C}$ | HV IO supply voltage | — | 4.5 | 5.5 | V |
| $V_{DD_HV_FLA}$ ³ | HV flash supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD_HV_ADC1_REF}$ | HV ADC1 high reference voltage | — | 3.15 | 5.5 | V |
| $V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$ | HV ADC supply voltage | — | $\max(V_{DD_H}\text{ V}_A, V_{DD_H}\text{ V}_B, V_{DD_H}\text{ V}_C) - 0.05$ | 5.5 | V |
| $V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$ | HV ADC supply ground | — | -0.1 | 0.1 | V |
| V_{DD_LV} ⁴ | Core supply voltage | — | 1.2 | 1.32 | V |
| $V_{IN1_CMP_REF}$ ^{5, 6} | Analog Comparator DAC reference voltage | — | 3.15 | 5.5 | V |
| I_{INJPAD} | Injected input current on any pin during overload condition | — | -3.0 | 3.0 | mA |

Table continues on the next page...

Table 4. Recommended operating conditions ($V_{DD_HV_x} = 5\text{ V}$) (continued)

| Symbol | Parameter | Conditions ¹ | Min ² | Max | Unit |
|--------------------|---------------------------------|-------------------------------|------------------|-----|------|
| T_A ⁷ | Ambient temperature under bias | $f_{CPU} \leq 160\text{ MHz}$ | -40 | 125 | °C |
| T_J | Junction temperature under bias | — | -40 | 150 | °C |

- All voltages are referred to V_{SS_HV} unless otherwise specified
- Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
- When V_{DD_HV} is in 5 V range, $V_{DD_HV_FLA}$ cannot be supplied externally. This pin is decoupled with C_{flash_reg} .
- V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
- $V_{IN1_CMP_REF} \leq V_{DD_HV_A}$
- This supply is shorted $V_{DD_HV_A}$ on lower packages.
- $T_J = 150^\circ\text{C}$. Assumes $T_A = 125^\circ\text{C}$
 - Assumes maximum θ_{JA} . See [Thermal attributes](#)

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
 - Control of external NPN ballast transistor
 - Connecting an external 1.25V (nominal) directly without the NPN ballast
- Internal generation of the 3.3V flash supply when device connected in 5V applications
- External bypass of the 3.3V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold ($LVD_IO_A_LO$) for $V_{DD_HV_IO_A}$ supply
- Low voltage detector - high threshold ($LVD_IO_A_Hi$) for $V_{DD_HV_IO_A}$ supply
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (V_{DD_LV})
- Power on Reset (POR_LV) for 1.25 V digital core supply (V_{DD_LV})
- Power on Reset (POR_HV) for 3.3V to 5V supply ($V_{DD_HV_A}$)

The following bipolar transistors¹ are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for I_{dd} , collector voltage, etc

1. BCP56, MCP68 and MJD31 are guaranteed ballasts.

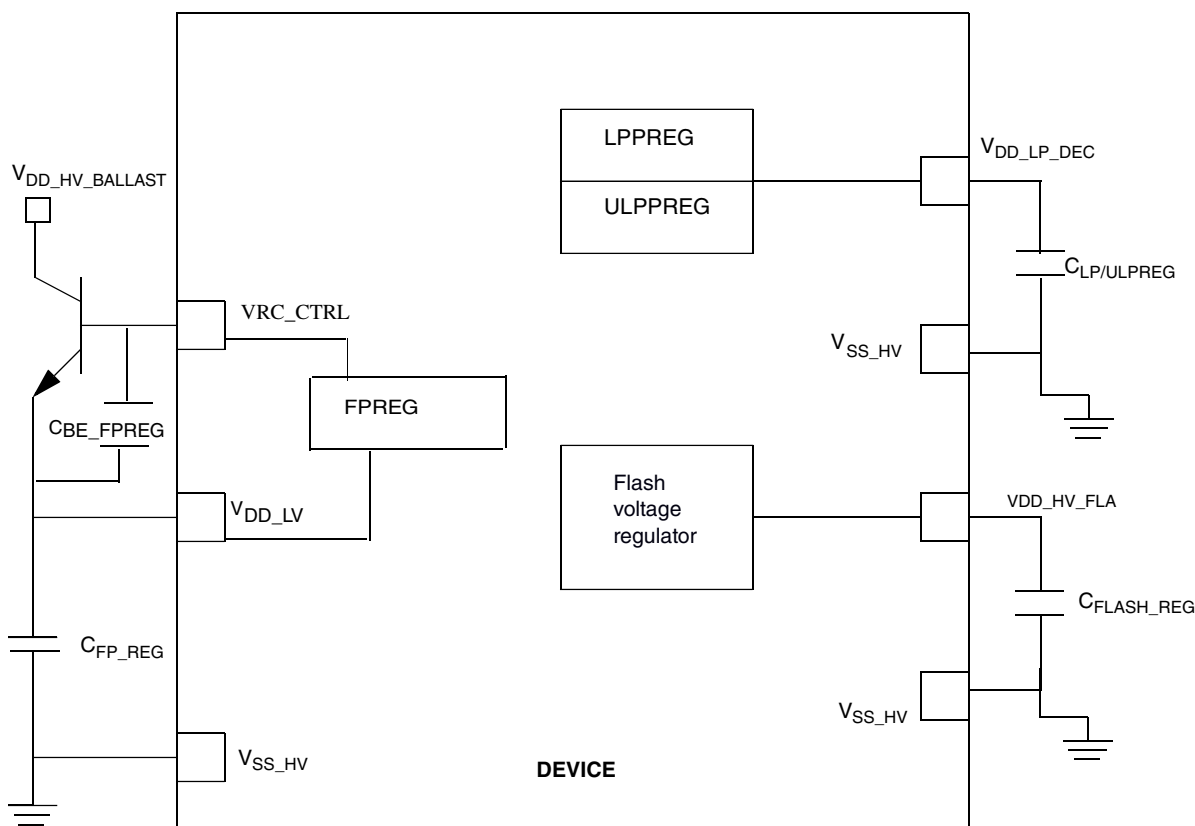


Figure 2. Voltage regulator capacitance connection

Table 5. Voltage regulator electrical specifications

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|---|---|-------|------------------|------|------|
| C _{fp_reg} ¹ | External decoupling / stability capacitor | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1.32 | 2.2 ² | 3 | μF |
| | Combined ESR of external capacitor | — | 0.001 | — | 0.03 | Ohm |
| C _{lp/ulp_reg} | External decoupling / stability capacitor for internal low power regulators | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 0.8 | 1 | 1.4 | μF |
| | Combined ESR of external capacitor | — | 0.001 | — | 0.1 | Ohm |
| C _{be_fpreg} ³ | Capacitor in parallel to base-emitter | BCP68 and BCP56 | | 3.3 | | nF |
| | | MJD31 | | 4.7 | | |
| C _{flash_reg} ⁴ | External decoupling / stability capacitor for internal Flash regulators | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1.32 | 2.2 | 3 | μF |
| | Combined ESR of external capacitor | — | 0.001 | — | 0.03 | Ohm |

Table continues on the next page...

Table 5. Voltage regulator electrical specifications (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------------|---|--|------|-----|-----|---------------|
| $C_{HV_VDD_A}$ | VDD_HV_A supply capacitor ⁵ | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | μF |
| $C_{HV_VDD_B}$ | VDD_HV_B supply capacitor ⁵ | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | μF |
| $C_{HV_VDD_C}$ | VDD_HV_C supply capacitor ⁵ | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | μF |
| C_{HV_ADC0} C_{HV_ADC1} | HV ADC supply decoupling capacitances | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 1 | — | — | μF |
| C_{HV_ADR} ⁶ | HV ADC SAR reference supply decoupling capacitances | Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations. | 0.47 | — | — | μF |
| $V_{DD_HV_BALLAST}$ | FPREG Ballast collector supply voltage | When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{C_BALLAST}$ less than 0.01 Ohm. | 2.25 | — | 5.5 | V |
| $R_{C_BALLAST}$ | Series resistor on collector of FPREG ballast | When VDD_HV_BALLAST is shorted to VDD_HV_A on the board | — | — | 0.1 | Ohm |
| t_{SU} | Start-up time after main supply stabilization | $C_{fp_reg} = 3 \mu\text{F}$ | — | 74 | — | μs |
| t_{ramp} | Load current transient | Iload from 15% to 55% $C_{fp_reg} = 3 \mu\text{F}$ | | 1.0 | | μs |

- Split capacitance on each pair VDD_LV pin should sum up to a total value of C_{fp_reg}
- Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
- Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
- It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FL A pin and the routing inductance should be less than 1nH.
- For VDD_HV_A, VDD_HV_B, and VDD_HV_C, 1 μf on each side of the chip
 - 0.1 μf close to each VDD/VSS pin pair.
 - 10 μf near for each power supply source
 - For VDD_LV, 0.1 μf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter.
 - For VDD_LV, 0.1 μf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter
- Only applicable to ADC1

4.4 Voltage monitor electrical characteristics

Table 6. Voltage monitor electrical characteristics

| Symbol | Parameter | State | Conditions | Configuration | | | Threshold | | | Unit |
|---------------------------------------|--|-------|------------|-----------------------|-----------------------|------------|-------------------|-------|-------|------|
| | | | | Power Up ¹ | Mask Opt ² | Reset Type | Min | Typ | Max | V |
| V _{POR_LV} | LV supply power on reset detector | Fall | Untrimmed | Yes | No | Powerup | 0.930 | 0.979 | 1.028 | V |
| | | | Trimmed | | | | 0.959 | 0.979 | 0.999 | V |
| | | Rise | Untrimmed | | | | 0.980 | 1.029 | 1.078 | V |
| | | | Trimmed | | | | 1.009 | 1.029 | 1.049 | V |
| V _{HVD_LV_cold} | LV supply high voltage monitoring, detecting at the device pin | Fall | Untrimmed | No | Yes | Functional | Disabled at Start | | | |
| | | | Trimmed | | | | 1.325 | 1.345 | 1.375 | V |
| | | Rise | Untrimmed | | | | Disabled at Start | | | |
| | | | Trimmed | | | | 1.345 | 1.365 | 1.395 | V |
| V _{LVD_LV_PD2_hot} | LV supply low voltage monitoring, detecting in the PD2 core (hot) area | Fall | Untrimmed | Yes | No | Powerup | 1.080 | 1.120 | 1.160 | V |
| | | | Trimmed | | | | 1.125 | 1.143 | 1.160 | V |
| | | Rise | Untrimmed | | | | 1.100 | 1.140 | 1.180 | V |
| | | | Trimmed | | | | 1.145 | 1.163 | 1.180 | V |
| V _{LVD_LV_PD1_hot} | LV supply low voltage monitoring, detecting in the PD1 core (hot) area | Fall | Untrimmed | Yes | No | Powerup | 1.080 | 1.120 | 1.160 | V |
| | | | Trimmed | | | | 1.114 | 1.137 | 1.160 | V |
| | | Rise | Untrimmed | | | | 1.100 | 1.140 | 1.180 | V |
| | | | Trimmed | | | | 1.134 | 1.157 | 1.180 | V |
| V _{LVD_LV_PD0_hot} | LV supply low voltage monitoring, detecting in the PD0 core (hot) area | Fall | Untrimmed | Yes | No | Powerup | 1.080 | 1.120 | 1.160 | V |
| | | | Trimmed | | | | 1.114 | 1.137 | 1.160 | V |
| | | Rise | Untrimmed | | | | 1.100 | 1.140 | 1.180 | V |
| | | | Trimmed | | | | 1.134 | 1.157 | 1.180 | V |
| V _{POR_HV} | HV supply power on reset detector | Fall | Untrimmed | Yes | No | Powerup | 2.700 | 2.850 | 3.000 | V |
| | | | Trimmed | | | | 2.815 | 2.873 | 2.930 | V |
| | | Rise | Untrimmed | | | | 2.750 | 2.900 | 3.050 | V |
| | | | Trimmed | | | | 2.845 | 2.903 | 2.960 | V |
| V _{LVD_IO_A_LO} ³ | HV IO_A supply low voltage monitoring - low range | Fall | Untrimmed | Yes | No | Powerup | 2.750 | 2.923 | 3.095 | V |
| | | | Trimmed | | | | 2.978 | 3.039 | 3.100 | V |
| | | Rise | Untrimmed | | | | 2.780 | 2.953 | 3.125 | V |
| | | | Trimmed | | | | 3.008 | 3.069 | 3.130 | V |
| V _{LVD_IO_A_HI} ³ | HV IO_A supply low voltage monitoring - high range | Fall | Trimmed | No | Yes | Functional | Disabled at Start | | | |
| | | | 4.060 | | | | 4.151 | 4.240 | V | |
| | | Rise | Trimmed | | | | Disabled at Start | | | |
| | | | 4.115 | | | | 4.201 | 4.3 | V | |

Table continues on the next page...

Table 6. Voltage monitor electrical characteristics (continued)

| Symbol | Parameter | State | Conditions | Configuration | | | Threshold | | | Unit |
|------------------------------|---|-------|------------|-----------------------|-----------------------|------------|-------------------|-------|-------|------|
| | | | | Power Up ¹ | Mask Opt ² | Reset Type | Min | Typ | Max | V |
| V _{LVD_LV_PD2_cold} | LV supply low voltage monitoring, detecting at the device pin | Fall | Untrimmed | No | Yes | Functional | Disabled at Start | | | |
| | | | Trimmed | | | | 1.14 | 1.158 | 1.175 | V |
| | | Rise | Untrimmed | | | | Disabled at Start | | | |
| | | | Trimmed | | | | 1.16 | 1.178 | 1.195 | V |

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the V_{DD_HV_ADC0}, V_{DD_HV_ADC1}, V_{DD_HV_B} and V_{DD_HV_C} I/O segments. For applications requiring monitoring of these segments, either connect these to V_{DD_HV_A} at the PCB level or monitor externally.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 7. Current consumption characteristics

| Symbol | Parameter | Conditions ¹ | Min | Typ | Max | Unit |
|------------------------------|------------------------------------|---|-----|-----|-----|------|
| I _{DD_FULL} 2, 3 | RUN Full Mode Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85°C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz | — | 219 | 520 | mA |
| | | T _a = 105°C | — | 240 | 540 | mA |
| | | T _a = 125 °C ⁴ | — | 256 | 575 | mA |
| I _{DD_GWY} 5, 6 | RUN Gateway Mode Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85°C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz | — | 183 | 460 | mA |
| | | T _a = 105°C | — | 202 | 496 | mA |

Table continues on the next page...

Table 7. Current consumption characteristics (continued)

| Symbol | Parameter | Conditions ¹ | Min | Typ | Max | Unit |
|--|---|--|-----|------|-----|---------------|
| | | $T_a = 125^\circ\text{C}^4$ | — | 220 | 521 | mA |
| $I_{DD_BODY_1}$ 7, 8 | RUN Body Mode Profile Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies $T_a = 85^\circ\text{C}$ $V_{DD_LV} = 1.25\text{ V}$ $V_{DD_HV_A} = 5.5\text{ V}$ $SYS_CLK = 120\text{ MHz}$ | — | 149 | 345 | mA |
| | | $T_a = 105^\circ\text{C}$ | — | 158 | 370 | mA |
| | | $T_a = 125^\circ\text{C}^4$ | — | 175 | 405 | mA |
| $I_{DD_BODY_2}$ ^{9, 10} | RUN Body Mode Profile Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies $T_a = 85^\circ\text{C}$ $V_{DD_LV} = 1.25\text{ V}$ $V_{DD_HV_A} = 5.5\text{ V}$ $SYS_CLK = 80\text{ MHz}$ | — | 105 | 275 | mA |
| | | $T_a = 105^\circ\text{C}$ | — | 114 | 300 | mA |
| | | $T_a = 125^\circ\text{C}^4$ | — | 131 | 338 | mA |
| I_{DD_STOP} | STOP mode Operating current | $T_a = 25^\circ\text{C}$ $V_{DD_LV} = 1.25\text{ V}$ | — | 11 | — | mA |
| | | $T_a = 85^\circ\text{C}$ $V_{DD_LV} = 1.25\text{ V}$ | — | 19.8 | 105 | |
| | | $T_a = 105^\circ\text{C}$ $V_{DD_LV} = 1.25\text{ V}$ | | 29 | 145 | |
| | | $T_a = 125^\circ\text{C}^4$ $V_{DD_LV} = 1.25\text{ V}$ | — | 45 | 160 | |
| | | | | | | |
| $I_{DD_HV_ADC_REF}$ ^{11, 12} | ADC REF Operating current | $T_a = 25^\circ\text{C}$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 3.6\text{ V}$ | — | 200 | 400 | μA |
| | | $T_a = 125^\circ\text{C}^4$ 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF} = 5.5\text{ V}$ | — | 200 | 400 | |
| $I_{DD_HV_ADCX}$ ¹² | ADC HV Operating current | $T_a = 25^\circ\text{C}$ ADC operating at 80 MHz $V_{DD_HV_ADC} = 3.6\text{ V}$ | — | 1 | 2 | mA |
| | | $T_a = 125^\circ\text{C}^4$ ADC operating at 80 MHz $V_{DD_HV_ADC} = 5.5\text{ V}$ | — | 1.2 | 2 | |

Table continues on the next page...

Table 7. Current consumption characteristics (continued)

| Symbol | Parameter | Conditions ¹ | Min | Typ | Max | Unit |
|--------------------------|--|---|-----|-----|-----|------|
| I _{DD_HV_FLASH} | Flash Operating current during read access | T _a = 125 °C ⁴ 3.3 V supplies x MHz frequency | — | 40 | 45 | mA |

- The content of the Conditions column identifies the components that draw the specific current.
- ALL Modules enabled at maximum frequency: 2 x e200Z4 @160 MHz, e200Z2 at 80 MHz, Platform @160MHz, DMA (SRAM to SRAM), all SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals (500 pll clock cycles), ENET0 transmitting, MLB transmitting, FlexRay transmitting, USB-SPH transmitting (USB-OTG only clocked), 2 x I2C transmitting (rest clocked), 1 x SAI transmitting (rest clocked), ADC0 converting using BCTU triggers triggered through PIT (other ADC clocked), RTC running, 3 x STM running, 2 x DSPI transmitting (rest clocked), 2 x SPI transmitting (rest clocked), 4 x CAN state machines working(rest clocked), 9 x LINFlexD transmitting (rest clocked), 1 x eMIOS clocked (used OPWFMB mode) (Others clock gated), SDHC,3 x CMP only clocked, FIRC, SIRC, FXOSC, SXOSC, PLL running. All others modules clock gated if not specifically mentioned. I/O supply current excluded.
- Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C.
- T_j=150°C. Assumes T_a=125°C
 - Assumes maximum θJA. See [Thermal attributes](#)
- Enabled Modules in Gateway mode: 2 x e200Z4 @160 MHz (Instruction and Data cache enabled), Platform @160MHz, e200Z2 at 80 MHz(Instruction cache enabled), all SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals(500 pll clock cycles), ENET0 transmitting, MLB transmitting, FlexRay transmitting, USB-SPH Transmitting, USB-OTG clocked, 2 x I2C transmitting, (2 x I2C clock gated), 1 x SAI transmitting (2 x SAI clock gated), ADC0 converting in continuous mode (ADC1 clock gated), PIT clocked, RTC clocked, 3 x STM clocked, 2 x DSPI transmitting(Other DSPS clock gated), 2 x SPI transmitting(Other SPIs clock gated), 4 x FlexCAN state machines clocked(other FLEXCAN clock gated), 4 x LINFlexD transmitting (Other clock gated), 1x eMIOS clocked(used OPWFMB mode) (Others clock gated), FIRC, SIRC, FXOSC, SXOSC, PLL running, BCTU, DMAMUX, ACMP clock gated. All others modules clock gated if not specifically mentioned. I/O supply current excluded
- Recommended Transistors:MJD31@85°C, 105°C and 125°C.
- Enabled Modules in Body mode enabled at maximum frequency: 2 x e200Z4 @120Mhz(Instruction and Data cache enabled),Platform@120MHz, SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals(500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT(ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting(others DSPIs clocked), 2 x SPI transmitting(others clocked), 4 x FlexCAN state machines working(others clocked), 9xLINFlexD transmitting (others clocked), 1xeMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC,CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
- Recommended Transistors:BCP56, BCP68 or MJD31 @85°C, BCP56, BCP68 or MJD31 @105°C and MJD31 @125°C.
- Enabled Modules in Body mode enabled at maximum frequency:2 x e200Z4 @80Mhz(Instruction and Data cache enabled),Platform@80MHz, SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals(500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT(ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting(others DSPIs clocked), 2 x SPI transmitting(others clocked), 4 x FlexCAN state machines working(others clocked), 9xLINFlexD transmitting (others clocked), 1xeMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC,CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
- Recommended Transistors:BCP56, BCP68 or MJD31 @85°C, 105°C and 125°C
- Internal structures hold the input voltage less than V_{DD_HV_ADC_REF} + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
- This value is the total current for two ADCs.Each ADC might consume upto 2mA at max.

Table 8. Low Power Unit (LPU) Current consumption characteristics

| Symbol | Parameter | Conditions ¹ | Min | Typ | Max | Unit |
|----------|--|---|-----|-------|------|------|
| LPU_RUN | with 256K RAM, but only one RAM being accessed | T _a = 25 °C SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF | — | 8.9 | | mA |
| | | T _a = 25 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON | | 10.2 | | |
| | | T _a = 85 °C | — | 12.5 | 22 | |
| | | T _a = 105 °C | — | 14.5 | 24 | |
| | | T _a = 125 °C ² SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON | — | 16 | 26 | |
| | | | | | | |
| LPU_STOP | with 256K RAM | T _a = 25 °C | — | 0.535 | | mA |
| | | T _a = 85 °C | — | 0.72 | 6 | |
| | | T _a = 105 °C | — | 1 | 8 | |
| | | T _a = 125 °C ² | — | 1.6 | 10.6 | |

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming T_a=T_j, as the device is in static (fully clock gated) mode. Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)

Table 9. STANDBY Current consumption characteristics

| Symbol | Parameter | Conditions ^{1,2} | Min | Typ | Max | Unit |
|---------|--------------------------|--------------------------------------|-----|------|------|------|
| STANDBY | STANDBY with 256K RAM | T _a = 25 °C | — | 50 | — | μA |
| | | T _a = 85 °C | | 414 | 2800 | |
| | | T _a = 105 °C | | 989 | 3700 | |
| | | T _a = 125 °C ³ | — | 1680 | 5100 | |

1. The content of the Conditions column identifies the components that draw the specific current.
2. Measurement is made after 50 ms settling time
3. DRUN time is << STANDBY and T_a=T_j=125 °C

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification

requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 10. ESD ratings

| Symbol | Parameter | Conditions ¹ | Class | Max value ² | Unit |
|-----------------------|---|--|-------|------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge (Human Body Model) | T _A = 25 °C conforming to AEC- Q100-002 | H1C | 2000 | V |
| V _{ESD(CDM)} | Electrostatic discharge (Charged Device Model) | T _A = 25 °C conforming to AEC- Q100-011 | C3A | 500 750 (corners) | V |

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from Freescale on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 11. Functional Pad AC Specifications @ 3.3 V Range

| Symbol | Prop. Delay (ns) ¹ L>H/H>L | | Rise/Fall Edge (ns) | | Drive Load (pF) | ipp_sre[1:0] |
|-----------------------|--|-----------|---------------------|----------|------------------------|-----------------|
| | Min | Max | Min | Max | | |
| pad_sr_hv (output) | | 6/6 | | 1.7/1.5 | 25 | 11 |
| | 2.5/2.5 | 8.25/7.5 | 0.8/0.8 | 3.25/3 | 50 | |
| | 6.4/5 | 19.5/19.5 | 3.5/2.5 | 12/12 | 200 | |
| | 2.2/2.5 | 8/8 | 0.6/0.8 | 3.75/3.5 | 25 | 10 |
| | 0.090 | 1.1 | 0.035 | 1.1 | asymmetry ² | |
| | 2.9/3.5 | 12.5/11 | 1/1 | 7/6 | 50 | |
| | 11/8 | 35/31 | 7.7/5 | 25/21 | 200 | |
| | 8.3/9.6 | 45/45 | 4/3.5 | 25/25 | 50 | 01 ³ |
| | 13.5/15 | 65/65 | 6.3/6.2 | 30/30 | 200 | |
| | 13/13 | 75/75 | 6.8/6 | 40/40 | 50 | 00 ³ |

Table continues on the next page...

Table 11. Functional Pad AC Specifications @ 3.3 V Range (continued)

| Symbol | Prop. Delay (ns) ¹ L>H/H>L | | Rise/Fall Edge (ns) | | Drive Load (pF) | ipp_sre[1:0] MSB,LSB |
|--|--|---------|---------------------|---------|-----------------|-----------------------------|
| | Min | Max | Min | Max | | |
| | 21/22 | 100/100 | 11/11 | 51/51 | 200 | |
| pad_i_hv/pad_sr_hv (input) ⁴ | | 2/2 | | 0.5/0.5 | 0.5 | NA |

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
3. Slew rate control modes
4. Input slope = 2ns

NOTE

Data based on characterization results, not tested in production.

5.2 DC electrical specifications @ 3.3V Range**Table 12. DC electrical specifications @ 3.3V Range**

| Symbol | Parameter | Value | | Unit |
|-----------------------|---|-------------------------|-------------------------|------|
| | | Min | Max | |
| dVdd ¹ | LV (core) Supply Voltage | 1.08 | 1.32 | V |
| VDD_HV_x ¹ | I/O Supply Voltage | 3.15 | 3.63 | V |
| Vih (pad_i_hv) | pad_i_hv Input Buffer High Voltage | $0.72 \cdot VDD_HV_x$ | $VDD_HV_x + 0.3$ | V |
| Vil (pad_i_hv) | pad_i_hv Input Buffer Low Voltage | $dVss - 0.3$ | $0.45 \cdot VDD_HV_x$ | V |
| Vhys (pad_i_hv) | pad_i_hv Input Buffer Hysteresis | $0.11 \cdot VDD_HV_x$ | | V |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | $0.67 \cdot VDD_HV_x$ | $VDD_HV_x + 0.3$ | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | $dVss - 0.3$ | $0.35 \cdot VDD_HV_x$ | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | $0.57 \cdot VDD_HV_x$ | $VDD_HV_x + 0.3$ | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | $dVss - 0.3$ | $0.4 \cdot VDD_HV_x$ | V |
| Vhys | CMOS Input Buffer Hysteresis | $0.09 \cdot VDD_HV_x$ | | V |
| Pull_IIH (pad_i_hv) | Weak Pullup Current ² Low | 15 | | μA |
| Pull_IIH (pad_i_hv) | Weak Pullup Current ³ High | | 55 | μA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current ³ Low | 28 | | μA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current ² High | | 85 | μA |

Table continues on the next page...

Table 12. DC electrical specifications @ 3.3V Range (continued)

| Symbol | Parameter | Value | | Unit |
|----------|--|---------------|---------------|------|
| | | Min | Max | |
| Pull_loh | Weak Pullup Current ⁴ | 15 | 50 | μA |
| Pull_lol | Weak Pulldown Current ⁵ | 15 | 50 | μA |
| linact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | μA |
| Voh | Output High Voltage ⁶ | 0.8 *VDD_HV_x | — | V |
| Vol | Output Low Voltage ⁷ | — | 0.2 *VDD_HV_x | V |
| loh_f | Full drive loh ⁸ (ipp_sre[1:0] = 11) | 18 | 70 | mA |
| lol_f | Full drive lol ⁸ (ipp_sre[1:0] = 11) | 21 | 120 | mA |
| loh_h | Half drive loh ⁸ (ipp_sre[1:0] = 10) | 9 | 35 | mA |
| lol_h | Half drive lol ⁸ (ipp_sre[1:0] = 10) | 10.5 | 60 | mA |

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. loh/lol is derived from spice simulations. These values are NOT guaranteed by test.

5.3 AC specifications @ 5 V Range

Table 13. Functional Pad AC Specifications @ 5 V Range

| Symbol | Prop. Delay (ns) ¹ L>H/H>L | | Rise/Fall Edge (ns) | | Drive Load (pF) | ipp_sre[1:0] MSB,LSB |
|-----------------------------------|--|-----------|---------------------|---------|-----------------|-------------------------|
| | Min | Max | Min | Max | | |
| pad_sr_hv (output) | | 4.5/4.5 | | 1.3/1.2 | 25 | 11 |
| | | 6/6 | | 2.5/2 | 50 | |
| | | 13/13 | | 8/8 | 200 | |
| | | 5.25/5.25 | | 3/2 | 25 | 10 |
| | | 9/8 | | 5/4 | 50 | |
| | | 22/22 | | 18/16 | 200 | |
| | | 27/27 | | 13/13 | 50 | 01 ² |
| | | 40/40 | | 24/24 | 200 | |
| | | 40/40 | | 24/24 | 50 | 00 ² |
| | 65/65 | | 40/40 | 200 | | |
| pad_i_hv/pad_sr_hv (input) | | 1.5/1.5 | | 0.5/0.5 | 0.5 | NA |

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

5.4 DC electrical specifications @ 5 V Range

Table 14. DC electrical specifications @ 5 V Range

| Symbol | Parameter | Value | | Unit |
|-----------------------|---|-----------------|----------------|------|
| | | Min | Max | |
| dVdd ¹ | LV (core) Supply Voltage | 1.08 | 1.32 | V |
| VDD_HV_x ¹ | I/O Supply Voltage | 4.5 | 5.5 | V |
| Vih (pad_i_hv) | pad_i_hv Input Buffer High Voltage | 0.7*VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil (pad_i_hv) | pad_i_hv Input Buffer Low Voltage | dVss - 0.3 | 0.45*VDD_HV_x | V |
| Vhys (pad_i_hv) | pad_i_hv Input Buffer Hysteresis | 0.09*VDD_HV_x | | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | 0.55 * VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | dVss - 0.3 | 0.4 * VDD_HV_x | V |
| Vhys | CMOS Input Buffer Hysteresis | 0.09 * VDD_HV_x | | V |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | 0.65* VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | dVss - 0.3 | 0.35*VDD_HV_x | V |
| Pull_IIH (pad_i_hv) | Weak Pullup Current ² Low | 23 | | μA |
| Pull_IIH (pad_i_hv) | Weak Pullup Current ³ High | | 82 | μA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current ³ Low | 40 | | μA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current ² High | | 130 | μA |
| Pull_loh | Weak Pullup Current ⁴ | 30 | 80 | μA |
| Pull_lol | Weak Pulldown Current ⁵ | 30 | 80 | μA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | μA |
| Voh | Output High Voltage ⁶ | 0.8 * VDD_HV_x | — | V |
| Vol | Output Low Voltage ⁷ | — | 0.2 * VDD_HV_x | V |
| Ioh_f | Full drive Ioh ⁸ (ipp_sre[1:0] = 11) | 38 | 132 | mA |
| Iol_f | Full drive Iol ⁸ (ipp_sre[1:0] = 11) | 48 | 220 | mA |
| Ioh_h | Half drive Ioh ⁸ (ipp_sre[1:0] = 10) | 19 | 66 | mA |
| Iol_h | Half drive Iol ⁸ (ipp_sre[1:0] = 10) | 24 | 110 | mA |

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA

8. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

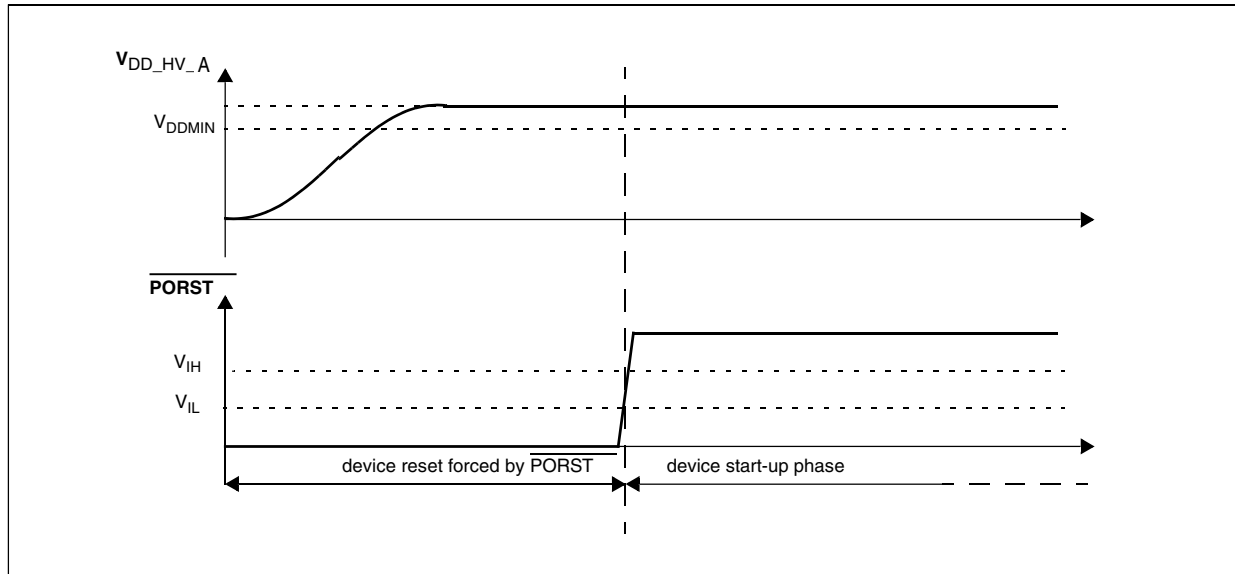


Figure 3. Start-up reset requirements

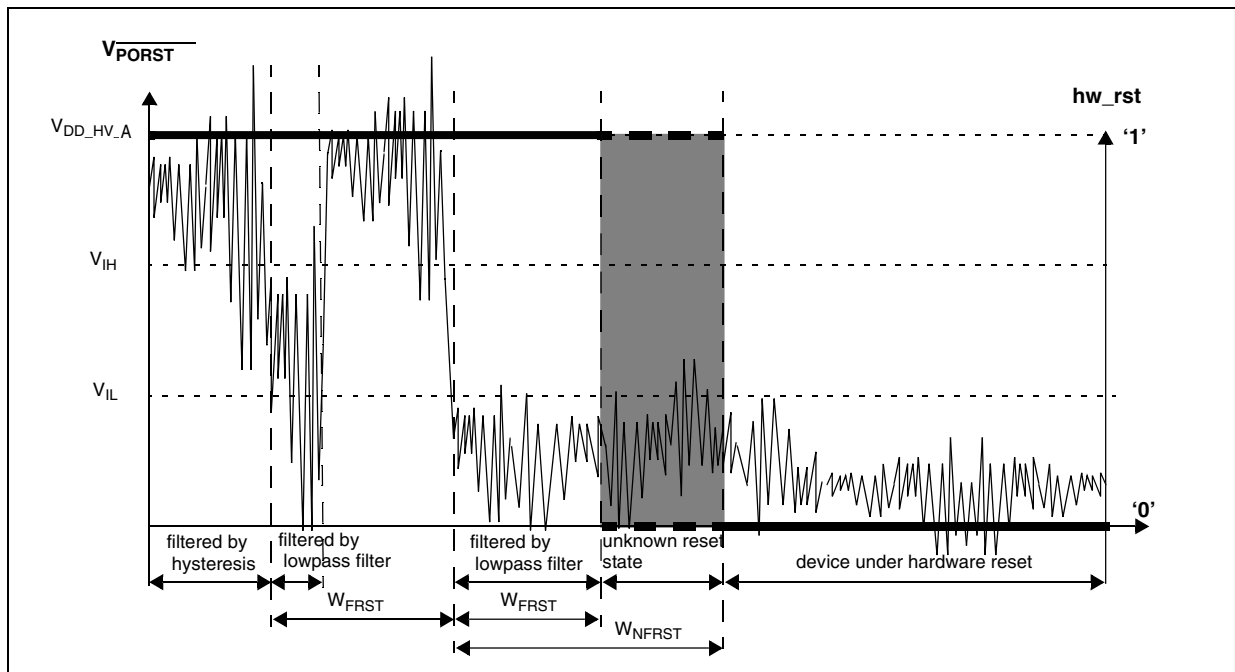


Figure 4. Noise filtering on reset signal

Table 15. Functional reset pad electrical specifications

| Symbol | Parameter | Conditions | Value | | | Unit |
|---------------------|--|---|-------|-----|---------------------------|------|
| | | | Min | Typ | Max | |
| V _{IH} | Input high level TTL (Schmitt Trigger) | — | 2.0 | — | V _{DD_HV_A} +0.4 | V |
| V _{IL} | Input low level TTL (Schmitt Trigger) | — | -0.4 | — | 0.8 | V |
| V _{HYS} | Input hysteresis TTL (Schmitt Trigger) | — | 300 | — | — | mV |
| V _{DD_POR} | Minimum supply for strong pull-down activation | — | — | — | 1.2 | V |
| I _{OL_R} | Strong pull-down current ¹ | Device under power-on reset V _{DD_HV_A} = V _{DD_POR} V _{OL} = 0.35*V _{DD_HV_A} | 0.2 | — | — | mA |
| | | Device under power-on reset V _{DD_HV_A} = V _{DD_POR} V _{OL} = 0.35*V _{DD_HV_IO} | 11 | — | — | mA |
| W _{FRST} | RESET input filtered pulse | — | — | — | 500 | ns |
| W _{NFRST} | RESET input not filtered pulse | — | 2000 | — | — | ns |
| I _{WPU} | Weak pull-up current absolute value | RESET pin V _{IN} = V _{DD} | 23 | — | 82 | μA |

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

5.6 PORST electrical specifications

Table 16. PORST electrical specifications

| Symbol | Parameter | Value | | | Unit |
|--|--------------------------------|-------|-----------------------------|-----|------|
| | | Min | Typ | Max | |
| W _{F_{PORST}} | PORST input filtered pulse | — | — | 200 | ns |
| W _{N_{F_{PORST}}} | PORST input not filtered pulse | 1000 | — | — | ns |
| V _{IH} | Input high level | — | 0.65 x V _{DD_HV_A} | — | V |
| V _{IL} | Input low level | — | 0.35 x V _{DD_HV_A} | — | V |

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

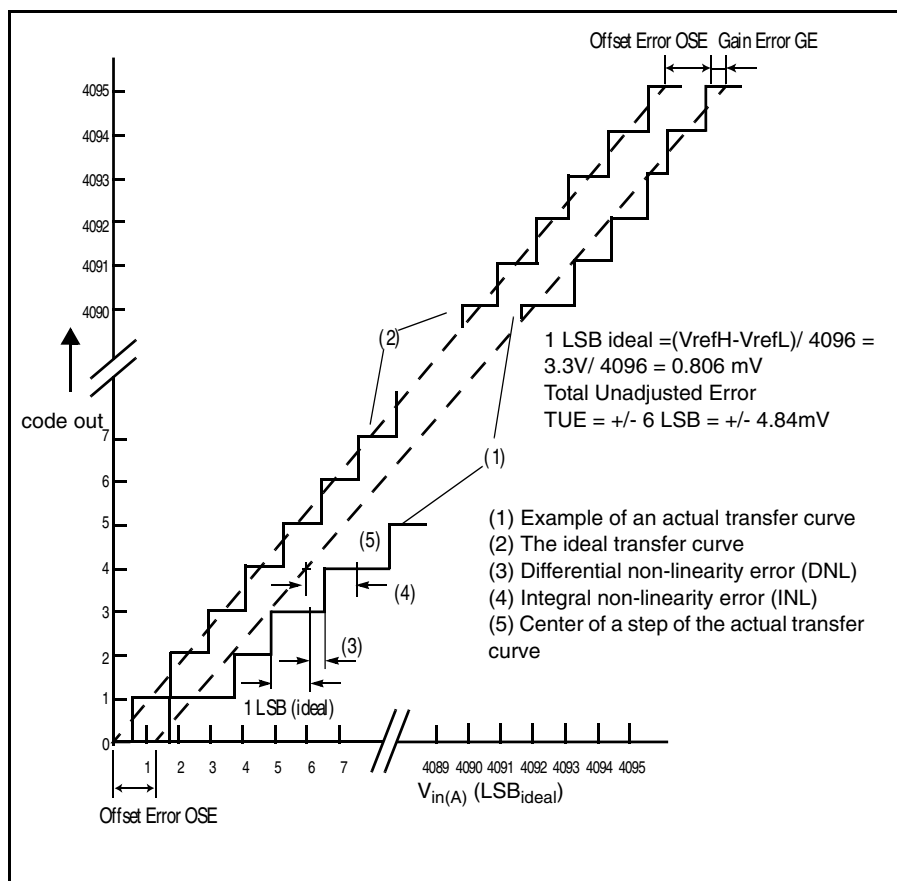


Figure 5. ADC characteristics and error definitions

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

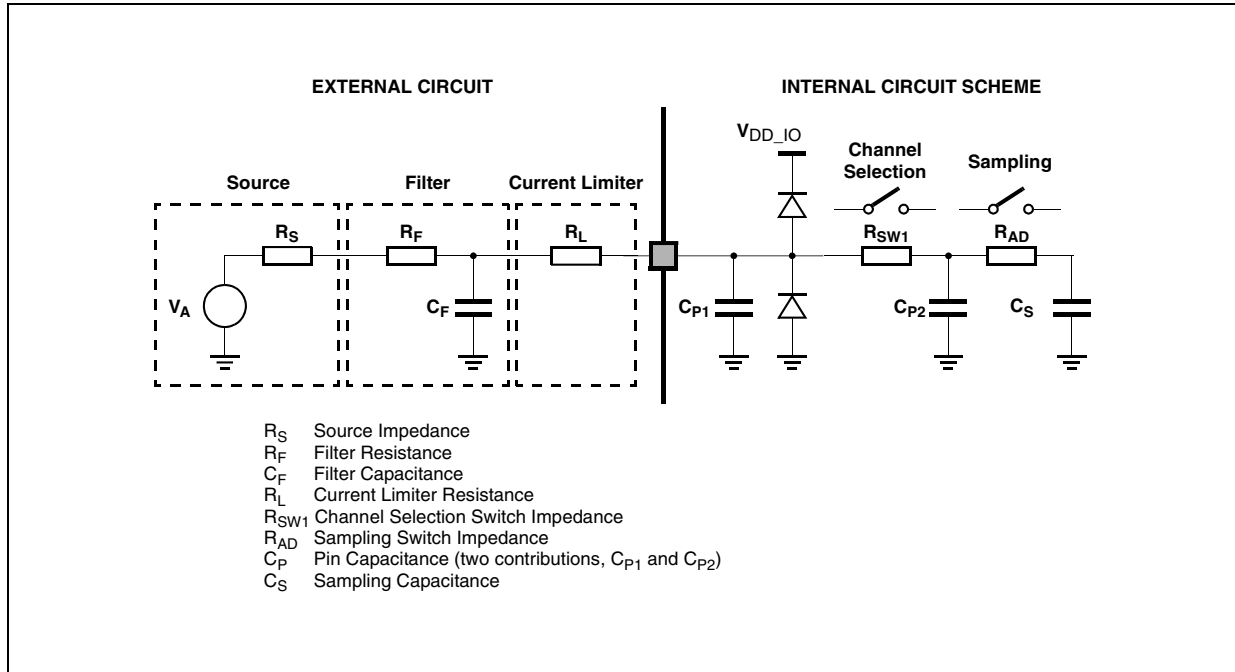


Figure 6. Input equivalent circuit

Table 17. ADC conversion characteristics (for 12-bit)

| Symbol | Parameter | Conditions | Min | Typ ¹ | Max | Unit |
|------------------------|---|-----------------------------------|------------------|------------------|------|------------|
| f_{CK} | ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK ² frequency) | — | 15.2 | 80 | 80 | MHz |
| f_s | Sampling frequency | 80 MHz | — | — | 1.00 | MHz |
| t_{sample} | Sample time ³ | 80 MHz @ 100 ohm source impedance | 250 | — | — | ns |
| t_{conv} | Conversion time ⁴ | 80 MHz | 700 | — | — | ns |
| t_{total_conv} | Total Conversion time $t_{sample} + t_{conv}$ (for standard and extended channels) | 80 MHz | 1.5 ⁵ | — | — | μ s |
| | Total Conversion time $t_{sample} + t_{conv}$ (for precision channels) | | 1 | — | — | |
| C_S ⁶ | ADC input sampling capacitance | — | — | 3 | 5 | pF |
| C_{P1} ⁶ | ADC input pin capacitance 1 | — | — | — | 5 | pF |
| C_{P2} ⁶ | ADC input pin capacitance 2 | — | — | — | 0.8 | pF |
| R_{SW1} ⁶ | Internal resistance of analog source | V_{REF} range = 4.5 to 5.5 V | — | — | 0.3 | k Ω |
| | | V_{REF} range = 3.15 to 3.6 V | — | — | 875 | Ω |
| R_{AD} ⁶ | Internal resistance of analog source | — | — | — | 825 | Ω |
| INL | Integral non-linearity (precise channel) | — | -2 | — | 2 | LSB |

Table continues on the next page...

Table 17. ADC conversion characteristics (for 12-bit) (continued)

| Symbol | Parameter | Conditions | Min | Typ ¹ | Max | Unit |
|---|---|-------------------------------------|-----|------------------|------|------|
| INL | Integral non-linearity (standard channel) | — | -3 | — | 3 | LSB |
| DNL | Differential non-linearity | — | -1 | — | 1 | LSB |
| OFS | Offset error | — | -6 | — | 6 | LSB |
| GNE | Gain error | — | -4 | — | 4 | LSB |
| ADC Analog Pad (pad going to one ADC) | Max leakage (precision channel) | 150 °C | — | — | 250 | nA |
| | Max leakage (standard channel) | 150 °C | — | — | 2500 | nA |
| | Max positive/negative injection | | -5 | — | 5 | mA |
| TUE _{precision channels} | Total unadjusted error for precision channels | Without current injection | -6 | +/-4 | 6 | LSB |
| | | With current injection ⁷ | | +/-5 | | LSB |
| TUE _{standard/extended channels} | Total unadjusted error for standard/extended channels | Without current injection | -8 | +/-6 | 8 | LSB |
| | | With current injection ⁷ | | +/-8 | | LSB |
| t _{recovery} | STOP mode to Run mode recovery time | | | | < 1 | µs |

- Active ADC input, $V_{inA} < [\min(\text{ADC_VrefH}, \text{ADC_ADV}, \text{VDD_HV_IOx})]$. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
- The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
- This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
- Apart from t_{sample} and t_{conv}, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
- See [Figure 2](#).
- Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 18. ADC conversion characteristics (for 10-bit)

| Symbol | Parameter | Conditions | Min | Typ ¹ | Max | Unit |
|-------------------------|--|-----------------------------------|------|------------------|------|------|
| f _{CK} | ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK ² frequency.) | — | 15.2 | 80 | 80 | MHz |
| f _s | Sampling frequency | — | — | — | 1.00 | MHz |
| t _{sample} | Sample time ³ | 80 MHz @ 100 ohm source impedance | 275 | — | — | ns |
| t _{conv} | Conversion time ⁴ | 80 MHz | 550 | — | — | ns |
| t _{total_conv} | Total Conversion time t _{sample} + t _{conv} (for standard channels) | 80 MHz | 1 | — | — | µs |
| | Total Conversion time t _{sample} + t _{conv} (for extended channels) | | 1.5 | — | — | |

Table continues on the next page...

Table 18. ADC conversion characteristics (for 10-bit) (continued)

| Symbol | Parameter | Conditions | Min | Typ ¹ | Max | Unit |
|---|--|-------------------------------------|-----|------------------|------|------------|
| C_S ⁵ | ADC input sampling capacitance | — | — | 3 | 5 | pF |
| C_{P1} ⁵ | ADC input pin capacitance 1 | — | — | — | 5 | pF |
| C_{P2} ⁵ | ADC input pin capacitance 2 | — | — | — | 0.8 | pF |
| R_{SW1} ⁵ | Internal resistance of analog source | V_{REF} range = 4.5 to 5.5 V | — | — | 0.3 | k Ω |
| | | V_{REF} range = 3.15 to 3.6 V | — | — | 875 | Ω |
| R_{AD} ⁵ | Internal resistance of analog source | — | — | — | 825 | Ω |
| INL | Integral non-linearity | — | -2 | — | 2 | LSB |
| DNL | Differential non-linearity | — | -1 | — | 1 | LSB |
| OFS | Offset error | — | -4 | — | 4 | LSB |
| GNE | Gain error | — | -4 | — | 4 | LSB |
| ADC Analog Pad (pad going to one ADC) | Max leakage (standard channel) | 150 °C | — | — | 2500 | nA |
| | Max positive/negative injection | | -5 | — | 5 | mA |
| $TUE_{\text{standard/extended channels}}$ | Total unadjusted error for standard channels | Without current injection | -4 | +/-3 | 4 | LSB |
| | | With current injection ⁶ | | +/-4 | | LSB |
| t_{recovery} | STOP mode to Run mode recovery time | | | | < 1 | μ s |

- Active ADC Input, $V_{inA} < [\min(\text{ADC_ADV}, \text{IO_Supply_A,B,C})]$. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A, B, C and ADC_Supply.
- The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
- This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
- See [Figure 2](#)
- Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (V_{INA} , see Table: 'Absolute maximum ratings') must be honored to meet TUE spec quoted here

NOTE

The ADC input pins sit across all three I/O segments, VDD_HV_A, VDD_HV_B and VDD_HV_C.

6.1.2 Analog Comparator (CMP) electrical specifications**Table 19. Comparator and 6-bit DAC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|------------|---|------|------|------|---------|
| I_{DDHS} | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 250 | μ A |

Table continues on the next page...

Table 19. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|--|-----------------|------|-------------------------------|------------------|
| I _{DDL5} | Supply current, low-speed mode (EN=1, PMODE=0) | — | 5 | 11 | μA |
| V _{AIN} | Analog input voltage | V _{SS} | — | V _{IN1_CMP_RE F} | V |
| V _{AIO} | Analog input offset voltage ¹ | -42 | — | 42 | mV |
| V _H | Analog comparator hysteresis ² | — | 1 | 25 | mV |
| | • CR0[HYSTCTR] = 00 | — | 20 | 50 | mV |
| | • CR0[HYSTCTR] = 01 | — | 40 | 70 | mV |
| | • CR0[HYSTCTR] = 10 | — | 60 | 105 | mV |
| | • CR0[HYSTCTR] = 11 | — | — | — | — |
| t _{DHS} | Propagation Delay, High Speed Mode (Full Swing) ^{1,3} | — | — | 250 | ns |
| t _{DLS} | Propagation Delay, Low power Mode (Full Swing) ^{1,3} | — | 5 | 14 | μs |
| | Analog comparator initialization delay, High speed mode ⁴ | — | 4 | | μs |
| | Analog comparator initialization delay, Low speed mode ⁴ | — | 100 | | μs |
| I _{DAC6b} | 6-bit DAC current adder (when enabled) | | | | |
| | 3.3V Reference Voltage | — | 6 | 9 | μA |
| | 5V Reference Voltage | — | 10 | 16 | μA |
| INL | 6-bit DAC integral non-linearity | -0.5 | — | 0.5 | LSB ⁵ |
| DNL | 6-bit DAC differential non-linearity | -0.8 | — | 0.8 | LSB |

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD_HV_A}-0.6V
3. Full swing = V_{IH}, V_{IL}
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = V_{reference}/64

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

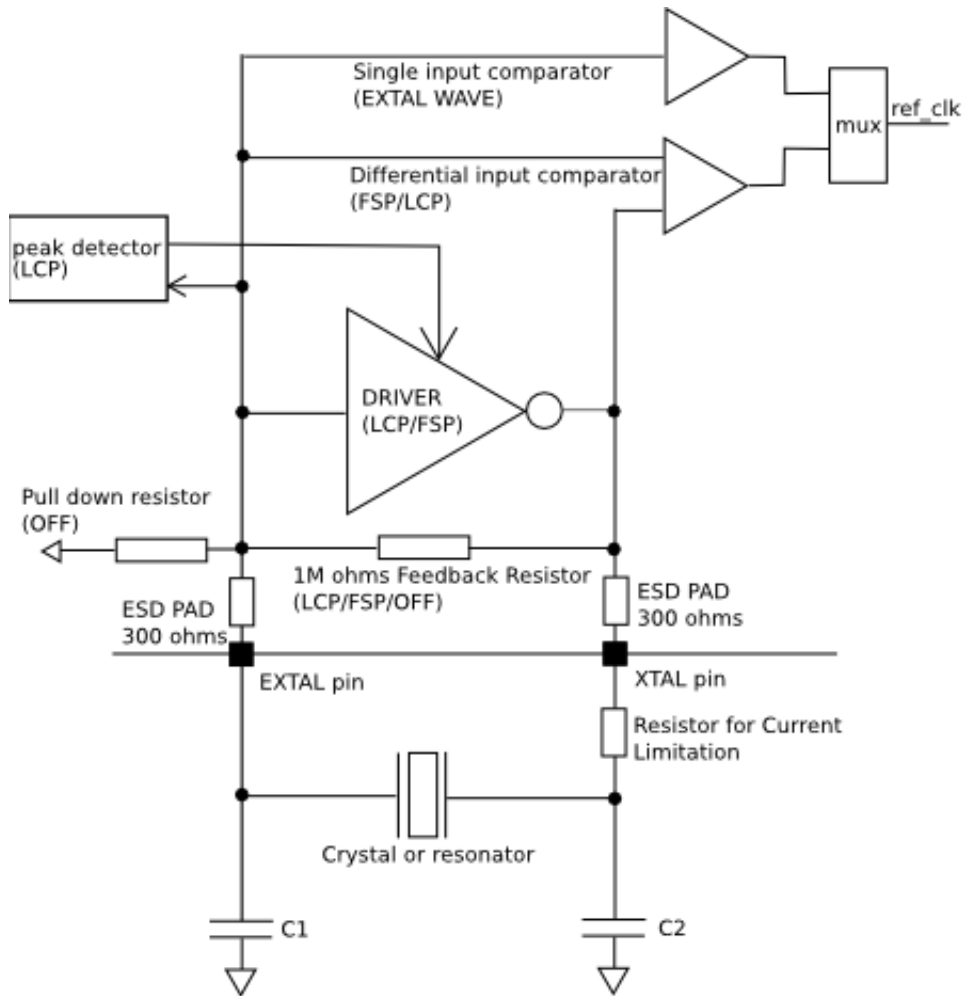


Figure 7. Oscillator connections scheme

Table 20. Main oscillator electrical characteristics

| Symbol | Parameter | Mode | Conditions | Min | Typ | Max | Unit |
|---------------------|----------------------|---------|------------|-----|-----|-----|------|
| f _{XOSCHS} | Oscillator frequency | FSP/LCP | | 8 | | 40 | MHz |

Table continues on the next page...

Table 20. Main oscillator electrical characteristics (continued)

| Symbol | Parameter | Mode | Conditions | Min | Typ | Max | Unit |
|-----------------------|--|----------------------|-----------------------|-----|------|-----|-----------------|
| g _m OSCHS | Driver Transconductance | LCP | | | 23 | | mA/V |
| | | FSP | | | 33 | | |
| V _{XOSCHS} | Oscillation Amplitude | LCP ^{1, 2} | 8 MHz | | 1.0 | | V _{PP} |
| | | | 16 MHz | | 1.0 | | |
| | | | 40 MHz | | 0.8 | | |
| T _{XOSCHSSU} | Startup time | FSP/LCP ³ | 8 MHz | | 2 | | ms |
| | | | 16 MHz | | 1 | | |
| | | | 40 MHz | | 0.5 | | |
| | Oscillator Analog Circuit supply current | FSP | 8 MHz | | 2.2 | | mA |
| | | | 16 MHz | | 2.2 | | |
| | | | 40 MHz | | 3.2 | | |
| | | LCP | 8 MHz | | 141 | | uA |
| | | | 16 MHz | | 252 | | |
| | | | 40 MHz | | 518 | | |
| V _{IH} | Input High level CMOS Schmitt trigger | EXT Wave | Oscillator supply=3.3 | | 1.84 | | V |
| V _{IL} | Input low level CMOS Schmitt trigger | EXT Wave | Oscillator supply=3.3 | | 1.48 | | V |

1. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.
2. Typ value for oscillator supply 3.3 V@27 °C
3. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board

6.2.2 32 kHz Oscillator electrical specifications

Table 21. 32 kHz oscillator electrical specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---------------------|---|-----------|-----|-----|-----|------|
| f _{osc_lo} | Oscillator crystal or resonator frequency | | 32 | | 40 | KHz |
| t _{cst} | Crystal Start-up Time ^{1, 2} | | | | 2 | s |

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 22. 16 MHz RC Oscillator electrical specifications

| Symbol | Parameter | Conditions | Value | | | Unit |
|---------------|---|---------------------|-------|-----|-----|---------|
| | | | Min | Typ | Max | |
| F_{Target} | IRC target frequency | — | — | 16 | — | MHz |
| PTA | IRC frequency variation after trimming | — | -5 | — | 5 | % |
| $T_{startup}$ | Startup time | — | — | — | 1.5 | us |
| T_{STJIT} | Cycle to cycle jitter | — | — | — | 1.5 | % |
| T_{LTJIT} | Long term jitter | — | — | — | 0.2 | % |
| I_{VDDHV} | Current consumption on 3.3 V power supply | After $T_{startup}$ | — | — | 75 | μA |
| $I_{VDDL V}$ | Current consumption on 1.2 V power supply | After $T_{startup}$ | — | — | 25 | μA |

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

6.2.4 128 KHz Internal RC oscillator Electrical specifications

Table 23. 128 KHz Internal RC oscillator electrical specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|-------------------------|------------------------|---------------|-----|-----|-------|---------|
| F_{osc1} ¹ | Oscillator frequency | Calibrated | 119 | 128 | 136.5 | KHz |
| | Temperature dependence | | | | 600 | ppm/C |
| | Supply dependence | | | | 18 | %/V |
| | Supply current | Clock running | | | 2.75 | μA |
| | | Clock stopped | | | 200 | nA |

1. Vdd=1.2 V, 1.32V, T_a =-40 C, 125 C

6.2.5 PLL electrical specifications

Table 24. PLL electrical specifications

| Parameter | Min | Typ | Max | Unit | Comments |
|---------------------|-----|-----|------|------|----------|
| Input Frequency | 8 | | 40 | MHz | |
| VCO Frequency Range | 600 | | 1280 | MHz | |

Table continues on the next page...

**Table 24. PLL electrical specifications
(continued)**

| Parameter | Min | Typ | Max | Unit | Comments |
|----------------------------------|-----------|-----|------------------------------|------|---|
| Duty Cycle at pllclkout | 48% | | 52% | | This specification is guaranteed at PLL IP boundary |
| Period Jitter | | | See Table 25 | ps | NON SSCG mode |
| TIE | | | See Table 25 | | at 960 M Integrated over 1MHz offset not valid in SSCG mode |
| Modulation Depth (Center Spread) | +/- 0.25% | | +/- 4.0% | | |
| Modulation Frequency | | | 32 | KHz | |
| Lock Time | | | 60 | μs | Calibration mode |
| | 10 | | 30 | μs | Calibration bypass mode (wake-up mode) |

Table 25. Jitter calculation

| Type of jitter | Jitter due to Supply Noise (ps) J_{SN}^1 | Jitter due to Fractional Mode (ps) J_{SDM}^2 | Jitter due to Fractional Mode J_{SSCG} (ps) 3 | 1 Sigma Random Jitter J_{RJ} (ps) 4 | Total Period Jitter (ps) |
|------------------------------------|--|--|--|--|--|
| Period Jitter | 60 ps | 3% of pllclkout1,2 | Modulation depth | 0.1% of pllclkout1,2 | $\pm(J_{SN}+J_{SDM}+J_{SSCG}+N^{[4]} \times J_{RJ})$ |
| Long Term Jitter (Integer Mode) | | | | 40 | $\pm(N \times J_{RJ})$ |
| Long Term jitter (Fractional Mode) | | | | 100 | $\pm(N \times J_{RJ})$ |

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on avdd, avss, dvdd, dvss.
2. This jitter component is added when the PLL is working in the fractional mode.
3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.
4. The value of N is dependent on the accuracy requirement of the application. See [Percentage of sample exceeding specified value of jitter table](#)

Table 26. Percentage of sample exceeding specified value of jitter

| N | Percentage of samples exceeding specified value of jitter (%) |
|---|---|
| 1 | 31.73 |
| 2 | 4.55 |
| 3 | 0.27 |
| 4 | $6.30 \times 1e-03$ |
| 5 | $5.63 \times 1e-05$ |
| 6 | $2.00 \times 1e-07$ |
| 7 | $2.82 \times 1e-10$ |

6.3 Memory interfaces

6.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 27 shows the estimated Program/Erase times.

Table 27. Flash memory program and erase specifications

| Symbol | Characteristic ¹ | Typ ² | Factory Programming ^{3,4} | | Field Update | | Unit | |
|----------------------|------------------------------------|------------------|------------------------------------|--------------------------------|----------------------------------|---------------------------|------|------------------|
| | | | Initial Max | Initial Max, Full Temp | Typical End of Life ⁵ | Lifetime Max ⁶ | | |
| | | | 20°C ≤ T _A ≤ 30°C | -40°C ≤ T _J ≤ 150°C | -40°C ≤ T _J ≤ 150°C | ≤ 1,000 cycles | | ≤ 250,000 cycles |
| t _{dwpgm} | Doubleword (64 bits) program time | 43 | 100 | 150 | 55 | 500 | μs | |
| t _{ppgm} | Page (256 bits) program time | 73 | 200 | 300 | 108 | 500 | μs | |
| t _{qppgn} | Quad-page (1024 bits) program time | 268 | 800 | 1,200 | 396 | 2,000 | μs | |
| t _{16kers} | 16 KB Block erase time | 168 | 290 | 320 | 250 | 1,000 | ms | |
| t _{16kpgn} | 16 KB Block program time | 34 | 45 | 50 | 40 | 1,000 | ms | |
| t _{32kers} | 32 KB Block erase time | 217 | 360 | 390 | 310 | 1,200 | ms | |
| t _{32kpgm} | 32 KB Block program time | 69 | 100 | 110 | 90 | 1,200 | ms | |
| t _{64kers} | 64 KB Block erase time | 315 | 490 | 590 | 420 | 1,600 | ms | |
| t _{64kpgm} | 64 KB Block program time | 138 | 180 | 210 | 170 | 1,600 | ms | |
| t _{256kers} | 256 KB Block erase time | 884 | 1,520 | 2,030 | 1,080 | 4,000 | — | ms |
| t _{256kpgm} | 256 KB Block program time | 552 | 720 | 880 | 650 | 4,000 | — | ms |

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programming times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.2 Flash memory Array Integrity and Margin Read specifications

Table 28. Flash memory Array Integrity and Margin Read specifications

| Symbol | Characteristic | Min | Typical | Max ¹ | Units ² |
|-----------------|--|--------|---------|------------------------------|--------------------|
| $t_{ai16kseq}$ | Array Integrity time for sequential sequence on 16KB block. | — | — | 512 x Tperiod x Nread | — |
| $t_{ai32kseq}$ | Array Integrity time for sequential sequence on 32KB block. | — | — | 1024 x Tperiod x Nread | — |
| $t_{ai64kseq}$ | Array Integrity time for sequential sequence on 64KB block. | — | — | 2048 x Tperiod x Nread | — |
| $t_{ai256kseq}$ | Array Integrity time for sequential sequence on 256KB block. | — | — | 8192 x Tperiod x Nread | — |
| $t_{mr16kseq}$ | Margin Read time for sequential sequence on 16KB block. | 73.81 | — | 110.7 | μs |
| $t_{mr32kseq}$ | Margin Read time for sequential sequence on 32KB block. | 128.43 | — | 192.6 | μs |
| $t_{mr64kseq}$ | Margin Read time for sequential sequence on 64KB block. | 237.65 | — | 356.5 | μs |
| $t_{mr256kseq}$ | Margin Read time for sequential sequence on 256KB block. | 893.01 | — | 1,339.5 | μs |

1. Array Integrity times need to be calculated and is dependant on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

6.3.3 Flash memory module life specifications

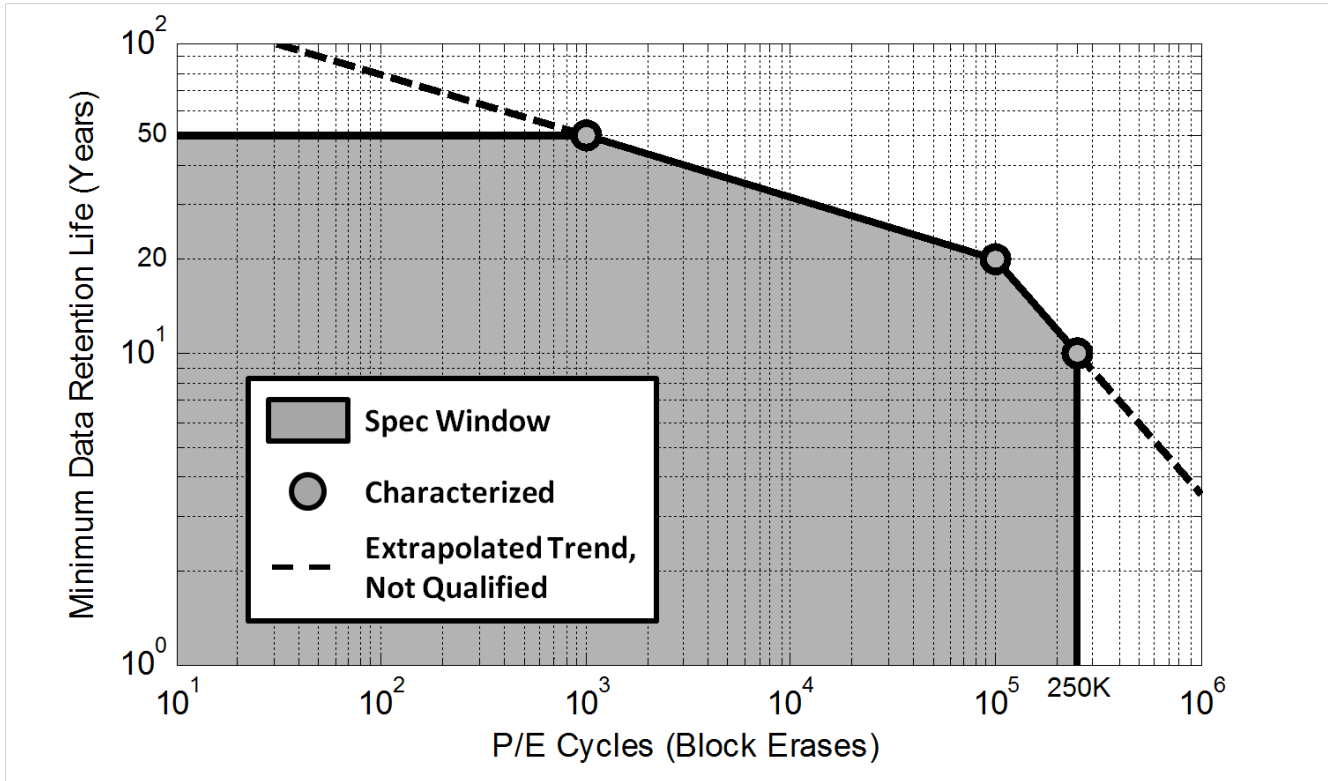
Table 29. Flash memory module life specifications

| Symbol | Characteristic | Conditions | Min | Typical | Units |
|------------------|--|-----------------------------------|---------|---------|------------|
| Array P/E cycles | Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks. ¹ | — | 250,000 | — | P/E cycles |
| | Number of program/erase cycles per block for 256 KB blocks. ² | — | 1,000 | 250,000 | P/E cycles |
| Data retention | Minimum data retention. | Blocks with 0 - 1,000 P/E cycles. | 50 | — | Years |
| | | Blocks with 100,000 P/E cycles. | 20 | — | Years |
| | | Blocks with 250,000 P/E cycles. | 10 | — | Years |

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

6.3.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



6.3.5 Flash memory AC timing specifications

Table 30. Flash memory AC timing specifications

| Symbol | Characteristic | Min | Typical | Max | Units |
|------------|---|-----|--------------------------------------|--|---------|
| t_{psus} | Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1. | — | 7 plus four system clock periods | 9.1 plus four system clock periods | μs |
| t_{esus} | Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1. | — | 16 plus four system clock periods | 20.8 plus four system clock periods | μs |
| t_{res} | Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low. | — | — | 100 | ns |

Table continues on the next page...

Table 30. Flash memory AC timing specifications (continued)

| Symbol | Characteristic | Min | Typical | Max | Units |
|---------------|--|--|---|--|---------|
| t_{done} | Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared. | — | — | 5 | ns |
| t_{dones} | Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1. | — | 16 plus four system clock periods | 20.8 plus four system clock periods | μ s |
| t_{drcv} | Time to recover once exiting low power mode. | 16 plus seven system clock periods. | — | 45 plus seven system clock periods | μ s |
| $t_{aistart}$ | Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP | — | — | 5 | ns |
| t_{aistop} | Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request. | — | — | 80 plus fifteen system clock periods | ns |
| t_{mrstop} | Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request. | 10.36 plus four system clock periods | — | 20.42 plus four system clock periods | μ s |

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 31. Flash Read Wait State and Address Pipeline Control Combinations

| Flash frequency | RWSC setting | APC setting |
|-----------------------------|--------------|-------------|
| 0 MHz < fFlash <= 33 MHz | 0 | 0 |
| 33 MHz < fFlash <= 100 MHz | 2 | 1 |
| 100 MHz < fFlash <= 133 MHz | 3 | 1 |
| 133 MHz < fFlash <= 160 MHz | 4 | 1 |

6.4 Communication interfaces

6.4.1 DSPI timing

Table 32. DSPI electrical specifications

| No | Symbol | Parameter | Conditions | High Speed Mode | | low Speed mode | | Unit |
|----|------------|-----------------------------|---|------------------|------------------|-----------------|-----------------|------|
| | | | | Min | Max | Min | Max | |
| 1 | t_{SCK} | DSPI cycle time | Master (MTFE = 0) | 25 | — | 50 | — | ns |
| | | | Slave (MTFE = 0) | 40 | — | 60 | — | |
| 2 | t_{CSC} | PCS to SCK delay | — | 16 | — | — | — | ns |
| 3 | t_{ASC} | After SCK delay | — | 16 | — | — | — | ns |
| 4 | t_{SDC} | SCK duty cycle | — | $t_{SCK}/2 - 10$ | $t_{SCK}/2 + 10$ | — | — | ns |
| 5 | t_A | Slave access time | \overline{SS} active to SOUT valid | — | 40 | — | — | ns |
| 6 | t_{DIS} | Slave SOUT disable time | ss inactive to SOUT High-Z or invalid | — | 10 | — | — | ns |
| 7 | t_{PCSC} | PCSx to PCSS time | — | 13 | — | — | — | ns |
| 8 | t_{PASC} | PCSS to PCSx time | — | 13 | — | — | — | ns |
| 9 | t_{SUI} | Data setup time for inputs | Master (MTFE = 0) | NA | — | 20 | — | ns |
| | | | Slave | 2 | — | 2 | — | |
| | | | Master (MTFE = 1, CPHA = 0) | 15 | — | 8 ¹ | — | |
| | | | Master (MTFE = 1, CPHA = 1) | 15 | — | 20 | — | |
| 10 | t_{HI} | Data hold time for inputs | Master (MTFE = 0) | NA | — | -5 | — | ns |
| | | | Slave | 4 | — | 4 | — | |
| | | | Master (MTFE = 1, CPHA = 0) | 0 | — | 11 ¹ | — | |
| | | | Master (MTFE = 1, CPHA = 1) | 0 | — | -5 | — | |
| 11 | t_{SUO} | Data valid (after SCK edge) | Master (MTFE = 0) | — | NA | — | 4 | ns |
| | | | Slave | — | 15 | — | 23 | |
| | | | Master (MTFE = 1, CPHA = 0) | — | 4 | — | 16 ¹ | |
| | | | Master (MTFE = 1, CPHA = 1) | — | 4 | — | 4 | |
| 12 | t_{HO} | Data hold time for outputs | Master (MTFE = 0) | NA | — | -2 | — | ns |

Table continues on the next page...

Table 32. DSPI electrical specifications (continued)

| No | Symbol | Parameter | Conditions | High Speed Mode | | low Speed mode | | Unit |
|----|--------|-----------|--------------------------------|-----------------|-----|-----------------|-----|------|
| | | | | Min | Max | Min | Max | |
| | | | Slave | 4 | — | 6 | — | |
| | | | Master (MTFE = 1, CPHA = 0) | -2 | — | 10 ¹ | — | |
| | | | Master (MTFE = 1, CPHA = 1) | -2 | — | -2 | — | |

1. SMPL_PTR should be set to 1

NOTE

Restriction For High Speed modes

- DSPI2, DSPI3, SPI1 and SPI2 will support 40MHz Master mode SCK
- DSPI2, DSPI3, SPI1 and SPI2 will support 25MHz Slave SCK frequency
- Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode
- For Master mode MTFE will be 1 for high speed mode
- For high speed slaves, their master have to be in MTFE=1 mode or should be able to support 15ns tSUO delay

NOTE

For numbers shown in the following figures, see [Table 32](#)

Table 33. Continuous SCK timing

| Spec | Characteristics | Pad Drive/Load | Value | |
|------|---------------------|----------------|---------|---------|
| | | | Minimum | Maximum |
| tSCK | SCK cycle timing | strong/50pf | 100ns | |
| | PCS valid after SCK | strong/50pf | | 15ns |
| | PCS valid after SCK | strong/50pf | -4ns | |

Table 34. DSPI high speed mode I/Os

| DSPI | High speed SCK | High speed SIN | High speed SOUT |
|-------|----------------|----------------|-----------------|
| DSPI2 | GPIO[78] | GPIO[76] | GPIO[77] |
| DSPI3 | GPIO[100] | GPIO[101] | GPIO[98] |
| SPI1 | GPIO[173] | GPIO[175] | GPIO[176] |
| SPI2 | GPIO[79] | GPIO[110] | GPIO[111] |

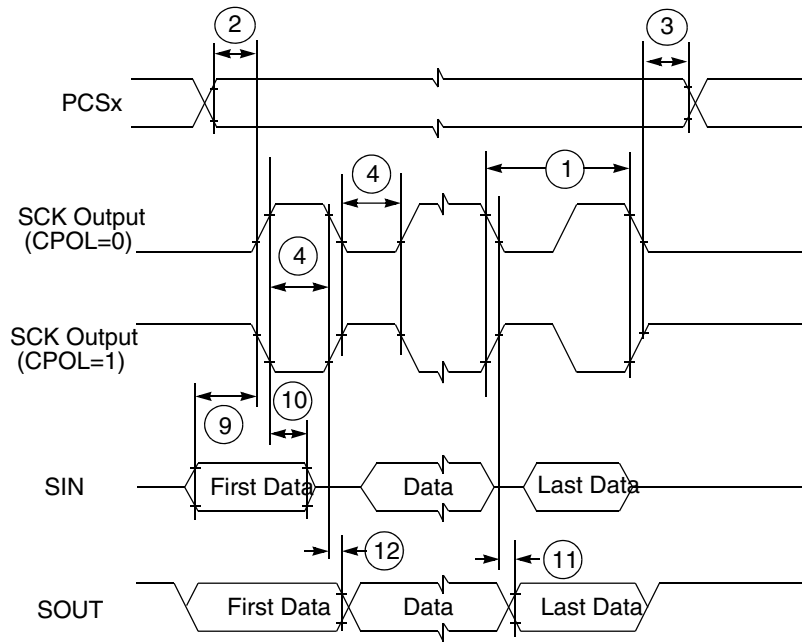


Figure 8. DSPI classic SPI timing — master, CPHA = 0

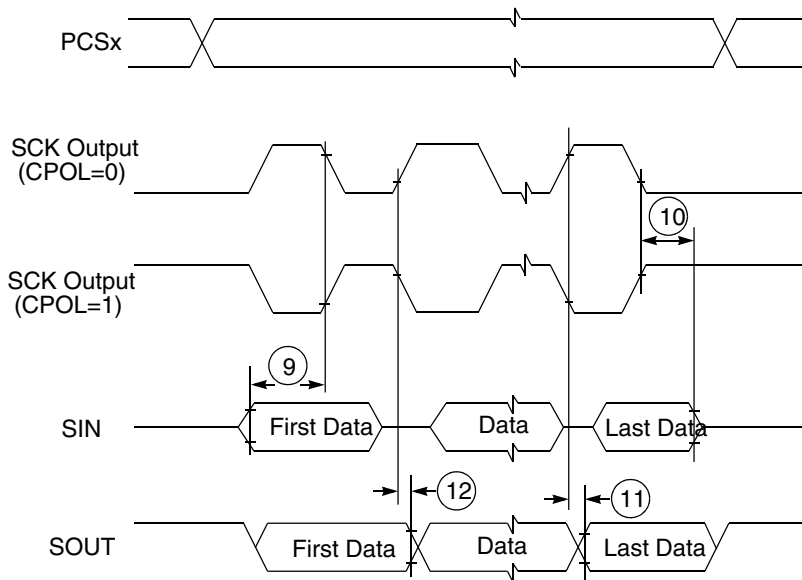


Figure 9. DSPI classic SPI timing — master, CPHA = 1

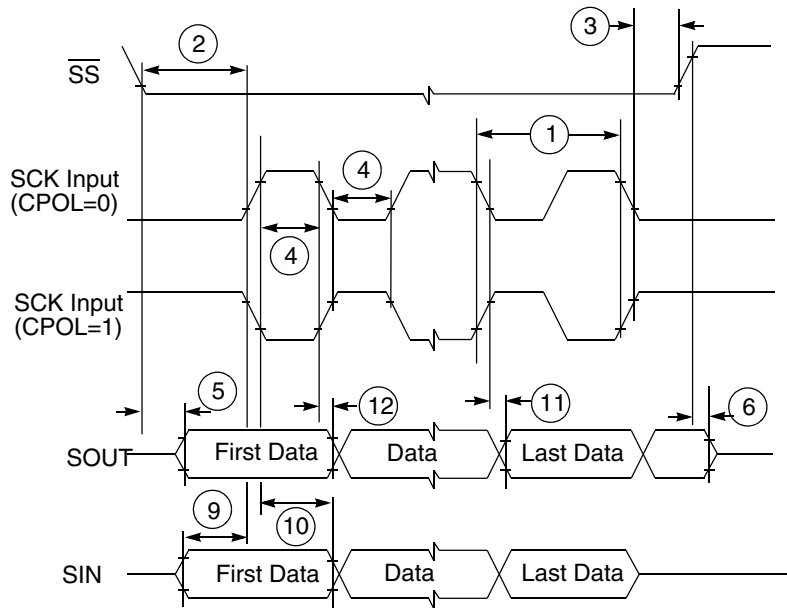


Figure 10. DSPI classic SPI timing — slave, CPHA = 0

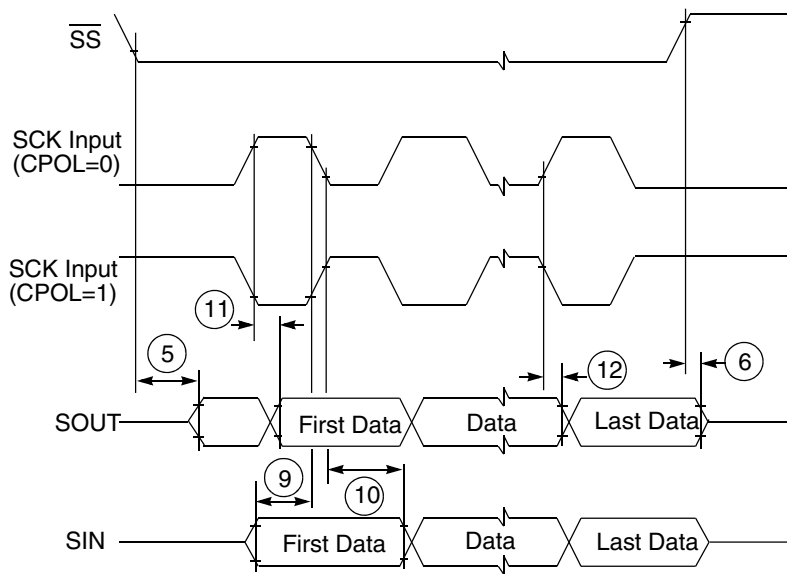


Figure 11. DSPI classic SPI timing — slave, CPHA = 1

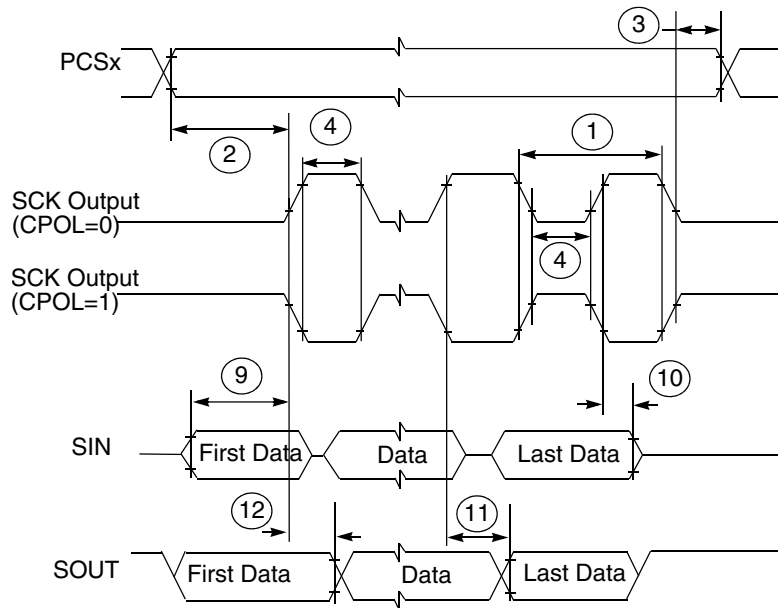


Figure 12. DSPI modified transfer format timing — master, CPHA = 0

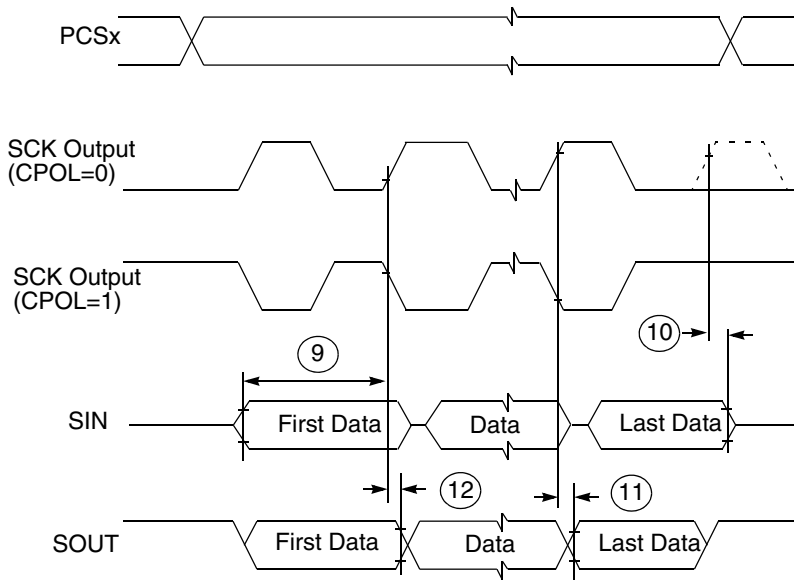


Figure 13. DSPI modified transfer format timing — master, CPHA = 1

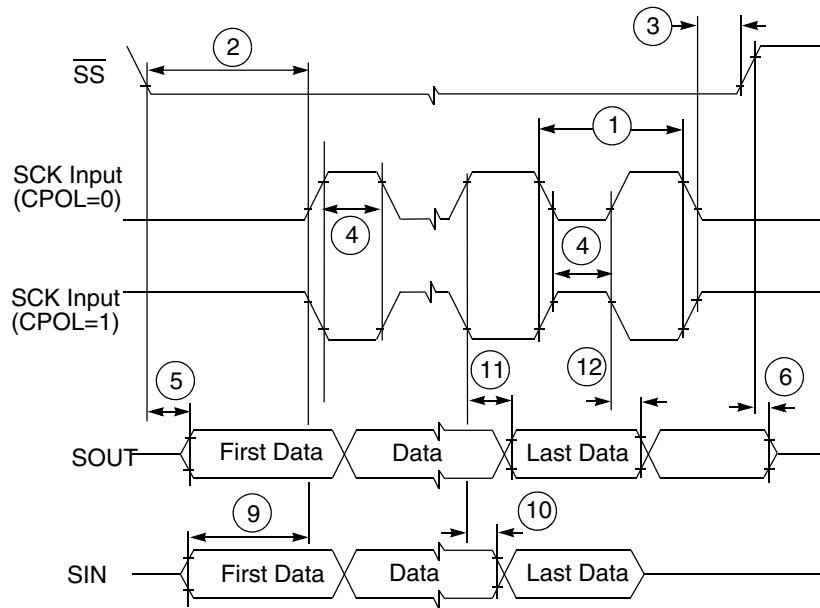


Figure 14. DSPI modified transfer format timing – slave, CPHA = 0

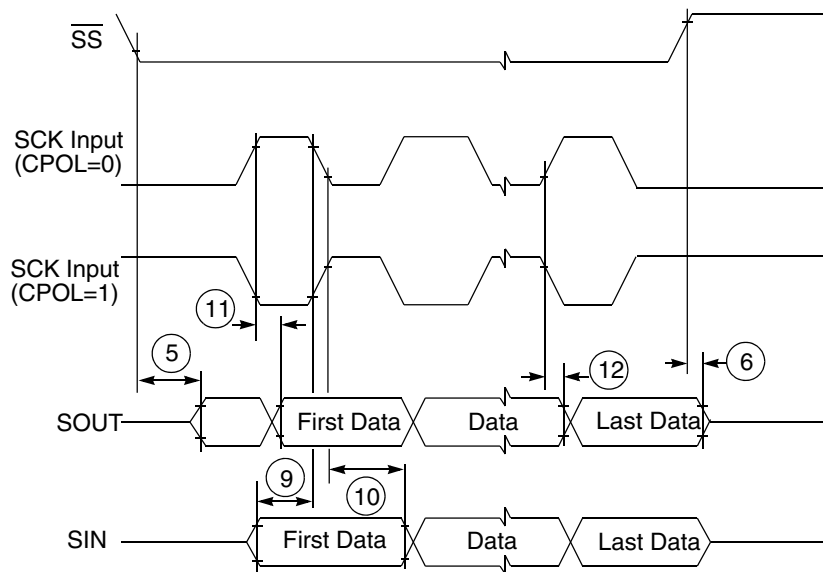


Figure 15. DSPI modified transfer format timing — slave, CPHA = 1

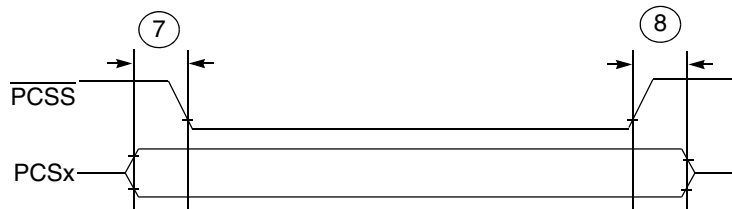


Figure 16. DSPI PCS strobe (PCSS) timing

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

6.4.2.2 TxEN

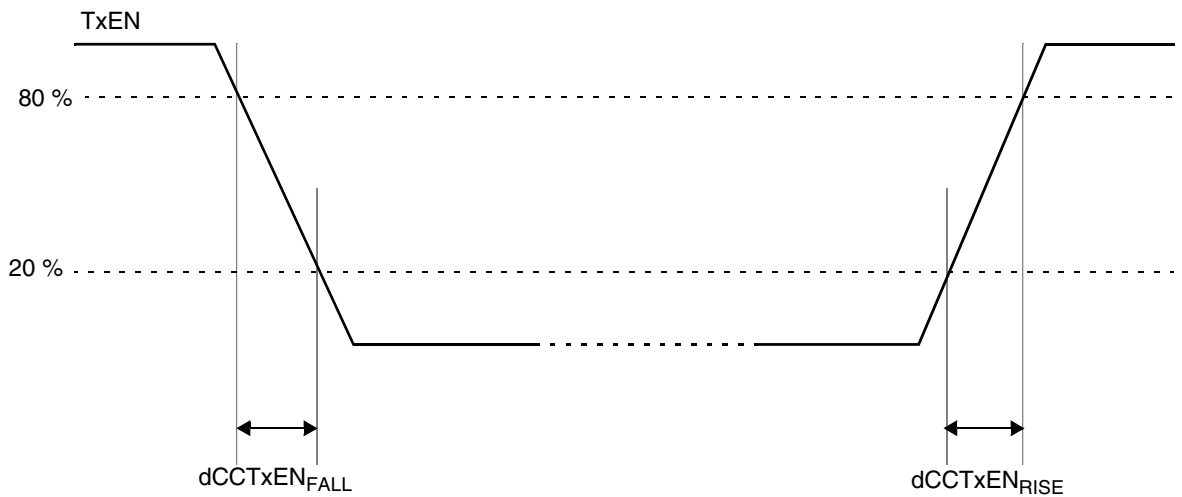


Figure 17. TxEN signal

Table 35. TxEN output characteristics¹

| Name | Description | Min | Max | Unit |
|--------------------|--|-----|-----|------|
| $dCCTxEN_{RISE25}$ | Rise time of TxEN signal at CC | | 9 | ns |
| $dCCTxEN_{FALL25}$ | Fall time of TxEN signal at CC | | 9 | ns |
| $dCCTxEN_{01}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | | 25 | ns |
| $dCCTxEN_{10}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | | 25 | ns |

1. All parameters specified for $V_{DD_HV_IOx} = 3.3\text{ V} -5\%, \pm 10\%$, $T_J = -40\text{ }^\circ\text{C} / 150\text{ }^\circ\text{C}$, TxEN pin load maximum 25 pF

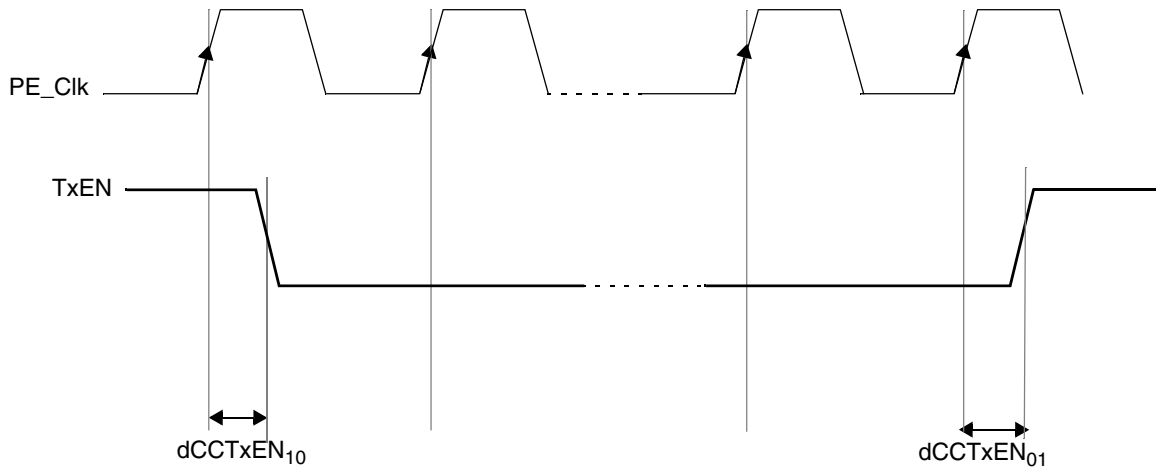


Figure 18. TxEN signal propagation delays

6.4.2.3 TxD

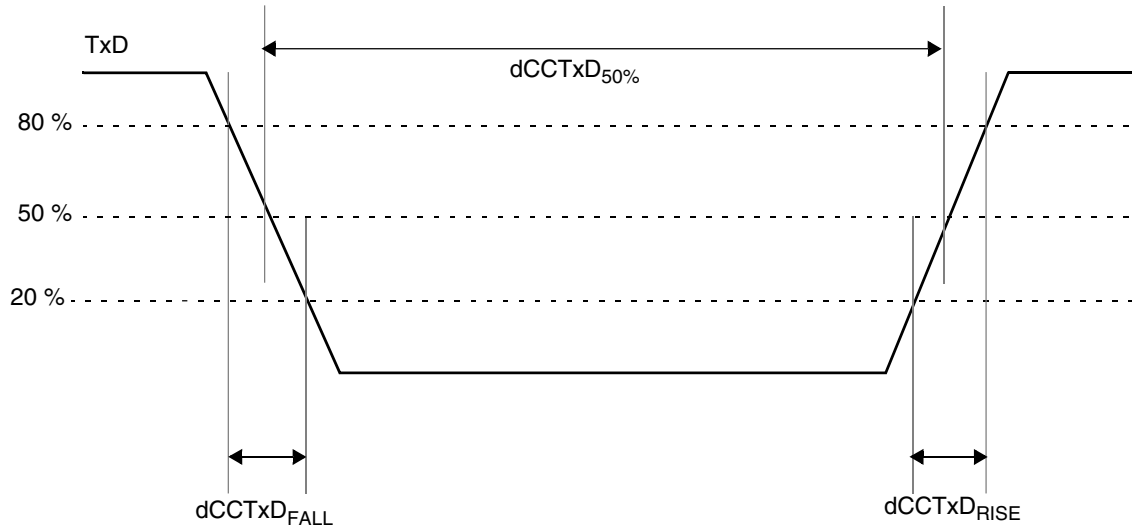


Figure 19. TxD Signal

Table 36. TxD output characteristics

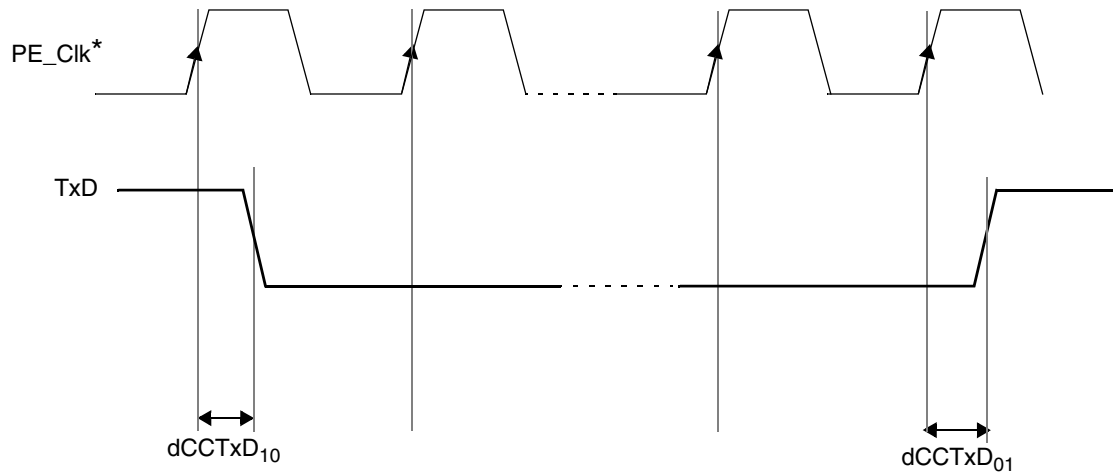
| Name | Description ¹ | Min | Max | Unit |
|--|--|-------|----------------|------|
| dCCT _{xAsym} | Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns) | -2.45 | 2.45 | ns |
| dCCTxD _{RISE25} +dCCTxD _{FALL25} | Sum of Rise and Fall time of TxD signal at the output | | 9 ² | ns |

Table continues on the next page...

Table 36. TxD output characteristics (continued)

| Name | Description ¹ | Min | Max | Unit |
|----------------------|--|-----|-----|------|
| dCCTxD ₀₁ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | | 25 | ns |
| dCCTxD ₁₀ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | | 25 | ns |

1. All parameters specified for $V_{DD_HV_IOx} = 3.3\text{ V} \pm 5\%, \pm 10\%$, $T_J = -40\text{ }^\circ\text{C} / 150\text{ }^\circ\text{C}$, TxD pin load maximum 25 pF.
2. For $3.3\text{ V} \pm 10\%$ operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 37. RxD input characteristic

| Name | Description ¹ | Min | Max | Unit |
|----------------------|---|-----|-----|------|
| C_CCRxD | Input capacitance on RxD pin | | 7 | pF |
| uCCLogic_1 | Threshold for detecting logic high | 35 | 70 | % |
| uCCLogic_0 | Threshold for detecting logic low | 30 | 65 | % |
| dCCRxD ₀₁ | Sum of delay from actual input to the D input of the first FF, rising edge | | 10 | ns |
| dCCRxD ₁₀ | Sum of delay from actual input to the D input of the first FF, falling edge | | 10 | ns |

1. All parameters specified for $VDD_HV_IOx = 3.3\text{ V} \pm 5\%$, $\pm 10\%$, $T_J = -40\text{ }^{\circ}\text{C} / 150\text{ }^{\circ}\text{C}$.

6.4.3 uSDHC specifications

Table 38. uSDHC switching specifications

| Num | Symbol | Description | Min. | Max. | Unit |
|---|------------------|---------------------------------------|------|------|------|
| Card input clock | | | | | |
| SD1 | fpp | Clock frequency (Identification mode) | 0 | 400 | kHz |
| | fpp | Clock frequency (SD\SDIO full speed) | 0 | 25 | MHz |
| | fpp | Clock frequency (SD\SDIO high speed) | 0 | 40 | MHz |
| | fpp | Clock frequency (MMC full speed) | 0 | 20 | MHz |
| | f _{OD} | Clock frequency (MMC full speed) | 0 | 40 | MHz |
| SD2 | t _{WL} | Clock low time | 7 | — | ns |
| SD3 | t _{WH} | Clock high time | 7 | — | ns |
| SD4 | t _{TLH} | Clock rise time | — | 3 | ns |
| SD5 | t _{THL} | Clock fall time | — | 3 | ns |
| SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD6 | t _{OD} | SDHC output delay (output valid) | -5 | 6.5 | ns |
| SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD7 | t _{ISU} | SDHC input setup time | 5 | — | ns |
| SD8 | t _{IH} | SDHC input hold time | 0 | — | ns |

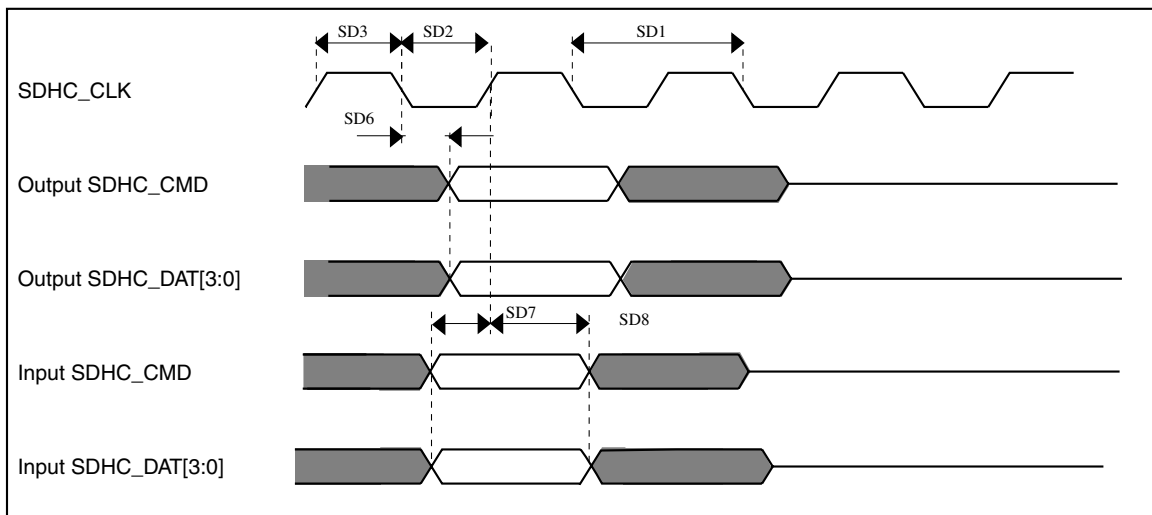


Figure 21. uSDHC timing

6.4.4 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.4.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

NOTE

ENET0 supports the following xMII interfaces: MII, MII_Lite and RMI. ENET1 supports the following xMII interfaces: MII_Lite.

NOTE

It is only possible to use ENET0 and ENET1 simultaneously when both are configured for MII_Lite.

NOTE

In certain pinout configurations ENET1 MII-Lite signals can be across multiple VDD_HV_A/B/C domains. If these configuration are used, VDD_HV IO domains need to be at the same voltage (for example: 3.3V)

Table 39. MII signal switching specifications

| Symbol | Description | Min. | Max. | Unit |
|--------|---------------------------------------|------|------|--------------|
| — | RXCLK frequency | — | 25 | MHz |
| MII1 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| MII2 | RXCLK pulse width low | 35% | 65% | RXCLK period |
| MII3 | RXD[3:0], RXDV, RXER to RXCLK setup | 5 | — | ns |
| MII4 | RXCLK to RXD[3:0], RXDV, RXER hold | 5 | — | ns |
| — | TXCLK frequency | — | 25 | MHz |
| MII5 | TXCLK pulse width high | 35% | 65% | TXCLK period |
| MII6 | TXCLK pulse width low | 35% | 65% | TXCLK period |
| MII7 | TXCLK to TXD[3:0], TXEN, TXER invalid | 2 | — | ns |
| MII8 | TXCLK to TXD[3:0], TXEN, TXER valid | — | 25 | ns |

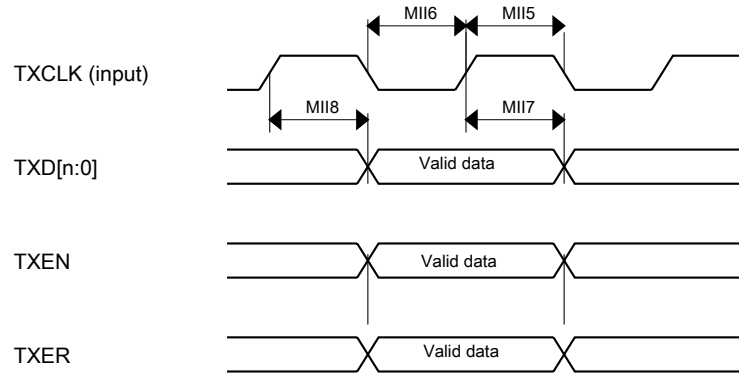


Figure 22. RMII/MII transmit signal timing diagram

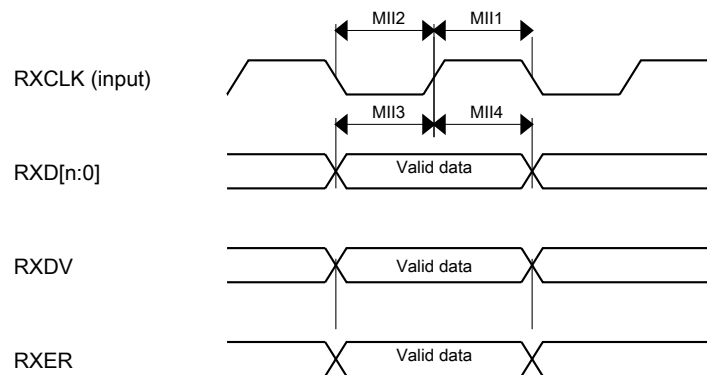


Figure 23. RMII/MII receive signal timing diagram

6.4.4.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 40. RMII signal switching specifications

| Num | Description | Min. | Max. | Unit |
|-------|---|------|------|-----------------|
| — | EXTAL frequency (RMII input clock RMII_CLK) | — | 50 | MHz |
| RMII1 | RMII_CLK pulse width high | 35% | 65% | RMII_CLK period |
| RMII2 | RMII_CLK pulse width low | 35% | 65% | RMII_CLK period |
| RMII3 | RXD[1:0], CRS_DV, RXER to RMII_CLK setup | 4 | — | ns |
| RMII4 | RMII_CLK to RXD[1:0], CRS_DV, RXER hold | 2 | — | ns |
| RMII7 | RMII_CLK to TXD[1:0], TXEN invalid | 4 | — | ns |
| RMII8 | RMII_CLK to TXD[1:0], TXEN valid | — | 15 | ns |

6.4.5 MediaLB (MLB) electrical specifications

6.4.5.1 MLB 3-pin interface DC characteristics

The section lists the MLB 3-pin interface electrical characteristics.

Table 41. MediaLB 3-Pin Interface Electrical DC Specifications

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|-----------------------------|----------|--------------------------|-----|----------|---------------|
| Maximum input voltage | — | — | — | 3.6 | V |
| Low level input threshold | V_{IL} | — | — | 0.7 | V |
| High level input threshold | V_{IH} | See Note ¹ | 1.8 | — | V |
| Low level output threshold | V_{OL} | $I_{OL} = -6 \text{ mA}$ | — | 0.4 | V |
| High level output threshold | V_{OH} | $I_{OH} = -6 \text{ mA}$ | 2.0 | — | V |
| Input leakage current | I_L | $0 < V_{in} < V_{DD}$ | — | ± 10 | μA |

- Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

6.4.5.2 MLB 3-pin interface electrical specifications

This section describes the timing electrical information of the MLB module.

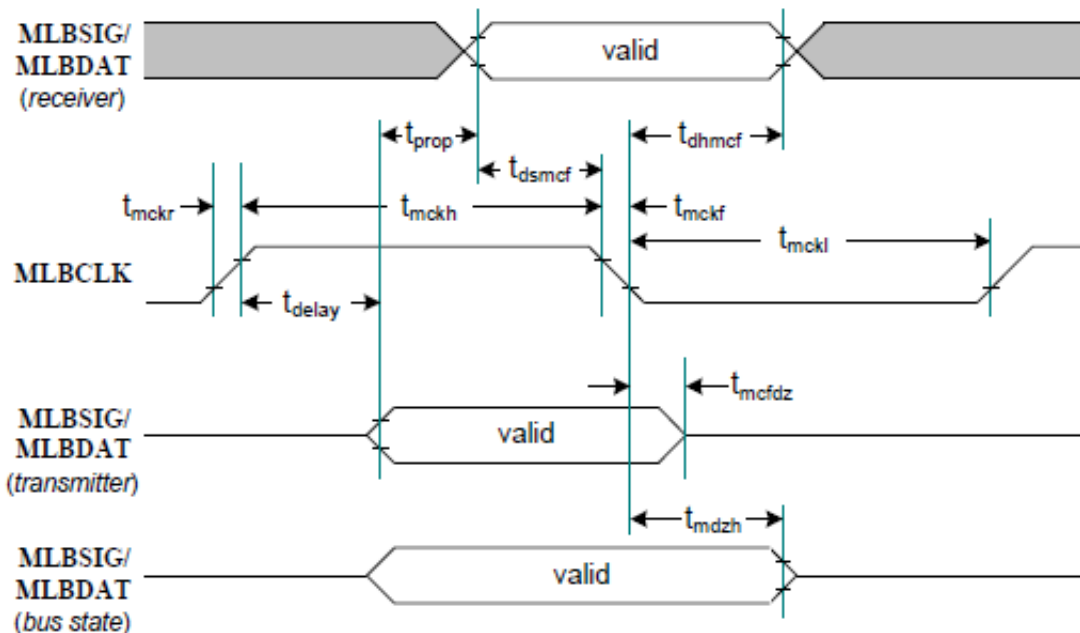


Figure 24. MediaLB 3-Pin Timing

Ground = 0.0 V; Load Capacitance = 60 pF, input transition= 1 ns ; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 42. MLB 3-Pin 256/512 Fs Timing Parameters

| Parameter | Symbol | Min | Max | Unit | Comment |
|--|-------------|-------------|------------|------|---|
| MLBCLK operating frequency | f_{mck} | 11.264 | 25.6 | MHz | 256xFs at 44.0 kHz, 512xFs at 50.0 kHz |
| MLBCLK rise time | t_{mckr} | | 3 | ns | V_{IL} to V_{IH} |
| MLBCLK fall time | t_{mckf} | | 3 | ns | V_{IH} to V_{IL} |
| MLBCLK low time ¹ | t_{mckl} | 30 14 | — | ns | 256xFs 512xFs |
| MLBCLK high time | t_{mckh} | 30 14 | — | ns | 256xFs 512xFs |
| MLBSIG/MLBDAT receiver input setup to MLBCLK falling | t_{dsmcf} | 1 | — | ns | — |
| MLBSIG/MLBDAT receiver input hold from MLBCLK low | t_{dhmcf} | t_{mcfdz} | — | ns | — |
| MLBSIG/MLBDAT output valid from MLBCLK low | t_{mcfdz} | 0 | t_{mckl} | ns | 2 |
| Bus output hold from MLBCLK low | t_{mdzh} | 4 | — | ns | 2 |

1. MLBCLK low/high time includes the pluse width variation.
2. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 43. MLB 3-Pin 1024 Fs Timing Parameters

| Parameter | Symbol | Min | Max | Unit | Comment |
|--|-------------|-------------|------------|------------|--|
| MLBCLK Operating Frequency ¹ | f_{mck} | 45.056 - | - 51.2 | MHz MHz | 1024 x fs at 44.0 kHz 1024 x fs at 50.0 kHz |
| MLBCLK rise time | f_{mckr} | | 1 | ns | V_{IL} to V_{IH} |
| MLBCLK fall time | f_{mckf} | | 1 | ns | V_{IH} to V_{IL} |
| MLBCLK low time | t_{mckl} | 6.1 | — | ns | 2 |
| MLBCLK high time | t_{mckh} | 9.3 | — | ns | 2 |
| MLBSIG/MLBDAT receiver input setup to MLBCLK falling | t_{dsmcf} | 1 | — | ns | |
| MLBSIG/MLBDAT receiver input hold from MLBCLK low | t_{dhmcf} | t_{mcfdz} | — | ns | |
| MLBSIG/MLBDAT output valid from MLBCLK low | t_{mcfdz} | 0 | t_{mckl} | ns | 3 |
| Bus Hold from MLBCLK low | t_{mdzh} | 2 | — | ns | 3 |

USB electrical specifications

1. The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.
2. MLBCLK low/high time includes the pluse width variation.
3. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for tmdzh. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

6.4.6 USB electrical specifications

6.4.6.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

6.4.6.2 ULPI timing specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in the following table. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin.

Table 44. ULPI timing specifications

| Num | Description | Min. | Typ. | Max. | Unit |
|-----|---------------------------------|------|-------|------|------|
| | USB_CLKIN operating frequency | — | 60 | — | MHz |
| | USB_CLKIN duty cycle | — | 50 | — | % |
| U1 | USB_CLKIN clock period | — | 16.67 | — | ns |
| U2 | Input setup (control and data) | 5 | — | — | ns |
| U3 | Input hold (control and data) | 1 | — | — | ns |
| U4 | Output valid (control and data) | — | — | 9.5 | ns |
| U5 | Output hold (control and data) | 1 | — | — | ns |

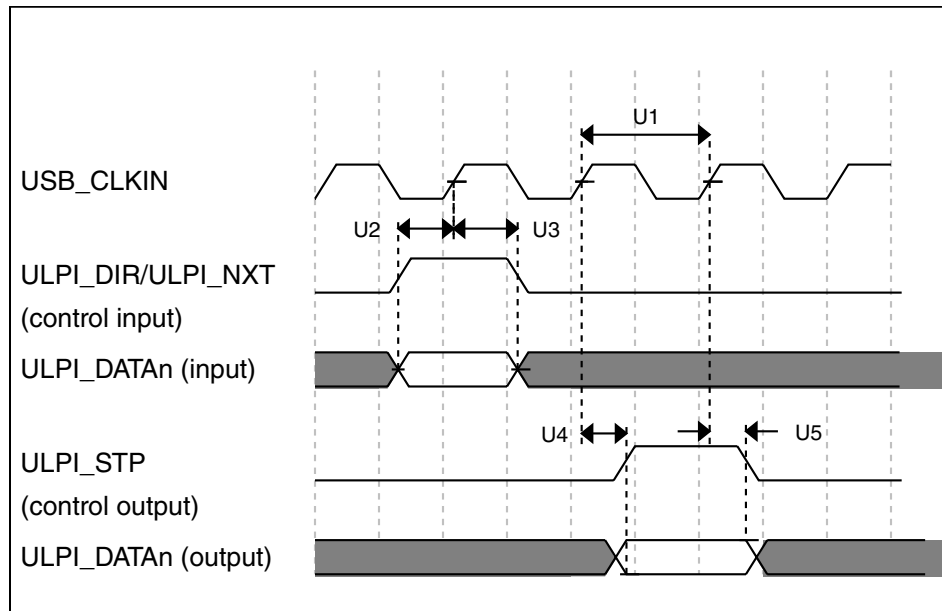


Figure 25. ULPI timing diagram

6.4.7 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 45. Master mode SAI Timing

| no | Parameter | Value | | Unit |
|-----|--|-------|-----|-------------|
| | | Min | Max | |
| | Operating Voltage | 2.7 | 3.6 | V |
| S1 | SAI_MCLK cycle time | 40 | - | ns |
| S2 | SAI_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | SAI_BCLK cycle time | 80 | - | BCLK period |
| S4 | SAI_BCLK pulse width high/low | 45% | 55% | ns |
| S5 | SAI_BCLK to SAI_FS output valid | - | 15 | ns |
| S6 | SAI_BCLK to SAI_FS output invalid | 0 | - | ns |
| S7 | SAI_BCLK to SAI_TXD valid | - | 15 | ns |
| S8 | SAI_BCLK to SAI_TXD invalid | 0 | - | ns |
| S9 | SAI_RXD/SAI_FS input setup before SAI_BCLK | 28 | - | ns |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK | 0 | - | ns |

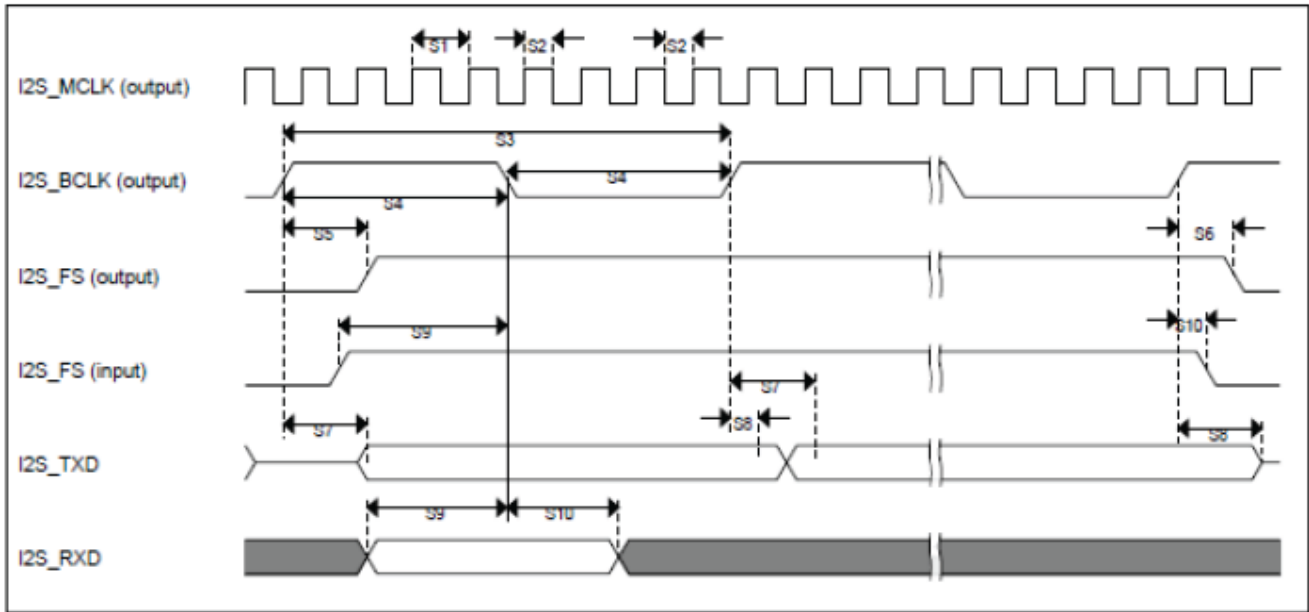


Figure 26. Master mode SAI Timing

Table 46. Slave mode SAI Timing

| No | Parameter | Value | | Unit |
|-----|---|-------|-----|-------------|
| | | Min | Max | |
| | Operating Voltage | 2.7 | 3.6 | V |
| S11 | SAI_BCLK cycle time (input) | 80 | - | ns |
| S12 | SAI_BCLK pulse width high/low (input) | 45% | 55% | BCLK period |
| S13 | SAI_FS input setup before SAI_BCLK | 10 | - | ns |
| S14 | SAI_FS input hold after SAI_BCLK | 2 | - | ns |
| S15 | SAI_BCLK to SAI_TXD/SAI_FS output valid | - | 28 | ns |
| S16 | SAI_BCLK to SAI_TXD/SAI_FS output invalid | 0 | - | ns |
| S17 | SAI_RXD setup before SAI_BCLK | 10 | - | ns |
| S18 | SAI_RXD hold after SAI_BCLK | 2 | - | ns |

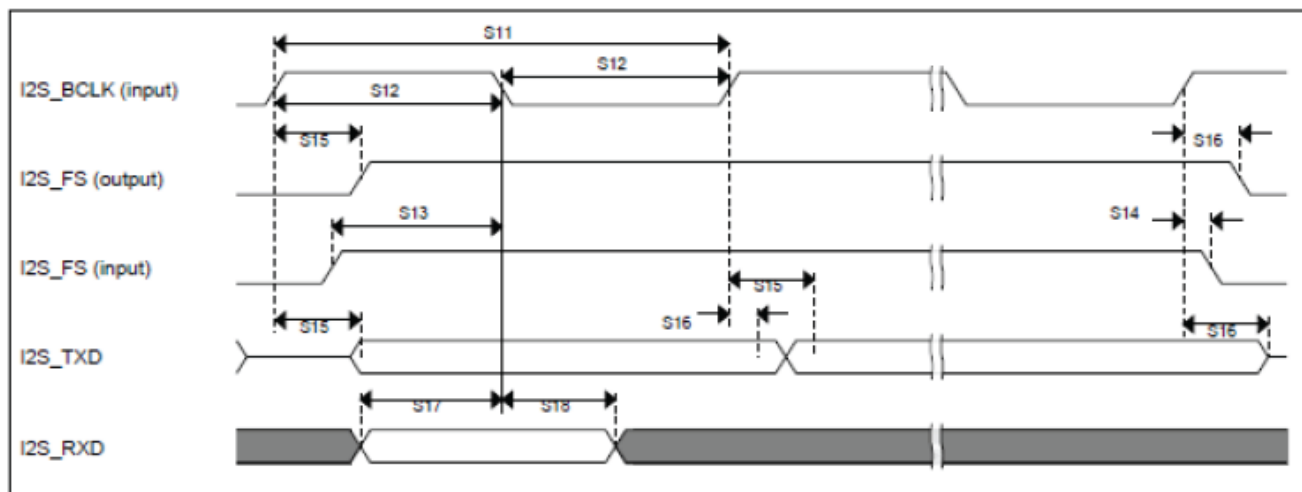


Figure 27. Slave mode SAI Timing

6.5 Debug specifications

6.5.1 JTAG interface timing

 Table 47. JTAG pin AC electrical characteristics ¹

| # | Symbol | Characteristic | Min | Max | Unit |
|----|----------------------|--|------|------------------|------|
| 1 | t_{JCYC} | TCK Cycle Time ² | 62.5 | — | ns |
| 2 | t_{JDC} | TCK Clock Pulse Width | 40 | 60 | % |
| 3 | $t_{TCKRISE}$ | TCK Rise and Fall Times (40% - 70%) | — | 3 | ns |
| 4 | t_{TMSS}, t_{TDIS} | TMS, TDI Data Setup Time | 5 | — | ns |
| 5 | t_{TMSH}, t_{TDIH} | TMS, TDI Data Hold Time | 5 | — | ns |
| 6 | t_{TDOV} | TCK Low to TDO Data Valid | — | 20 ³ | ns |
| 7 | t_{TDOI} | TCK Low to TDO Data Invalid | 0 | — | ns |
| 8 | t_{TDOHZ} | TCK Low to TDO High Impedance | — | 15 | ns |
| 11 | t_{BSDV} | TCK Falling Edge to Output Valid | — | 600 ⁴ | ns |
| 12 | t_{BSDVZ} | TCK Falling Edge to Output Valid out of High Impedance | — | 600 | ns |
| 13 | t_{BSDHZ} | TCK Falling Edge to Output High Impedance | — | 600 | ns |
| 14 | t_{BSDST} | Boundary Scan Input Valid to TCK Rising Edge | 15 | — | ns |
| 15 | t_{BSDHT} | TCK Rising Edge to Boundary Scan Input Invalid | 15 | — | ns |

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

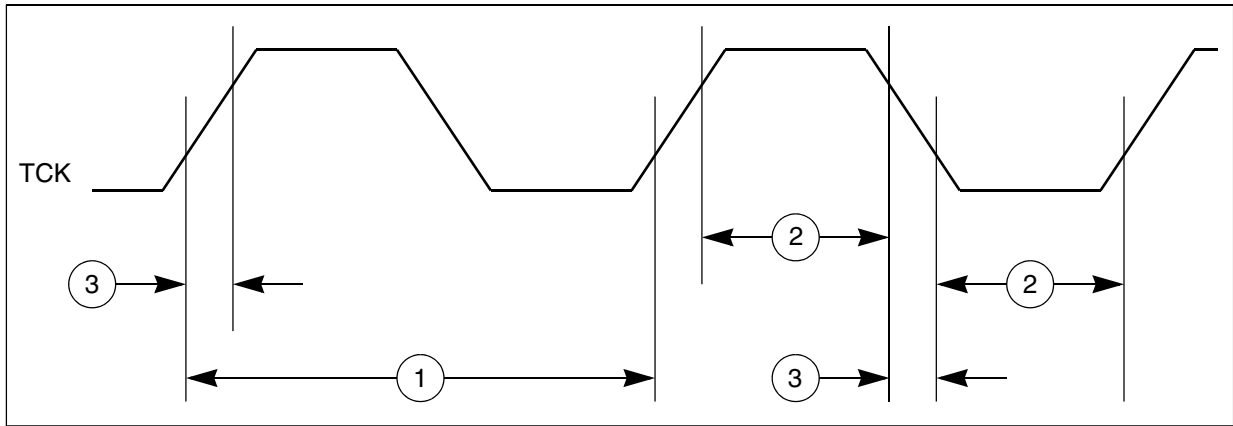


Figure 28. JTAG test clock input timing

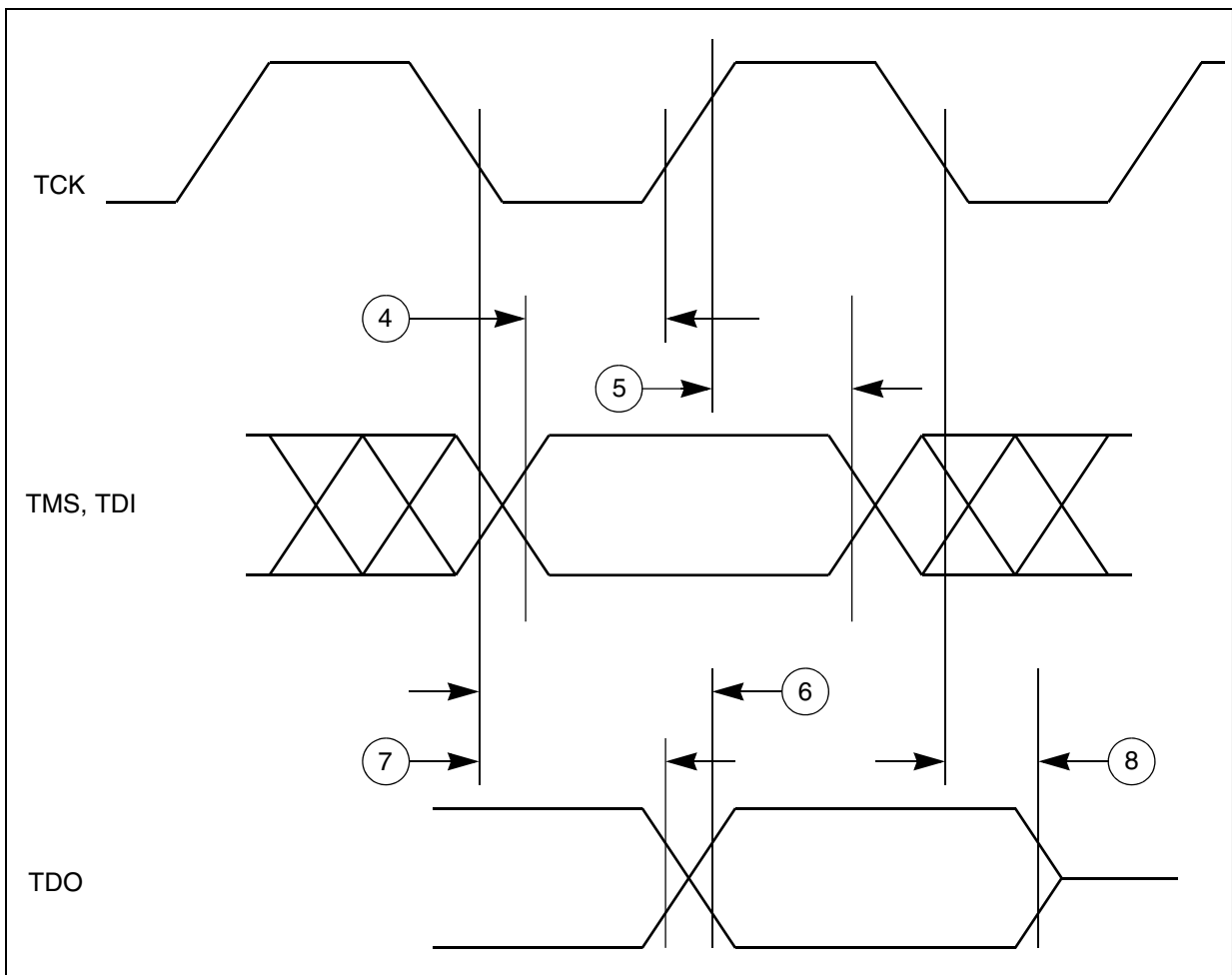


Figure 29. JTAG test access port timing

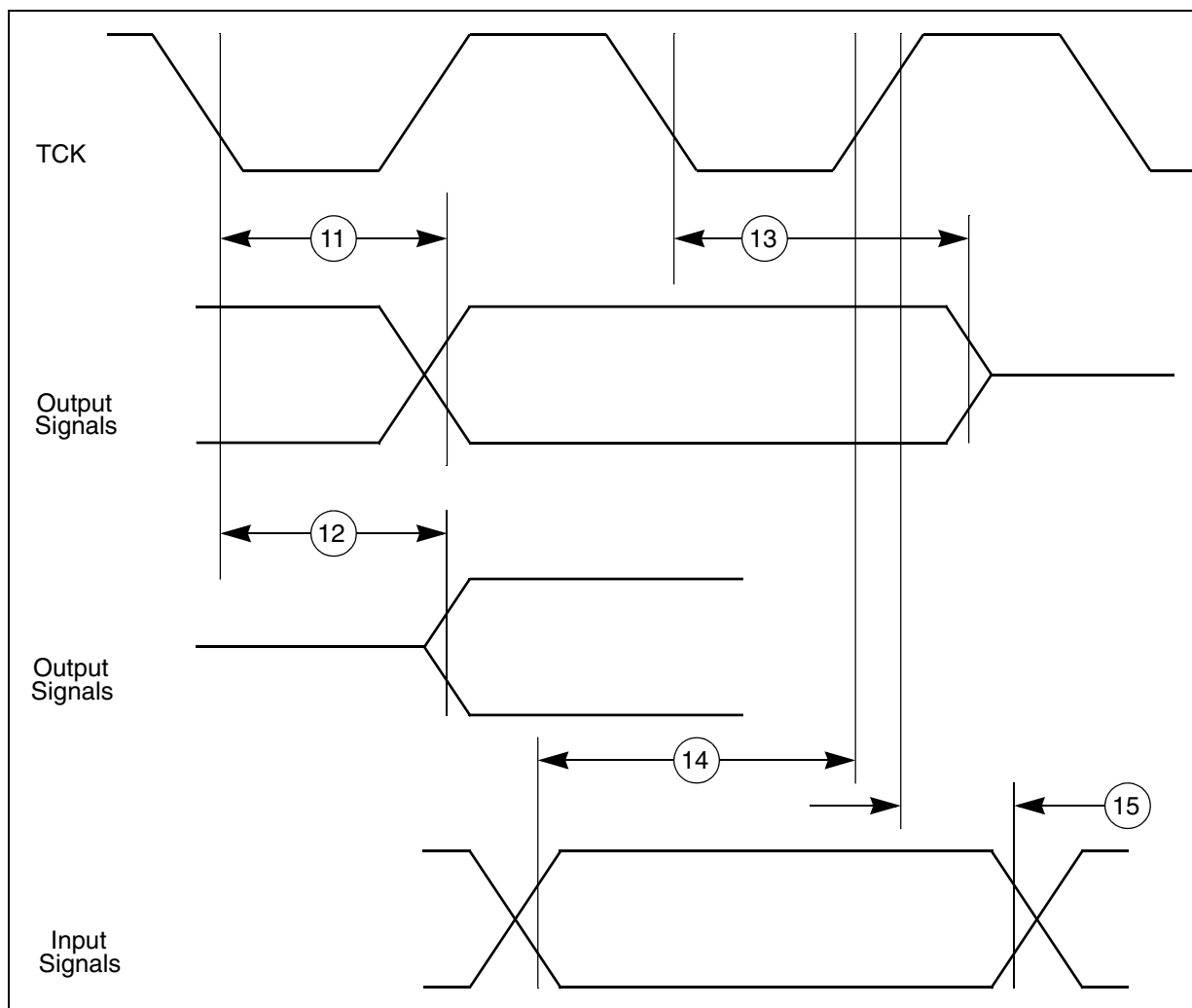


Figure 30. JTAG boundary scan timing

6.5.2 Nexus timing

Table 48. Nexus debug port timing ¹

| No. | Symbol | Parameter | Condition s | Min | Max | Unit |
|-----|------------------------------|---|-------------|------|------|------------|
| 1 | t_{MCCY} | MCKO Cycle Time | — | 15.6 | — | ns |
| 2 | t_{MDC} | MCKO Duty Cycle | — | 40 | 60 | % |
| 3 | t_{MDOV} | MCKO Low to MDO, MSEO, EVTO Data Valid ² | — | -0.1 | 0.25 | t_{MCCY} |
| 4 | t_{EVTIPW} | EVTI Pulse Width | — | 4 | — | t_{TCYC} |
| 5 | t_{EVTOPW} | EVTO Pulse Width | — | 1 | — | t_{MCCY} |
| 6 | t_{TCYC} | TCK Cycle Time ³ | — | 62.5 | — | ns |
| 7 | t_{TDC} | TCK Duty Cycle | — | 40 | 60 | % |
| 8 | t_{NTDIS} , t_{NTMSS} | TDI, TMS Data Setup Time | — | 8 | — | ns |

Table continues on the next page...

Table 48. Nexus debug port timing ¹ (continued)

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|-----|------------------------------|-------------------------------|------------|-----|-----|------|
| 9 | t_{NTDIH} , t_{NTMSH} | TDI, TMS Data Hold Time | — | 5 | — | ns |
| 10 | t_{JOV} | TCK Low to TDO/RDY Data Valid | — | 0 | 25 | ns |

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, \overline{MSEO} , and \overline{EVTO} data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

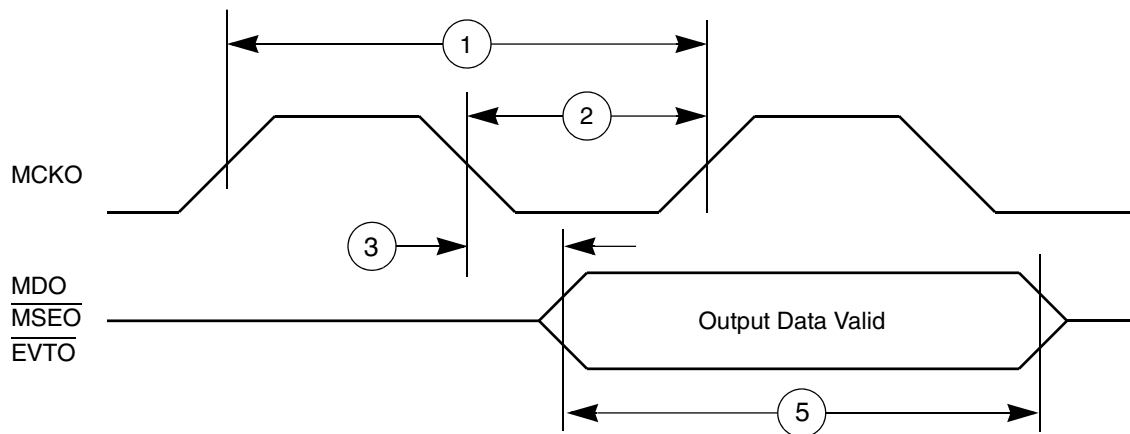


Figure 31. Nexus output timing

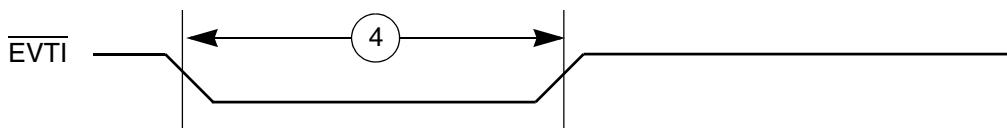


Figure 32. Nexus EVTI Input Pulse Width

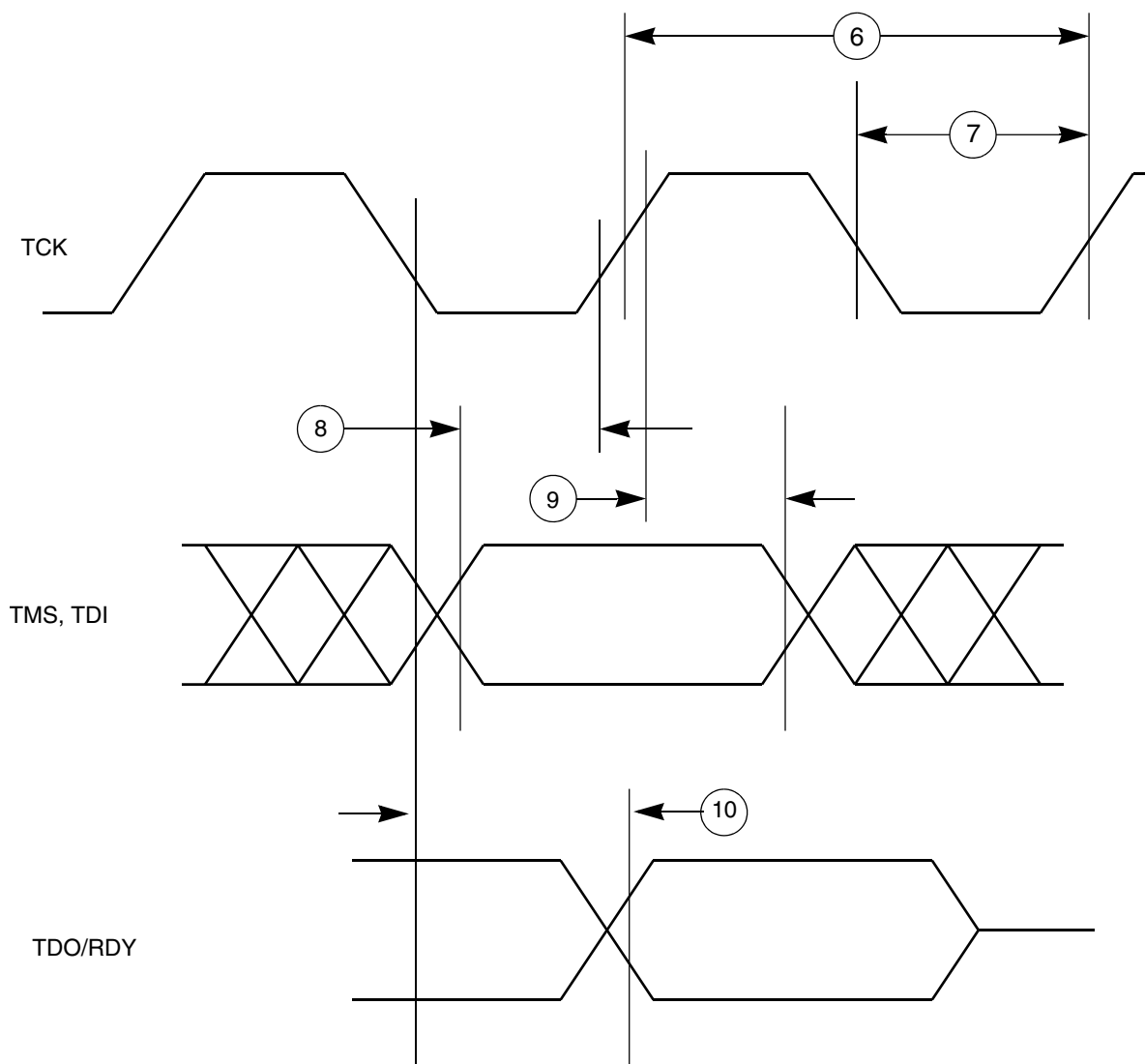


Figure 33. Nexus TDI, TMS, TDO timing

6.5.3 WKPU/NMI timing

Table 49. WKPU/NMI glitch filter

| No. | Symbol | Parameter | Min | Typ | Max | Unit |
|-----|--------------|----------------------------------|-----|-----|-----|------|
| 1 | W_{FNMI} | NMI pulse width that is rejected | — | — | 20 | ns |
| 2 | $W_{NFNMI}D$ | NMI pulse width that is passed | 400 | — | — | ns |

6.5.4 External interrupt timing (IRQ pin)

Table 50. External interrupt timing specifications

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|-----|------------|-----------------------|------------|-----|-----|-----------|
| 1 | t_{IPWL} | IRQ pulse width low | — | 3 | — | t_{CYC} |
| 2 | t_{IPWH} | IRQ pulse width high | — | 3 | — | t_{CYC} |
| 3 | t_{ICYC} | IRQ edge to edge time | — | 6 | — | t_{CYC} |

These values applies when IRQ pins are configured for rising edge or falling edge events, but not both.

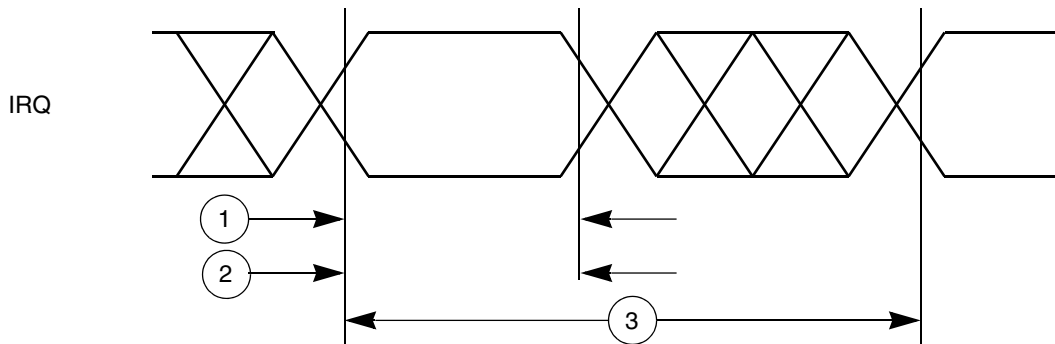


Figure 34. External interrupt timing

7 Thermal attributes

7.1 Thermal attributes

| Board type | Symbol | Description | 176LQFP | Unit | Notes |
|-------------------|------------------------|--|---------|---------------|-------|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 45 | $^{\circ}C/W$ | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 22 | $^{\circ}C/W$ | 1, 3 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 36 | $^{\circ}C/W$ | 1,3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 16 | $^{\circ}C/W$ | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 11 | $^{\circ}C/W$ | 4 |
| — | $R_{\theta JCTop}$ | Thermal resistance, junction to case top | 8 | $^{\circ}C/W$ | 5 |
| — | $R_{\theta JCbotttom}$ | Thermal resistance, junction to case bottom | 0.5 | $^{\circ}C/W$ | 6 |

Table continues on the next page...

| Board type | Symbol | Description | 176LQFP | Unit | Notes |
|------------|-------------|---|---------|------|-------|
| — | Ψ_{JT} | Thermal characterization parameter, junction to package top | 1 | °C/W | 7 |

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
- Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
- Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

| Board type | Symbol | Description | 324 MAPBGA | Unit | Notes |
|-------------------|------------------|--|------------|------|-------|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 25.5 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 19.0 | °C/W | 1,23 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 18.1 | °C/W | 1, 3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 14.8 | °C/W | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 10.4 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 8.4 | °C/W | 5 |
| — | Ψ_{JT} | Thermal characterization parameter, junction to package top (natural convection) | 0.45 | °C/W | 6 |
| — | Ψ_{JB} | Thermal characterization parameter, junction to package bottom center (natural convection) | 2.65 | °C/W | 7 |

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
- Per JEDEC JESD51-6 with the board horizontal
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
- Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Dimensions

| Board type | Symbol | Description | 256 MAPBGA | Unit | Notes |
|-------------------|------------------|---|------------|------|-------|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 29.4 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 19.3 | °C/W | 1,2,3 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 21.4 | °C/W | 1,3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 14.8 | °C/W | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 11 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 9.5 | °C/W | 5 |
| — | Ψ_{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | 0.5 | °C/W | 6 |
| — | Ψ_{JB} | Thermal characterization parameter, junction to package bottom center (natural convection) | 2.8 | °C/W | 7 |

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
- Per JEDEC JESD51-6 with the board horizontal
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
- Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

| Package | Freescale Document Number |
|-----------------|---------------------------|
| 176-pin LQFP-EP | 98ASA00673D |
| 256 MAPBGA | 98ASA00346D |
| 324 MAPBGA | 98ASA10582D |

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1 Reset sequence duration

[Table 51](#) specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in [Reset sequence description](#).

Table 51. RESET sequences

| No. | Symbol | Parameter | T _{Reset} | | | Unit |
|-----|-------------------|--|--------------------|------------------|-----|------|
| | | | Min | Typ ¹ | Max | |
| 1 | T _{DRB} | Destructive Reset Sequence, BIST enabled | 5.730 | 7.796 | | ms |
| 2 | T _{DR} | Destructive Reset Sequence, BIST disabled | 0.111 | 0.182 | | ms |
| 3 | T _{ERLB} | External Reset Sequence Long, Unsecure Boot | 5.729 | 7.793 | | ms |
| 4 | T _{FRL} | Functional Reset Sequence Long, Unsecure Boot | 0.110 | 0.179 | | ms |
| 5 | T _{FRS} | Functional Reset Sequence Short, Unsecure Boot | 0.004 | 0.005 | | ms |

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

10.2 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in [Table 51](#).

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

Reset sequence

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in [Table 51](#) are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

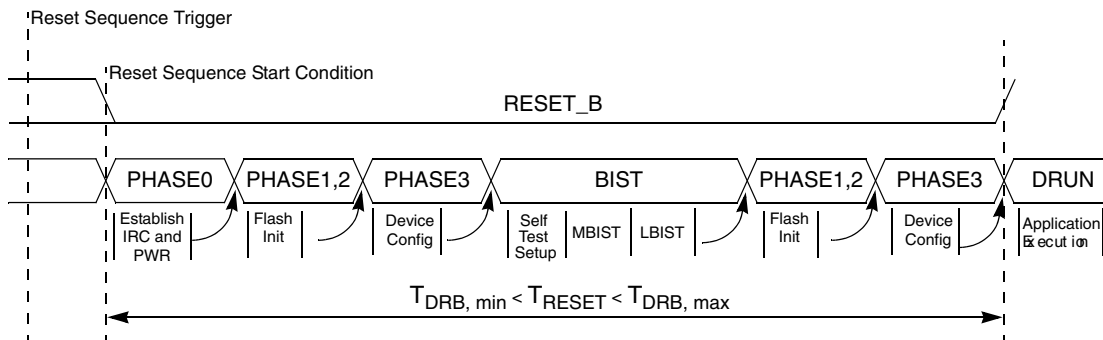


Figure 35. Destructive reset sequence, BIST enabled

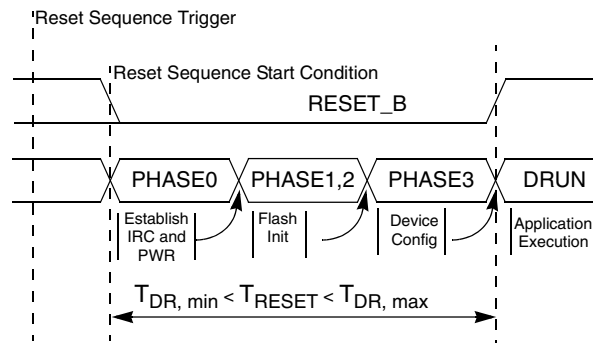


Figure 36. Destructive reset sequence, BIST disabled

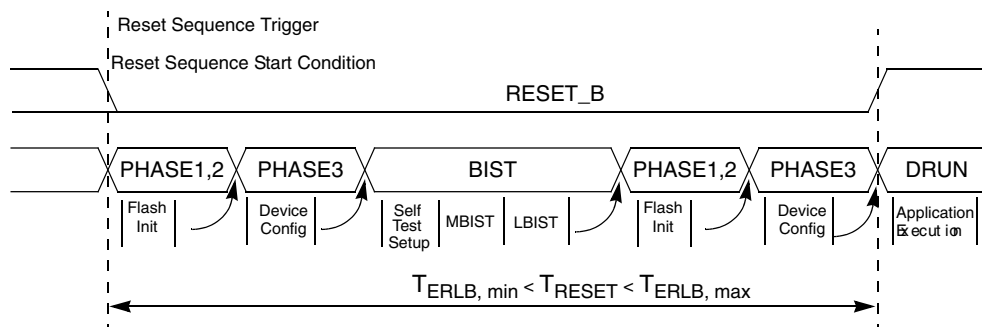


Figure 37. External reset sequence long, BIST enabled

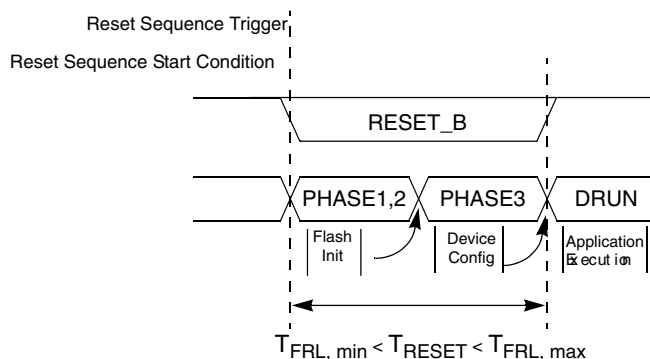


Figure 38. Functional reset sequence long

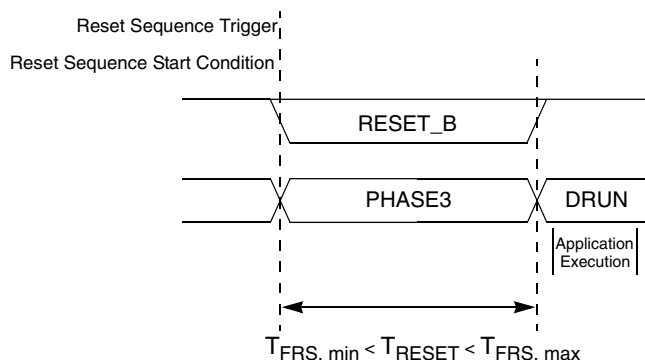


Figure 39. Functional reset sequence short

The reset sequences shown in [Figure 38](#) and [Figure 39](#) are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

The following table provides a revision history for this document.

Table 52. Revision History

| Rev. No. | Date | Substantial Changes |
|----------|---------------|--|
| 1 | 14 March 2013 | Initial Release |
| 1.1 | 16 May 2013 | Updated Pinouts section |
| 2 | 22 May 2014 | <ul style="list-style-type: none"> • Removed Category (SR, CC, P, T, D, B) column from all the table of the Datasheet • Revised the feature list. • Revised Introduction section to remove classification information. • Updated optional information in the ordering information figure. • Revised Absolute maximum rating section: <ul style="list-style-type: none"> • Removed category column from table • Added footnote at Ta • Revised Recommended operating conditions section <ul style="list-style-type: none"> • Added notes • Updated table: Recommended operating conditions (VDD_HV_x = 3.3 V) • Updated table: Recommended operating conditions (VDD_HV_x = 5 V) • Revised Voltage regulator electrical characteristics <ul style="list-style-type: none"> • Updated text describing bipolar transistors • Updated figure: Voltage regulator capacitance connection • Updated table: Voltage regulator electrical specifications • Removed Brownout information • Revised Voltage monitor electrical characteristics table |
| | | <ul style="list-style-type: none"> • Revised Supply current characteristics section <ul style="list-style-type: none"> • Updated table: Current consumption characteristics • Updated table: Low Power Unit (LPU) Current consumption characteristics • STANDBY Current consumption characteristics • Revised Electromagnetic Interference (EMI) characteristics section • Revised DC electrical specifications @ 3.3V Range table for naming conventions. • Revised DC electrical specifications @ 5 V Range table for naming conventions • Deleted MLB 6-pin Electrical Specifications • Removed PORST characteristics from Functional reset pad electrical characteristics table • Added section PORST electrical characteristics • Revised Input impedance and ADC accuracy section to remove SNR, THD, SINAD, ENOB, • Revised 32 kHz oscillator electrical specifications table to remove 'Vpp' row. • Updated 16 MHz RC Oscillator electrical specifications table for statuptime, cycle to cycle jitter, and lonf term jitter • Updated 128 KHz Internal RC oscillator electrical specifications table. • Updated PLL electrical specifications table • Added Jitter Calculation table • Added Percentage of Sample exceeding specified value of jitter table |
| | | <ul style="list-style-type: none"> • Revised Memory interfaces section • Revised Communication interfaces section <ul style="list-style-type: none"> • Updated note • Added Continuous SCK timing table • Added DSPi high speed mode I/Os table • Updated input transition value in section MLB 3-pin interface electrical specifications • Deleted MLB 6-pin interface DC characteristics section • Deleted MLB 6-pin interface AC characteristics section • Updated JTAG pin AC electrical characteristics table • Revised table under Thermal attributes section • Updated Obtaining package dimensions section for Freescale Document numbers |
| 3 | 12 May 2015 | <ul style="list-style-type: none"> • Editorial updates throughout the sections • Renamed '176 LQFP' package to '176 LQFP-EP' • Added following sections: |

Table continues on the next page...

Table 52. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|----------|------|---|
| | | <ul style="list-style-type: none"> • Block diagram • Family comparison • Ordering Information • In table: Absolute maximum ratings as follows: <ul style="list-style-type: none"> • Removed row for symbol: 'V_{SS_HV}' • Added symbol: 'V_{DD_LV}' • Updated 'Max' column for symbol 'V_{INA}' • Added footnote to 'Conditions' column • Removed footnote from 'Max' column • In section: Recommended operating conditions <ul style="list-style-type: none"> • Added opening text: "The following table describes the operating conditions ... " • Added note: "V_{DD_HV_A}, V_{DD_HV_B} and V_{DD_HV_C} are all ... " • In table: Recommended operating conditions (V_{DD_HV_x} = 3.3 V) <ul style="list-style-type: none"> • Added footnote to 'Conditions' column • Updated footnote for 'Min' column • Removed footnote from symbols 'V_{DD_HV_A}', 'V_{DD_HV_B}', and 'V_{DD_HV_C}' • Removed row for symbol: 'V_{SS_HV}' • Updated 'Parameter' column for symbol 'V_{DD_HV_FLTA}', 'V_{DD_HV_ADC1_REF}', 'V_{DD_LV}' • Updated 'Min' column for symbol 'V_{DD_HV_ADC0}' and 'V_{DD_HV_ADC1}' • Updated 'Parameter' 'Min' 'Max' column for symbol 'V_{SS_HV_ADC0}' and 'V_{SS_HV_ADC1}' • Added footnote to symbol 'V_{DD_LV}' • Removed footnote from symbol 'V_{IN1_CMP_REF}' • Removed row for symbol 'V_{SS_LV}' • Removed footnote from 'Max' column of symbols 'V_{DD_HV_ADC0}' and 'V_{DD_HV_ADC1}' |
| | | <ul style="list-style-type: none"> • In section: Recommended operating conditions <ul style="list-style-type: none"> • In table: Recommended operating conditions (V_{DD_HV_x} = 5 V) <ul style="list-style-type: none"> • Added footnote to 'Conditions' column • Updated footnote for 'Min' column • Removed footnote from symbols 'V_{DD_HV_A}', 'V_{DD_HV_B}', and 'V_{DD_HV_C}' • Removed row for symbol: 'V_{SS_HV}' • Updated 'Parameter' column for symbol 'V_{DD_HV_ADC1_REF}' • Updated 'Min' column of symbol 'V_{DD_HV_ADC0}' and 'V_{DD_HV_ADC1}' • Updated 'Parameter', 'Min' 'Max' column for symbol 'V_{SS_HV_ADC0}' and 'V_{SS_HV_ADC1}' • Added footnote to symbol 'V_{DD_LV}' • Removed row for symbol 'V_{SS_LV}' • Added row for symbol 'V_{IN1_CMP_REF}' and corresponding footnotes to the symbol • In section: Voltage regulator electrical characteristics <ul style="list-style-type: none"> • In table: Voltage regulator electrical specifications <ul style="list-style-type: none"> • Added note to symbol 'Cbe_fpreg' • In section: Voltage monitor electrical characteristics <ul style="list-style-type: none"> • In table: Voltage monitor electrical characteristics <ul style="list-style-type: none"> • Updated column 'Parameter', 'Min' and 'Max' (of fall/rise trimmed condition) for symbol 'V_{HVD_LV_cold}' and 'V_{LVD_IO_A_HI}' • Updated column 'Parameter', 'Min' and 'Typ' (of fall/rise trimmed condition) for symbol) 'V_{LVD_LV_PD2_hot}', 'V_{LVD_LV_PD2_cold} LV' • Updated column 'Parameter' for symbol 'V_{LVD_LV_PD0_hot}' |

Table continues on the next page...

Table 52. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|----------|------|---|
| | | <ul style="list-style-type: none"> • Updated column 'Typ' and 'Max' (of fall/rise trimmed condition) for symbol 'V_{LVD_FLASH}' • Updated footnote on symbol 'V_{LVD_IO_A_LO}' and 'V_{LVD_IO_A_HI}' |
| | | <ul style="list-style-type: none"> • In section: Supply current characteristics <ul style="list-style-type: none"> • In table: Current consumption characteristics <ul style="list-style-type: none"> • Updated column 'Typ' for symbol 'I_{DD_FULL}' for temperature 85, 105, 125 • Updated column 'Typ' for symbol 'I_{DD_GWY}' for temperature 85, 105, 125 and column 'Max' for temperature 105 • Updated column 'Typ' for symbol 'I_{DD_BODY1}' for temperature 85, 105, 125 • Updated column 'Typ' for symbol 'I_{DD_BODY2}' for temperature 85, 105, 125 and 'Max' for temperature 125 • Added 'Typ' value for temperature 25 for symbol 'I_{DD_STOP}' • Updated column 'Typ' and 'Max' for symbol 'I_{DD_STOP}' for temperature 85, 105, 125 • In table: Low Power Unit (LPU) Current consumption characteristics <ul style="list-style-type: none"> • Updated column 'Typ' for symbol 'LPU_RUN' for temperature 25 and 125 • Added 'Typ' and 'Max' value for temperature 85 and 105 for symbol 'LPU_RUN' • Updated column 'Typ' for symbol 'LPU_STOP' for temperature 25 and 125 • Added 'Typ' and 'Max' value for temperature 85 and 105 for symbol 'LPU_STOP' • In table: STANDBY Current consumption characteristics <ul style="list-style-type: none"> • Updated to have one STANDBY • In section: I/O parameters <ul style="list-style-type: none"> • In table: Functional Pad AC Specifications @ 3.3 V Range <ul style="list-style-type: none"> • Updated values for symbol 'pad_sr_hv (output)' • In table: DC electrical specifications @ 3.3V Range <ul style="list-style-type: none"> • Updated values for V_{DD_HV_x}, V_{ih}, V_{hys} • Added V_{ih} (pad_i_hv), V_{il} (pad_i_hv), V_{hys} (pad_i_hv), V_{ih_hys}, V_{il_hys} • In table: Functional Pad AC Specifications @ 5 V Range <ul style="list-style-type: none"> • Updated values for symbol 'pad_sr_hv (output)' • In table DC electrical specifications @ 5 V Range <ul style="list-style-type: none"> • Added V_{ih} (pad_i_hv), V_{il} (pad_i_hv), V_{hys} (pad_i_hv), V_{ih_hys}, V_{il_hys} |
| | | <ul style="list-style-type: none"> • In section: PORST electrical specifications <ul style="list-style-type: none"> • In table: PORST electrical specifications <ul style="list-style-type: none"> • Updated 'Min' value for W_{NFPORST} • Corrected 'Unit' for V_{IH} and V_{IL} • In section: Peripheral operating requirements and behaviours <ul style="list-style-type: none"> • Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit) • In section: Analogue Comparator (CMP) electrical specifications <ul style="list-style-type: none"> • In table: Comparator and 6-bit DAC electrical specifications <ul style="list-style-type: none"> • Updated 'Max' value of I_{DDLs} • Updated 'Min' and 'Max' for V_{AIO} and DNL • Updated 'Descriptor' 'Min' 'Max' of V_H • Updated row for t_{DHS} • Added row for t_{DLS} • Removed row for V_{CMPOh} and V_{CMPOI} • In section: Clocks and PLL interfaces modules <ul style="list-style-type: none"> • Revised table: Main oscillator electrical characteristics • In table: 16 MHz RC Oscillator electrical specifications |

Table continues on the next page...

Table 52. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|----------|------|--|
| | | <ul style="list-style-type: none"> • Updated 'Max' of Tstartup • In table: 128 KHz Internal RC oscillator electrical specifications <ul style="list-style-type: none"> • Removed Uncalibrated 'Condition' for Fosc • Updated 'Min' and 'Max' of Calibrated Fosc • Updated 'Temperature dependence' and 'Supply dependence' • In table: PLL electrical specifications <ul style="list-style-type: none"> • Removed Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (VDD_LV), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption • Removed 'Typ' value of Duty Cycle at pllclkout • Removed 'Min' from calibration mode of Lock Time • In table: Jitter calculation <ul style="list-style-type: none"> • Added 1 Sigma Random Jitter value for Long term jitter |
| | | <ul style="list-style-type: none"> • In section Flash read wait state and address pipeline control settings <ul style="list-style-type: none"> • Revised table: Flash Read Wait State and Address Pipeline Control • Removed section: On-chip peripherals • Added section: 'Reset sequence' |

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