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Specification

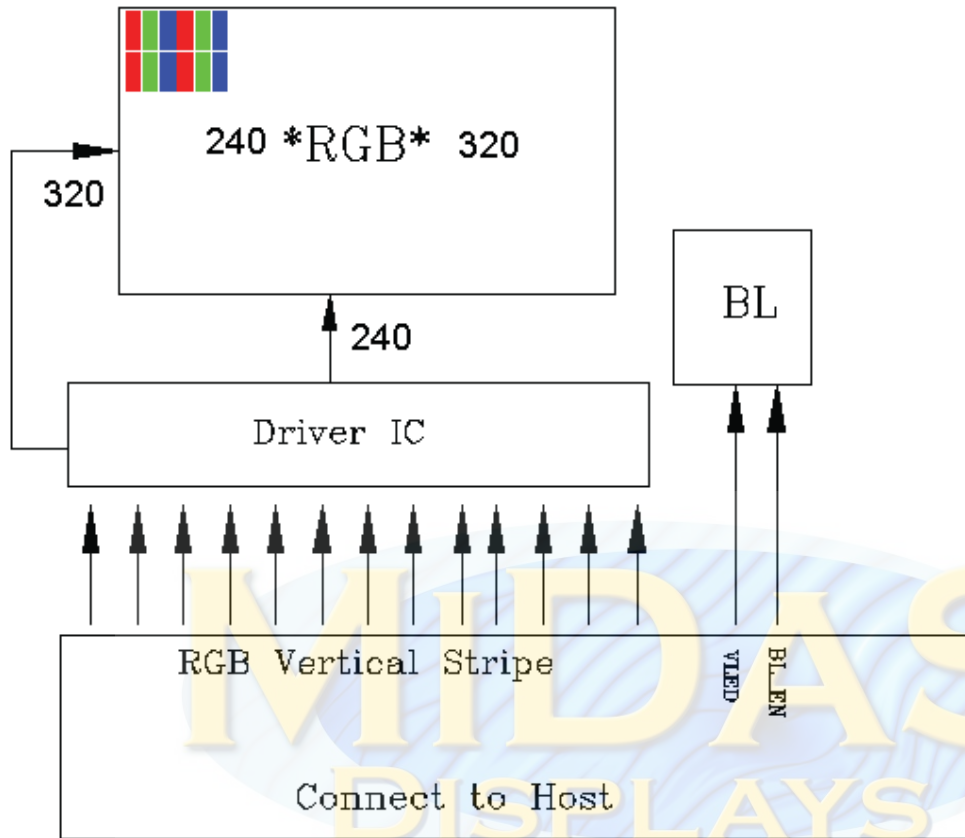


GENERAL SPECIFICATIONS

| ITEM | SPECIFICATION | UNIT |
|---------------------------|---------------------------|-------------|
| OUTLINE DIMENSIONS | 50(W) X69.2 (H) X2.45 (D) | mm |
| DISPLAY SIZE | 2.8 | inch |
| DOT PITCH | 0.18mmX0.18mm | mm |
| NUMBER OF DOTS | 240* (RGB) *320 | - |
| DRIVER IC | ILI9341 | - |
| LCD TYPE | TFT(262K) TRANSMISSIVE | - |
| INTERFACE | MCU 16 BITS | - |
| BACKLIGHT TYPE | LED White | - |
| VIEWING DIRECTION | 6 O'clock | - |

***See attached drawing for details.**

BLOCK DIAGRAM

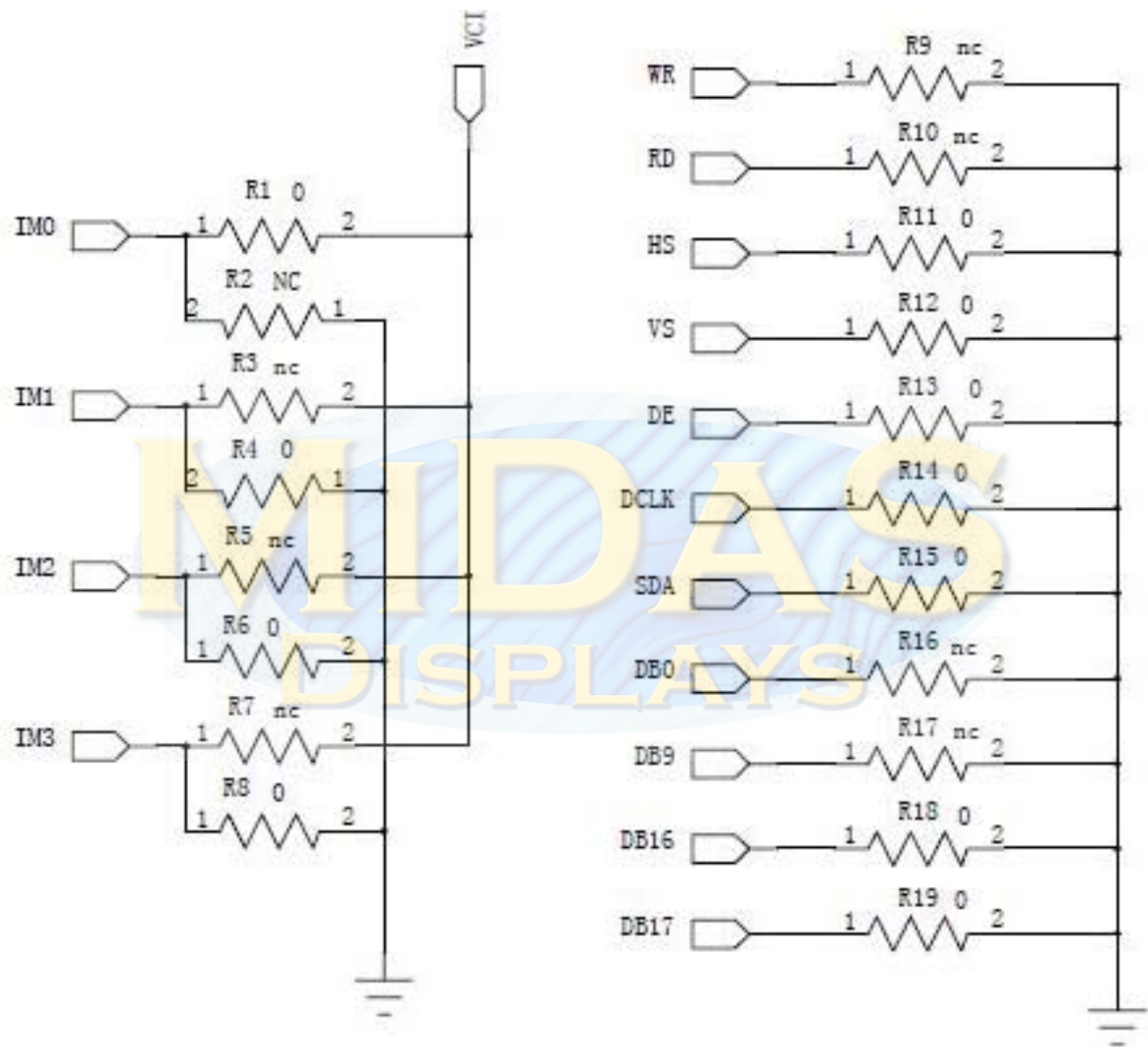


PIN DESCRIPTION:

| NO. | PIN NAME | Type | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----------|------|--|--------------------------------------|-------------|------------------|-----|--------------------|--------------------|---------------|------------------|------|---|---|---|---|------------------------------|--------|--------|---|---|---|---|-------------------------------|--------|---------|---|---|---|---|------------------------------|--------|--------|---|---|---|---|-------------------------------|--------|---------|---|---|---|---|--------------------------------------|-------------|--|---|---|---|---|--------------------------------------|-------------|--|---|---|---|---|--------------------------------|--------|------------------|---|---|---|---|-------------------------------|----------|----------|---|---|---|---|--------------------------------|--------|---------|---|---|---|---|-------------------------------|----------|---------|
| 1 | LEDK | P | Power supply for LED (Cathode) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | LEDA | P | Power supply for LED (Anode) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | GND | P | Ground(0V) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4~6 | NC | - | No connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | SDA | I/O | SPI Serial Data Input/output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | DOTCLK | I | Pixel clock signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | DE | I | Data enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | VSYNC | I | Vertical synchronizing signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | HSYNC | I | Horizontal synchronizing signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | VCC | P | Power voltage | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | RESET | I | Reset signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | GND | P | Ground(0V) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 15~32 | DB17~DB0 | I/O | <p>Data bus</p> <p>- Select the MCU interface mode</p> <table border="1"> <thead> <tr> <th rowspan="2">IM3</th> <th rowspan="2">IM2</th> <th rowspan="2">IM1</th> <th rowspan="2">IM0</th> <th rowspan="2">MCU-Interface Mode</th> <th colspan="2">DB Pin in use</th> </tr> <tr> <th>Register/Content</th> <th>GRAM</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>80 MCU 8-bit bus interface I</td> <td>D[7:0]</td> <td>D[7:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>80 MCU 16-bit bus interface I</td> <td>D[7:0]</td> <td>D[15:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>80 MCU 9-bit bus interface I</td> <td>D[7:0]</td> <td>D[8:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>80 MCU 18-bit bus interface I</td> <td>D[7:0]</td> <td>D[17:0]</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>3-wire 9-bit data serial interface I</td> <td colspan="2">SDA: In/OUT</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>4-wire 8-bit data serial interface I</td> <td colspan="2">SDA: In/OUT</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>80 MCU 16-bit bus interface II</td> <td>D[8:1]</td> <td>D[17:10], D[8:1]</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>80 MCU 8-bit bus interface II</td> <td>D[17:10]</td> <td>D[17:10]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>80 MCU 18-bit bus interface II</td> <td>D[8:1]</td> <td>D[17:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>80 MCU 9-bit bus interface II</td> <td>D[17:10]</td> <td>D[17:9]</td> </tr> </tbody> </table> <p>In MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface (3SPI 0101) * : Fix this pin at VDDI or VSS</p> | IM3 | IM2 | IM1 | IM0 | MCU-Interface Mode | DB Pin in use | | Register/Content | GRAM | 0 | 0 | 0 | 0 | 80 MCU 8-bit bus interface I | D[7:0] | D[7:0] | 0 | 0 | 0 | 1 | 80 MCU 16-bit bus interface I | D[7:0] | D[15:0] | 0 | 0 | 1 | 0 | 80 MCU 9-bit bus interface I | D[7:0] | D[8:0] | 0 | 0 | 1 | 1 | 80 MCU 18-bit bus interface I | D[7:0] | D[17:0] | 0 | 1 | 0 | 1 | 3-wire 9-bit data serial interface I | SDA: In/OUT | | 0 | 1 | 1 | 0 | 4-wire 8-bit data serial interface I | SDA: In/OUT | | 1 | 0 | 0 | 0 | 80 MCU 16-bit bus interface II | D[8:1] | D[17:10], D[8:1] | 1 | 0 | 0 | 1 | 80 MCU 8-bit bus interface II | D[17:10] | D[17:10] | 1 | 0 | 1 | 0 | 80 MCU 18-bit bus interface II | D[8:1] | D[17:0] | 1 | 0 | 1 | 1 | 80 MCU 9-bit bus interface II | D[17:10] | D[17:9] |
| IM3 | IM2 | IM1 | IM0 | | | | | | MCU-Interface Mode | DB Pin in use | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Register/Content | GRAM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 80 MCU 8-bit bus interface I | D[7:0] | D[7:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 80 MCU 16-bit bus interface I | D[7:0] | D[15:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 80 MCU 9-bit bus interface I | D[7:0] | D[8:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 80 MCU 18-bit bus interface I | D[7:0] | D[17:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | 3-wire 9-bit data serial interface I | SDA: In/OUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 4-wire 8-bit data serial interface I | SDA: In/OUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 80 MCU 16-bit bus interface II | D[8:1] | D[17:10], D[8:1] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 80 MCU 8-bit bus interface II | D[17:10] | D[17:10] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 80 MCU 18-bit bus interface II | D[8:1] | D[17:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | 80 MCU 9-bit bus interface II | D[17:10] | D[17:9] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 33 | RD | I | Read signal, active at low in MCU mode; In SPI mode, connect to GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 34 | WR | I | Write Signal, active at low in MCU mode; In SPI mode, SPI Serial Clock | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 35 | RS | I | In MCU mode, Register select signal, low is selected data register; High is selected command register. In SPI mode, connect to GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 36 | CS | I | Chip selection pin/ Serial port data enable signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 37 | XR(NC) | - | No connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 38 | YD(NC) | - | No connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 39 | XL(NC) | - | No connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 40 | YU(NC) | - | No connection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note: 1: input, 0: output, P: Power

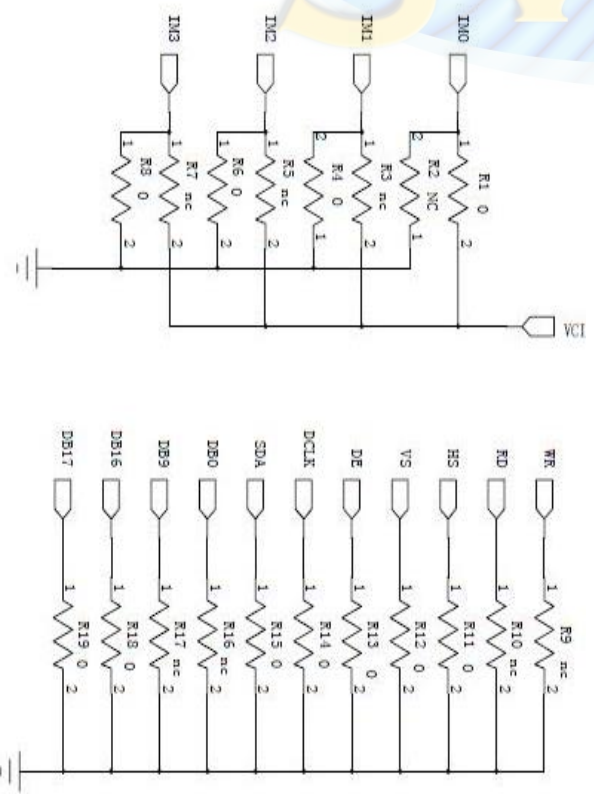
Note: 2: Default interface of this part is "80 MCU 16-bit bus interface 1" ([IM3:IM0] =0001), and "HS", "VS", "DE", "DCLK", "SDA", "DB16", "DB17", already are connected to GND via 0 ohm resistor on FPC. Refer to below circuit.



| IM3 | IM2 | IM1 | IM0 | MCU-Interface Mode | DB pin in use | | PIN of LCM to Gnd |
|-------------|-------------|-------------|-------------|--------------------------|------------------|-----------------|------------------------------|
| | | | | | Register/content | GRAM | |
| 0 | 0 | 0 | 0 | 80 MCU 8bit -bus | DB(7-0) | DB(7-0) | HS,VS,DE,DCLK,SDA,DB8-DB17 |
| 0 | 0 | 0 | 1 | 80 MCU 16bit -bus | DB(7-0) | DB(15-0) | HS,VS,DE,DCLK,SDA,DB16,DB17 |
| 0 | 0 | 1 | 0 | 80 MCU 9bit -bus | DB(7-0) | DB(8-0) | HS,VS,DE,DCLK,SDA,DB9-DB17 |
| 0 | 0 | 1 | 1 | 80 MCU 18bit -bus | DB(7-0) | DB(17-0) | HS,VS,DE,DCLK,SDA |
| 0 | 1 | 0 | 1 | 3-wire 9-bit date serial | SDA in/out | | HS,VS,DE,DCLK,RS,RD,DB0-DB17 |
| 0 | 1 | 1 | 0 | 4-wire 8-bit date serial | SDA in/out | | HS,VS,DE,DCLK,RD,DB0-DB17 |
| 1 | 0 | 0 | 0 | 80 MCU 16bit -bus | DB(8-1) | DB(17-10) (8-1) | HS,VS,DE,DCLK,SDA,DB0,DB9 |
| 1 | 0 | 0 | 1 | 80 MCU 8bit -bus | DB(17-10) | DB(17-10) | HS,VS,DE,DCLK,SDA,DB0-DB9 |
| 1 | 0 | 1 | 0 | 80 MCU 18bit -bus | DB(17-10) | DB(17-0) | HS,VS,DE,DCLK,SDA |
| 1 | 0 | 0 | 1 | 80 MCU 9bit -bus | DB(8-0) | DB(17-9) | HS,VS,DE,DCLK,SDA,DB0-DB8 |
| R6=0 | R5=0 | R3=0 | R1=0 | | | | |
| R8=1 | R6=1 | R4=1 | R2=1 | | | | |

NOTE:

Default interface of this part is "80 MCU 16-bit bus interface I" ([IM3:IM0] =0001), and "HS", "VS", "DE", "DCLK", "SDA", "DB16", "DB17", already are connected to GND via 0 ohm resistor on FPC. Refer to below circuit.



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| Item | Symbol | Values | | Unit | Remark |
|-----------------------------|--------|--------|---------|----------|--------|
| | | Min | Max | | |
| Power Supply for Pump | VCC | -0.3 | 4.5 | V | |
| Operating temperature range | To | -20 | 70 | Degree C | |
| Storage temperature range | Ts | -30 | 80 | Degree C | |
| Logic input voltage range | VI | -0.3 | VCC+0.3 | V | |
| Logic input voltage range | VO | -0.3 | VCC+0.3 | V | |

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics

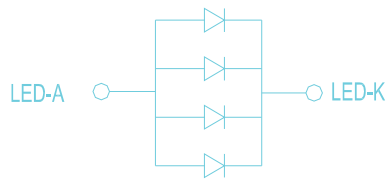
DC Characteristics

| Item | Symbol | Values | | | Unit | Conditions |
|---------------------------|--------|---------|------|---------|------|------------|
| | | Min | Typ | Max | | |
| Low Level Input Voltage | Vil | GND | - | 0.3xVCC | v | |
| High Level Input Voltage | Vih | 0.7xVCC | - | VCC | uA | |
| High Level Output Voltage | Voh | VCC-0.4 | - | VCC | ohm | |
| Low Level Output Voltage | Vol | GND | - | GND+0.4 | uA | |
| Power Supply | VCC | 2.5 | 2.8 | 3.3 | V | |
| Input Leakage Current | Iil | | | ±1.0 | uA | |
| Pull High/Low Resistor | Rp | - | 100K | - | ohm | |

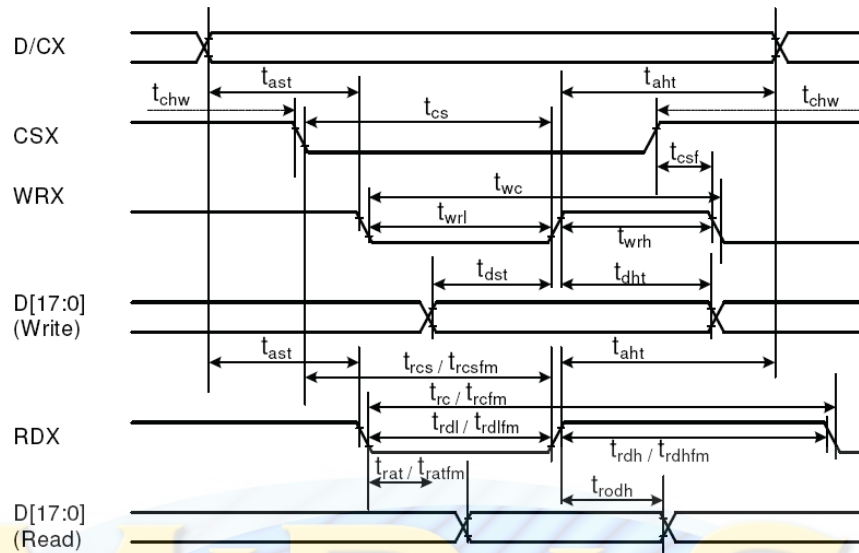
| Item | Symbol | Min | Typ | Max | Unit | Remark |
|----------------------------|--------|-------|-------|-------|-------|---------------|
| Average luminous Intensity | Iv | | 260 | | cd/m2 | IF=60mA |
| Chromaticity Coordinates | X | 0.234 | 0.284 | 0.334 | | IF=60mA |
| | Y | 0.273 | 0.323 | 0.373 | | IF=60mA |
| Forward Voltage | VF | | 3.2 | 3.4 | V | IF=60mA |
| Reverse Current | IR | | | 50 | μA | VR=5V,1LED |
| Luminous Tolerance | IV-M | 80 | | | % | (MIN/MAX)×100 |
| Power Dissipation | Pd | 192 | | | mW | |
| Peak Forward Current | Ifp | 100 | | | uA | |
| Reverse Voltage | VR | 5 | | | V | |

MIDAS
B/L CIRCUIT DIAGRAM

4 PCS WHITE LED; IF = 60mA, VF = 3.2V

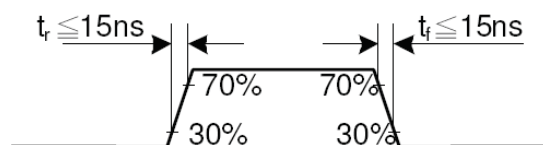


Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)

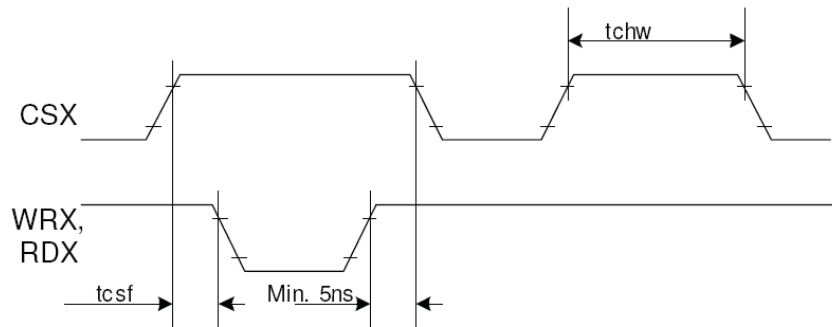


| Signal | Symbol | Parameter | min | max | Unit | Description |
|---|--------|------------------------------------|-----|-----|------|---|
| DCX | tast | Address setup time | 0 | - | ns | |
| | taht | Address hold time (Write/Read) | 0 | - | ns | |
| CSX | tchw | CSX "H" pulse width | 0 | - | ns | |
| | tcs | Chip Select setup time (Write) | 15 | - | ns | |
| | trcs | Chip Select setup time (Read ID) | 45 | - | ns | |
| | trcsfm | Chip Select setup time (Read FM) | 355 | - | ns | |
| | tcsf | Chip Select Wait time (Write/Read) | 10 | - | ns | |
| WRX | twc | Write cycle | 66 | - | ns | |
| | twrh | Write Control pulse H duration | 15 | - | ns | |
| | twrl | Write Control pulse L duration | 15 | - | ns | |
| RDX (FM) | trcfm | Read Cycle (FM) | 450 | - | ns | |
| | trdhfm | Read Control H duration (FM) | 90 | - | ns | |
| | trdlfm | Read Control L duration (FM) | 355 | - | ns | |
| RDX (ID) | trc | Read cycle (ID) | 160 | - | ns | |
| | trdh | Read Control pulse H duration | 90 | - | ns | |
| | trdl | Read Control pulse L duration | 45 | - | ns | |
| D[17:0], D[15:0], D[8:0], D[7:0] | tdst | Write data setup time | 10 | - | ns | For maximum CL=30pF For minimum CL=8pF |
| | tdht | Write data hold time | 10 | - | ns | |
| | trat | Read access time | - | 40 | ns | |
| | tratfm | Read access time | - | 340 | ns | |
| | trod | Read output disable time | 20 | 80 | ns | |

Note: $T_a = -30$ to 70 °C, $V_{DDI}=1.65V$ to $3.3V$, $V_{CI}=2.5V$ to $3.3V$, $V_{SS}=0V$

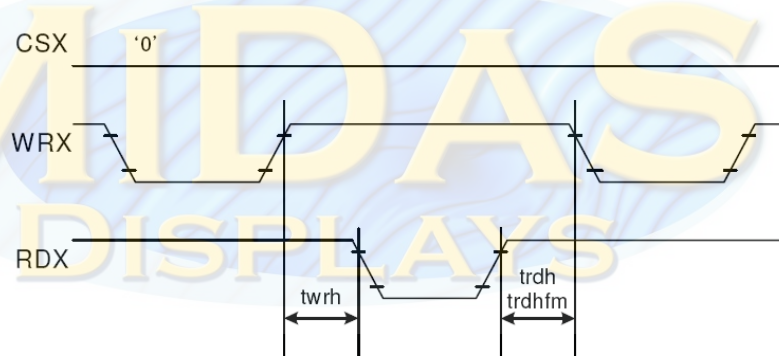


CSX timings :



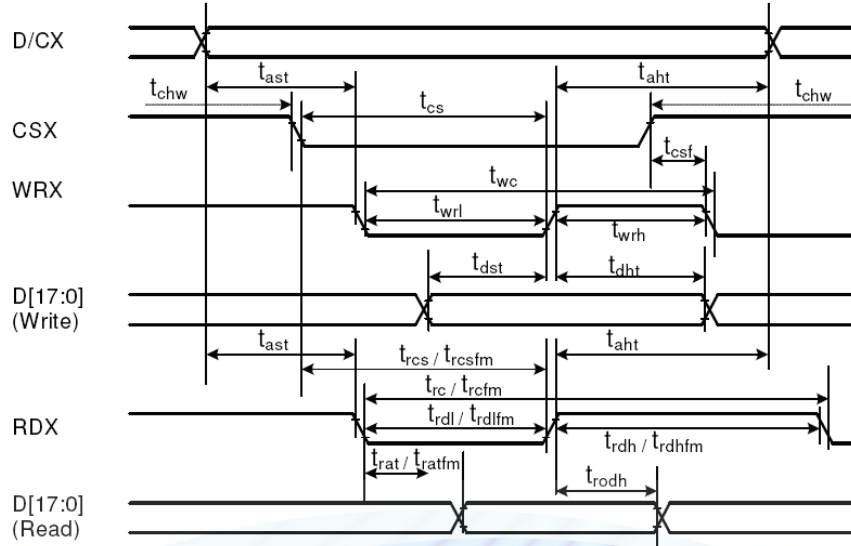
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



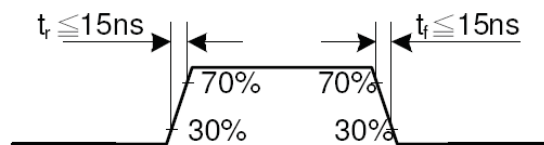
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- II system)

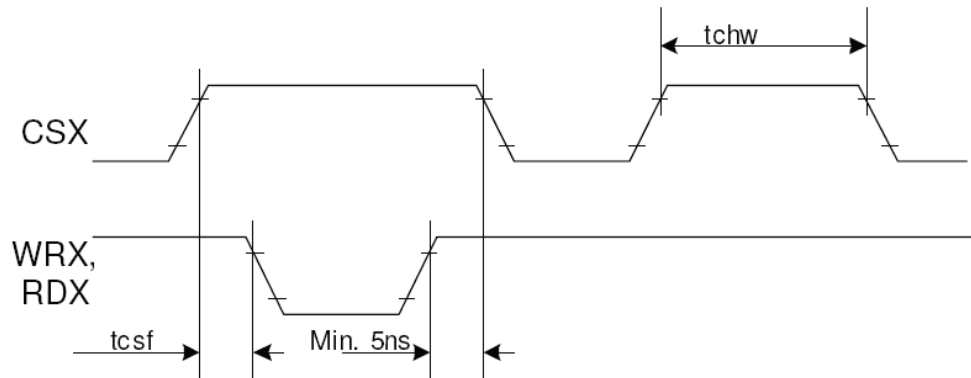


| Signal | Symbol | Parameter | min | max | Unit | Description |
|--|--------------------|------------------------------------|-----|-----|------|---|
| DCX | t _{ast} | Address setup time | 0 | - | ns | |
| | t _{ah} | Address hold time (Write/Read) | 0 | - | ns | |
| CSX | t _{chw} | CSX "H" pulse width | 0 | - | ns | |
| | t _{cs} | Chip Select setup time (Write) | 15 | - | ns | |
| | t _{rcs} | Chip Select setup time (Read ID) | 45 | - | ns | |
| | t _{rcsfm} | Chip Select setup time (Read FM) | 355 | - | ns | |
| | t _{csf} | Chip Select Wait time (Write/Read) | 10 | - | ns | |
| WRX | t _{wc} | Write cycle | 66 | - | ns | |
| | t _{wrh} | Write Control pulse H duration | 15 | - | ns | |
| | t _{wrl} | Write Control pulse L duration | 15 | - | ns | |
| RDX (FM) | t _{rcfm} | Read Cycle (FM) | 450 | - | ns | |
| | t _{rdhfm} | Read Control H duration (FM) | 90 | - | ns | |
| | t _{rdlfm} | Read Control L duration (FM) | 355 | - | ns | |
| RDX (ID) | t _{rc} | Read cycle (ID) | 160 | - | ns | |
| | t _{rdh} | Read Control pulse H duration | 90 | - | ns | |
| | t _{rdl} | Read Control pulse L duration | 45 | - | ns | |
| D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9] | t _{dst} | Write data setup time | 10 | - | ns | For maximum CL=30pF For minimum CL=8pF |
| | t _{dht} | Write data hold time | 10 | - | ns | |
| | t _{rat} | Read access time | - | 40 | ns | |
| | t _{ratfm} | Read access time | - | 340 | ns | |
| | t _{rodh} | Read output disable time | 20 | 80 | ns | |

Note: T_a = -30 to 70 °C, V_{DDI}=1.65V to 3.3V, V_{CI}=2.5V to 3.3V, V_{SS}=0V.

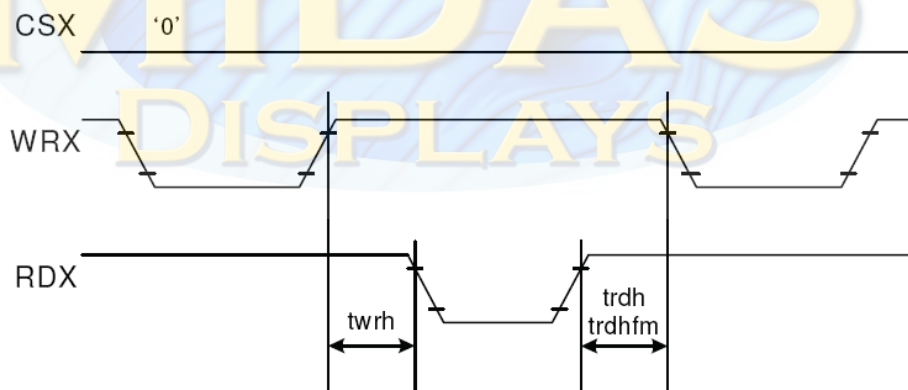


CSX timings :



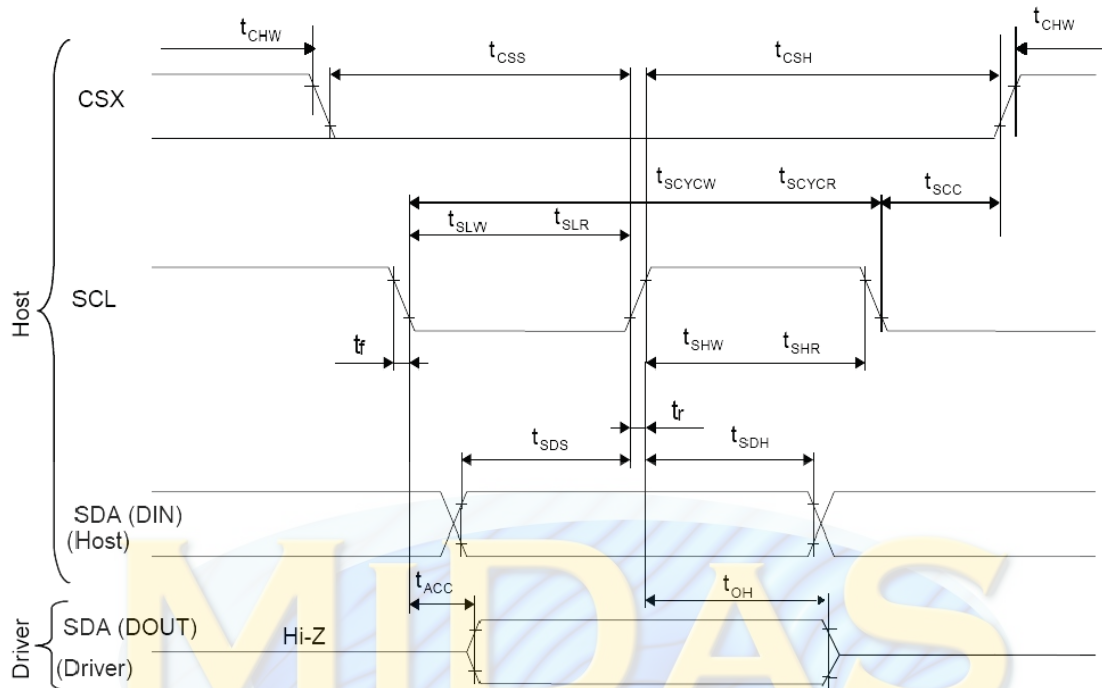
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



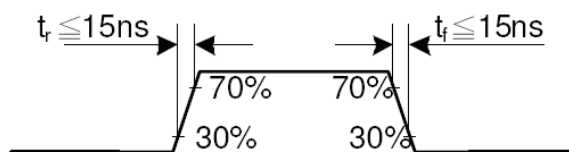
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Display Serial Interface Timing Characteristics (3-line SPI system)

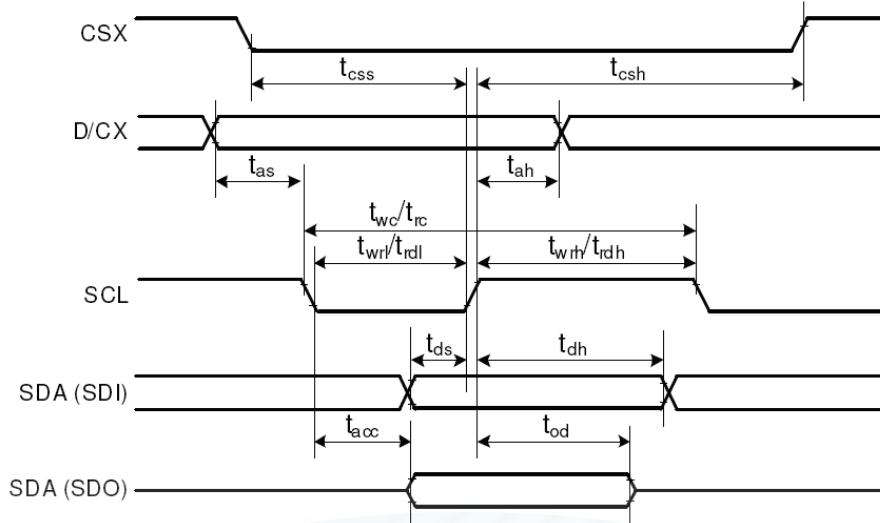


| Signal | Symbol | Parameter | min | max | Unit | Description |
|--------------------|-------------|-----------------------------|-----|-----|------|-------------|
| SCL | t_{scycw} | Serial Clock Cycle (Write) | 100 | - | ns | |
| | t_{shw} | SCL "H" Pulse Width (Write) | 40 | - | ns | |
| | t_{slw} | SCL "L" Pulse Width (Write) | 40 | - | ns | |
| | t_{scycr} | Serial Clock Cycle (Read) | 150 | - | ns | |
| | t_{shr} | SCL "H" Pulse Width (Read) | 60 | - | ns | |
| | t_{slr} | SCL "L" Pulse Width (Read) | 60 | - | ns | |
| SDA / SDI (Input) | t_{sds} | Data setup time (Write) | 30 | - | ns | |
| | t_{sdh} | Data hold time (Write) | 30 | - | ns | |
| SDA / SDO (Output) | t_{acc} | Access time (Read) | 10 | - | ns | |
| | t_{oh} | Output disable time (Read) | 10 | 50 | ns | |
| CSX | t_{scc} | SCL-CSX | 20 | - | ns | |
| | t_{chw} | CSX "H" Pulse Width | 40 | - | ns | |
| | t_{css} | CSX-SCL Time | 60 | - | ns | |
| | t_{csh} | | 65 | - | ns | |

Note: $T_a = 25\text{ }^\circ\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=V_{SS}=0\text{V}$

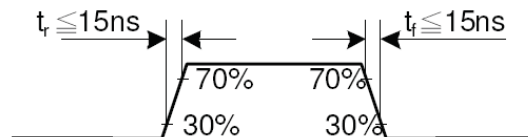


Display Serial Interface Timing Characteristics (4-line SPI system)

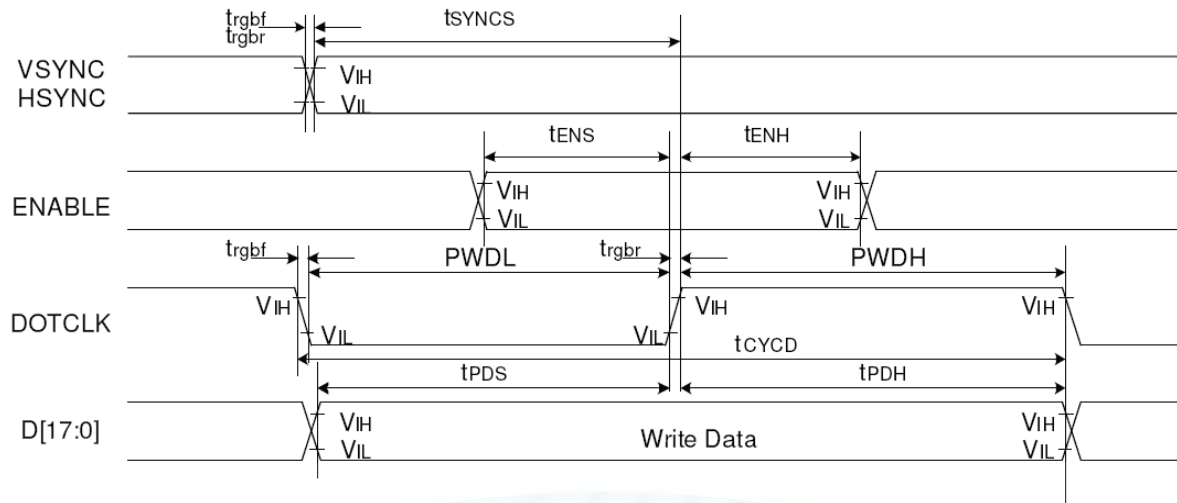


| Signal | Symbol | Parameter | min | max | Unit | Description |
|--------------------|-----------|-------------------------------|-----|-----|------|---------------------|
| CSX | t_{css} | Chip select time (Write) | 40 | - | ns | |
| | t_{csh} | Chip select hold time (Read) | 40 | - | ns | |
| SCL | t_{wc} | Serial clock cycle (Write) | 100 | - | ns | |
| | t_{wrh} | SCL "H" pulse width (Write) | 40 | - | ns | |
| | t_{wrl} | SCL "L" pulse width (Write) | 40 | - | ns | |
| | t_{rc} | Serial clock cycle (Read) | 150 | - | ns | |
| | t_{rdh} | SCL "H" pulse width (Read) | 60 | - | ns | |
| | t_{rdl} | SCL "L" pulse width (Read) | 60 | - | ns | |
| D/CX | t_{as} | D/CX setup time | 10 | - | | |
| | t_{ah} | D/CX hold time (Write / Read) | 10 | - | | |
| SDA / SDI (Input) | t_{ds} | Data setup time (Write) | 30 | - | ns | |
| | t_{dh} | Data hold time (Write) | 30 | - | ns | |
| SDA / SDO (Output) | t_{acc} | Access time (Read) | 10 | - | ns | For maximum CL=30pF |
| | t_{od} | Output disable time (Read) | 10 | 50 | ns | For minimum CL=8pF |

Note: $T_a = 25\text{ }^\circ\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=VSS=0\text{V}$

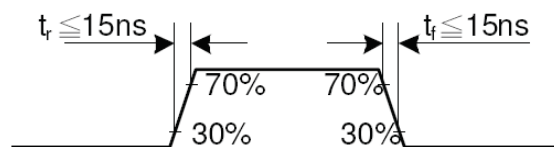


Parallel 18/16/6-bit RGB Interface Timing Characteristics



| Signal | Symbol | Parameter | min | max | Unit | Description | |
|---------------|----------------------|-------------------------------------|-----|-----|------|----------------------------------|------------------------------|
| VSYNC / HSYNC | t_{SYNCS} | VSYNC/HSYNC setup time | 15 | - | ns | 18/16-bit bus RGB interface mode | |
| | t_{SYNCH} | VSYNC/HSYNC hold time | 15 | - | ns | | |
| DE | t_{ENS} | DE setup time | 15 | - | ns | | |
| | t_{ENH} | DE hold time | 15 | - | ns | | |
| D[17:0] | t_{POS} | Data setup time | 15 | - | ns | | |
| | t_{PDH} | Data hold time | 15 | - | ns | | |
| DOTCLK | PWDH | DOTCLK high-level period | 15 | - | ns | | |
| | PWDL | DOTCLK low-level period | 15 | - | ns | | |
| | t_{CYCD} | DOTCLK cycle time | 100 | - | ns | | |
| | t_{rgrb}, t_{fgrb} | DOTCLK, HSYNC, VSYNC rise/fall time | - | 15 | ns | | |
| VSYNC / HSYNC | t_{SYNCS} | VSYNC/HSYNC setup time | 15 | - | ns | | 6-bit bus RGB interface mode |
| | t_{SYNCH} | VSYNC/HSYNC hold time | 15 | - | ns | | |
| DE | t_{ENS} | DE setup time | 15 | - | ns | | |
| | t_{ENH} | DE hold time | 15 | - | ns | | |
| D[17:0] | t_{POS} | Data setup time | 15 | - | ns | | |
| | t_{PDH} | Data hold time | 15 | - | ns | | |
| DOTCLK | PWDH | DOTCLK high-level pulse period | 15 | - | ns | | |
| | PWDL | DOTCLK low-level pulse period | 15 | - | ns | | |
| | t_{CYCD} | DOTCLK cycle time | 100 | - | ns | | |
| | t_{rgrb}, t_{fgrb} | DOTCLK, HSYNC, VSYNC rise/fall time | - | 15 | ns | | |

Note: $T_a = -30$ to 70 °C, $V_{DDI} = 1.65V$ to $3.3V$, $V_{CI} = 2.5V$ to $3.3V$, $AGND = VSS = 0V$



Controller Information

IC: ILI9341

OPTICAL CHARACTERISTICS

| Item | Symbol | Conditions | Specifications | Unit | Note |
|--------------------------|-----------|---|----------------|------|---|
| Transmittance | T% | Viewing normal angle $\theta_x = \theta_y = 0^\circ$ | 6.0 | % | All left side data are based on CMO's following condition – 1.CG : NTSC 59% 2.LC : TN 3.Light Source : CMO LED BLU 4.Film : Nitto Linear Polarizer 5.Machine : DMS |
| Contrast Ratio | CR | | 300 | -- | |
| Response Time (by Quick) | Ton+ Toff | | 30 | ms | |
| Viewing Angle | Hor. | θ_{x+} | 45 | deg. | |
| | | θ_{x-} | 45 | | |
| | Ver. | θ_{y+} | 45 | | |
| | | θ_{y-} | 20 | | |
| CF only Chromaticity | Red | X_R | 0.631 | -- | |
| | | Y_R | 0.316 | -- | |
| | Green | X_G | 0.298 | -- | |
| | | Y_G | 0.566 | -- | |
| | Blue | X_B | 0.138 | -- | |
| | | Y_B | 0.122 | -- | |
| | White | X_W | 0.297 | -- | |
| | | Y_W | 0.327 | -- | |

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

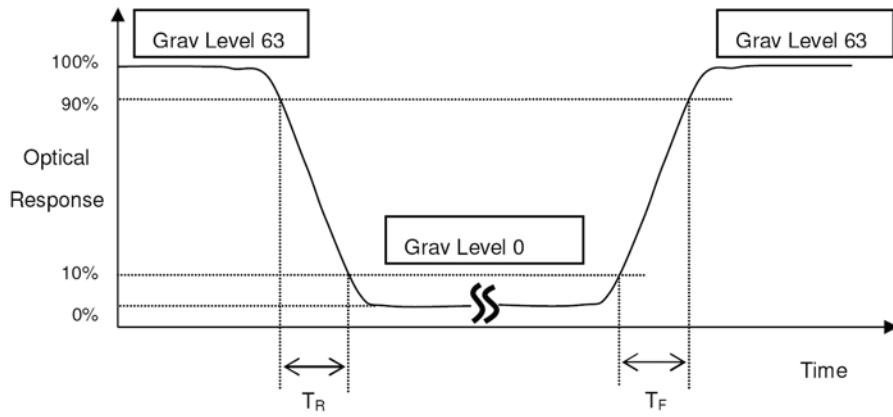
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

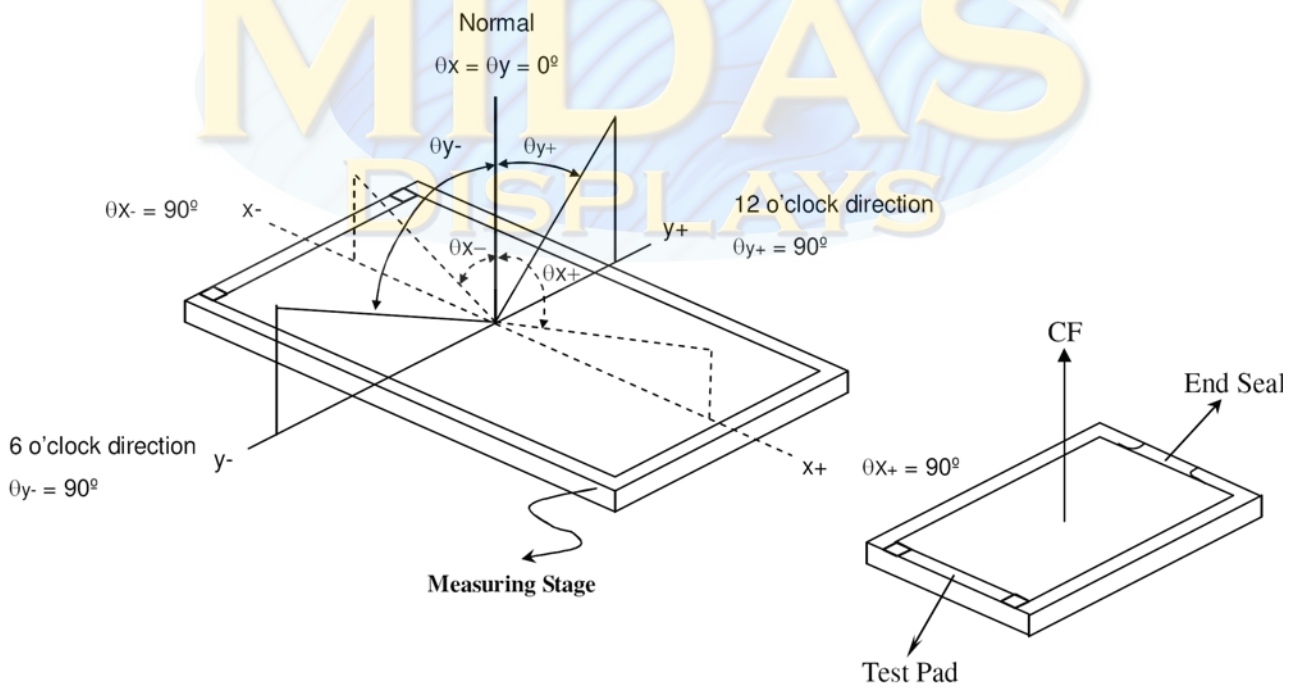
$$CR = CR(10)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

*Note (2) Definition of Response Time (Ton, Toff):

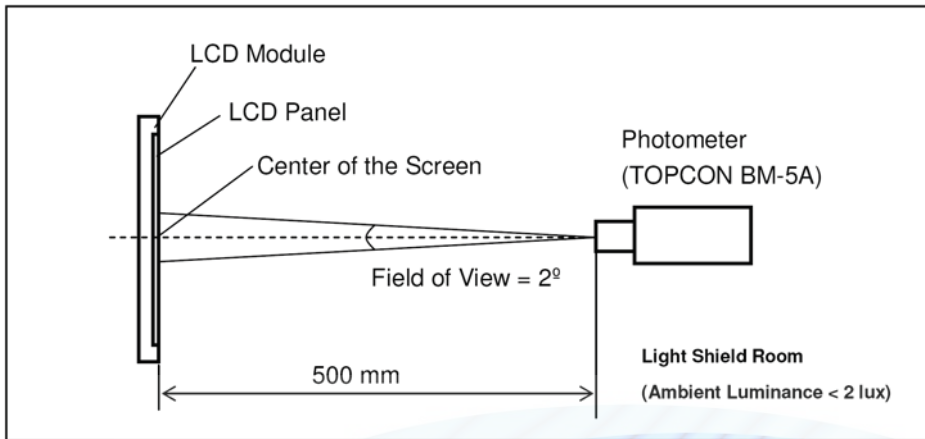


*Note(3) Definition of Viewing Angle

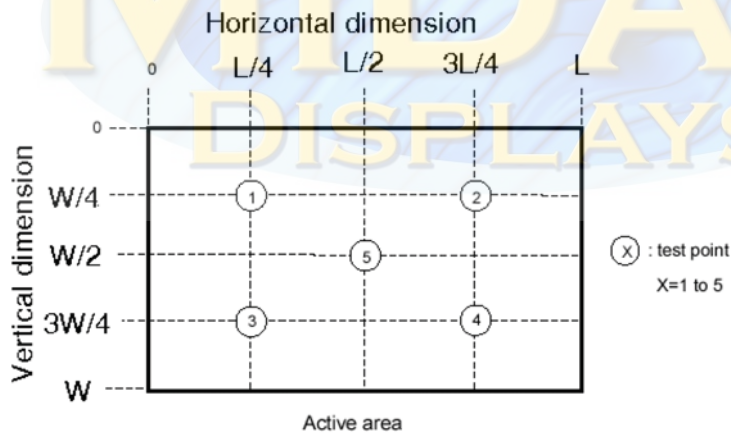


*Note (4) Measurement Set-Up:

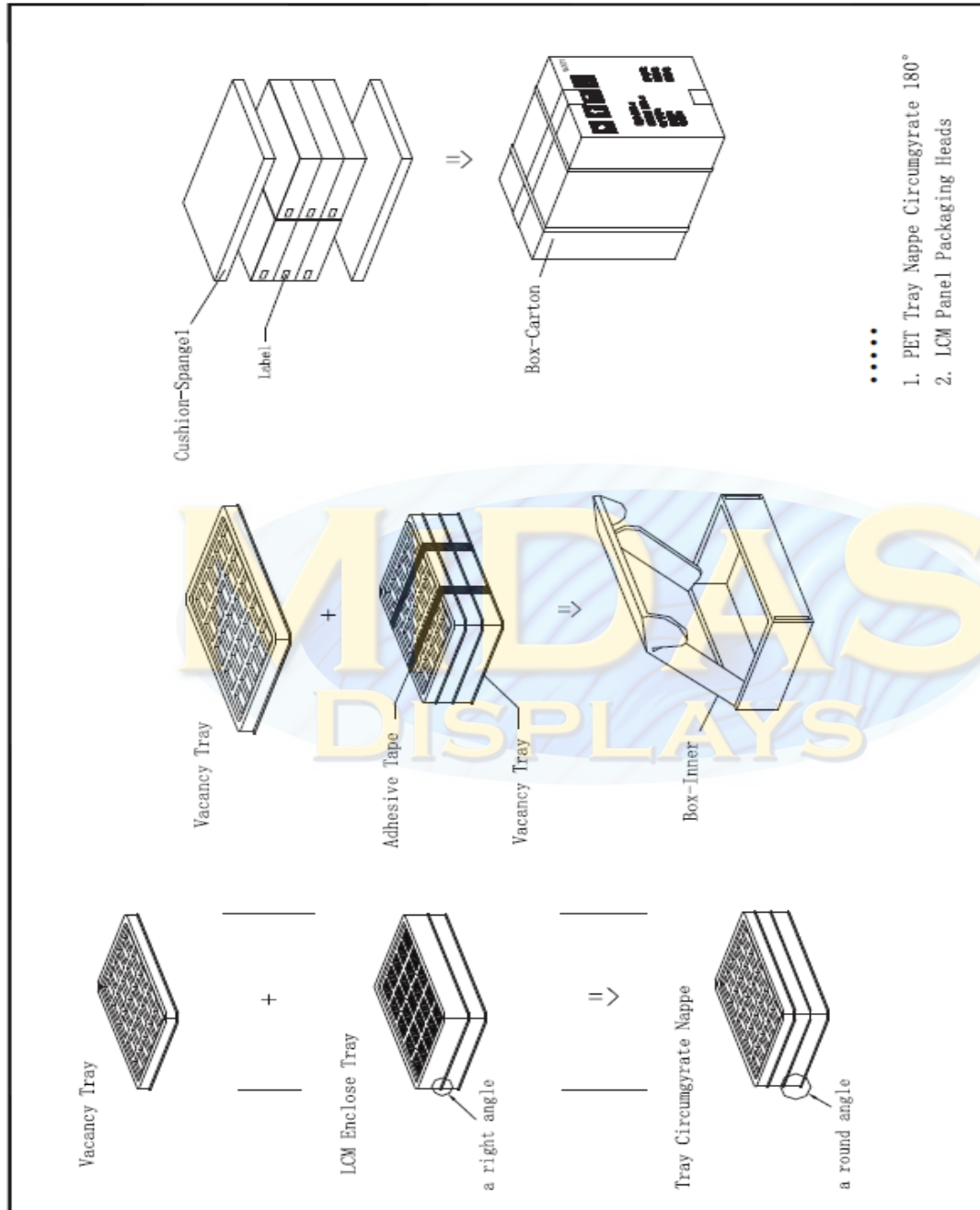
The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (5)



PACKAGE



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