

4V Drive Pch+Pch MOS FET

SP8J3

●Structure

Silicon P-channel MOS FET

●Features

- 1) Low On-resistance. (100mΩ at 4.5V)
- 2) High Power Package. (PD=2.0W)
- 3) High speed switching.
- 4) Low voltage drive. (4V)

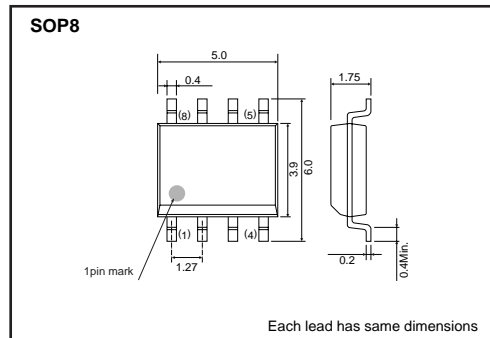
●Applications

Power switching, DC-DC converter

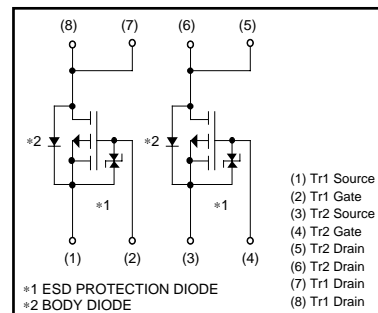
●Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8J3		○

●External dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V _{DSS}	-30	V	
Gate-source voltage	V _{GSS}	±20	V	
Drain current	Continuous	I _D	±3.5	A
	Pulsed	I _{DP} *1	±14	A
Source current (Body diode)	Continuous	I _S	-1.6	A
	Pulsed	I _{SP} *1	-14	A
Total power dissipation	P _D *2	2.0	W	
Channel temperature	T _{ch}	150	°C	
Range of Storage temperature	T _{stg}	-55 to +150	°C	

*1 Pw≤10μs, Duty cycle≤1%
*2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	R _{th(ch-a)} *	62.5	°C / W

* Mounted on a ceramic board.

Transistors

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±10	μA	V _{GS} =±20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	–30	–	–	V	I _D = –1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	–1	μA	V _{DS} = –30V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	–1.0	–	–2.5	V	V _{DS} = –10V, I _D = –1mA
Static drain-source on-state resistance	R _{DS(on)} *	–	65	90	mΩ	I _D = –3.5A, V _{GS} = –10V
		–	100	140	mΩ	I _D = –1.75A, V _{GS} = –4.5V
		–	120	165	mΩ	I _D = –1.75A, V _{GS} = –4.0V
Forward transfer admittance	Y _{fs} *	1.8	–	–	S	V _{DS} = –10V, I _D = –1.75A
Input capacitance	C _{iss}	–	490	–	pF	V _{DS} = –10V
Output capacitance	C _{oss}	–	110	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	–	75	–	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	–	10	–	ns	I _D = –1.75A
Rise time	t _r *	–	15	–	ns	V _{DD} ≐ –15V
Turn-off delay time	t _{d(off)} *	–	35	–	ns	V _{GS} = –10V
Fall time	t _f *	–	10	–	ns	R _L =8.6Ω
Total gate charge	Q _g *	–	5.5	–	nC	V _{DD} ≐ –15V
Gate-source charge	Q _{gs} *	–	1.5	–	nC	V _{GS} = –5V
Gate-drain charge	Q _{gd} *	–	2.0	–	nC	I _D = –3.5A

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD}	–	–	–1.2	V	I _S = –1.6A, V _{GS} =0V

Transistors

●Electrical characteristic curves

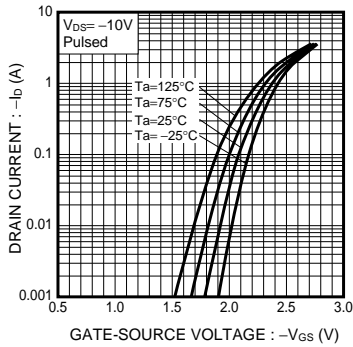


Fig.1 Typical Transfer Characteristics

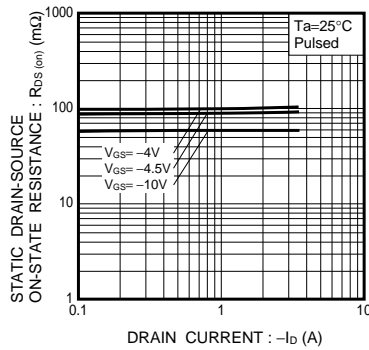


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

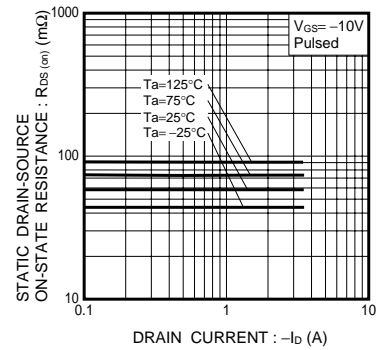


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

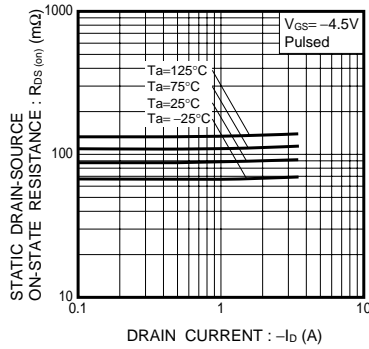


Fig.4 Static Drain-Source On-State vs. Drain Current

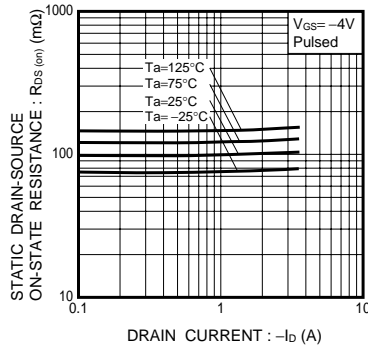


Fig.5 Static Drain-Source On-State vs. Drain Current

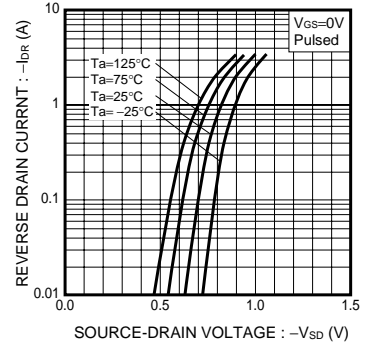


Fig.6 Reverse Drain Current Source-Drain Current

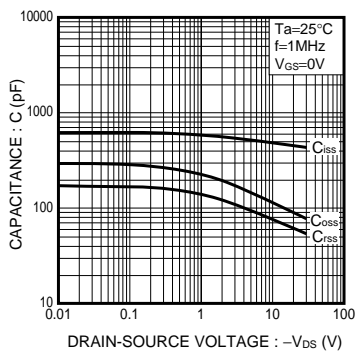


Fig.7 Typical Capacitance vs. Drain-Source Voltage

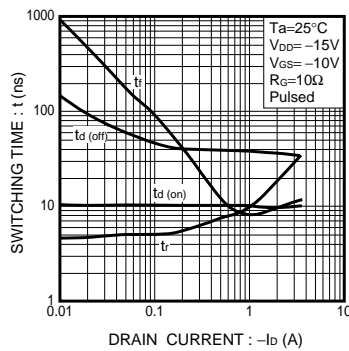


Fig.8 Switching Characteristics

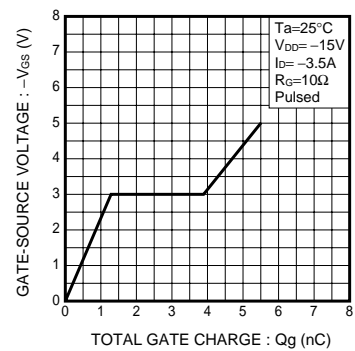


Fig.9 Dynamic Input Characteristics

Transistors

●Measurement circuits

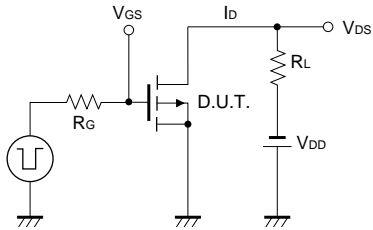


Fig.10 Switching Time Test Circuit

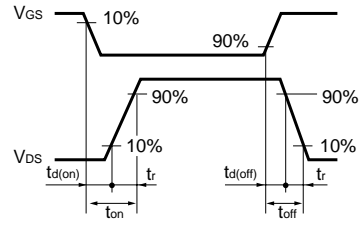


Fig.11 Switching Time Waveforms

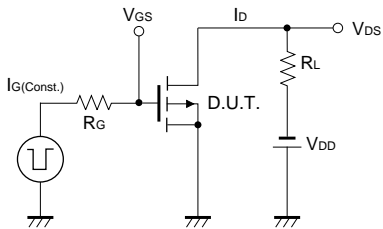


Fig.12 Gate Charge Test Circuit

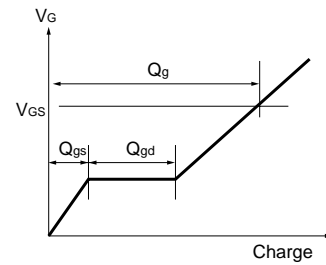


Fig.13 Gate Charge Waveform

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