# Contents

# 1. Revision History

| DATE | VERSION | REVISED PAGE NO. | Note |
|---|---|---|---|
| 2011/07/19 | 1 | | First issue |

# 2. General Specification

The Features of the Module is description as follow:

- Module dimension: 74.2 x 25.2 x 6.3 (max.) mm3
- View area: 61.0 x 15.1 mm2
- Active area: 58.5 x 9.8 mm2
- Number of Characters: 20 characters x 2 Lines
- Dot size: 0.45 x 0.54 mm2
- Dot pitch: 0.50x 0.59 mm2
- Character size: 2.45 x 4.67 mm2
- Character pitch: 2.95 x 5.17 mm2
- LCD type: FSTN Positive Transflective
- Duty: 1/16 , 1/5 Bias
- View direction: 6 o'clock
- Backlight Type: LED, White

# Midas LCD Part Number System

| MC | COG | 132033 | A | * | 6 | W | * | * | - | S | N | T | L | W | * | * |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | - | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

1 = **MC:** Midas Components

2 = **Blank:** COB (chip on board) **COG**: chip on glass

3 = **No of dots** (e.g. 240064 = 240 x 64 dots) (e.g. 21605 = 2 x 16 5mm C.H.)

4 = **Series**

5 = **Series Variant:** A to Z – see addendum

6 = **3:** 3 o'clock **6:** 6 o'clock **9**: 9 o'clock **12**: 12 o'clock

7 = **S**: Normal (0 to + 50 deg C) **W:** Wide temp. (-20 to + 70 deg C) **X:** Extended temp (-30 + 80 Deg C)

8 = **Character Set**

**Blank:** Standard (English/Japanese)
**C:** Chinese Simplified (Graphic Displays only)
**CB:** Chinese Big 5 (Graphic Displays only)
**H:** Hebrew
**K:** European (std) (English/German/French/Greek)
**L:** English/Japanese (special)
**M:** European (English/Scandinavian)
**R:** Cyrillic
**W:** European (English/Greek)
**U:** European (English/Scandinavian/Icelandic)

9 = **Bezel Height** (where applicable / available)

| | Top of Bezel to Top of PCB | Common (via pins 1 and 2) | Array or Edge Lit |
|---|---|---|---|
| **Blank** | 9.5mm / not applicable | Common | Array |
| **2** | 8.9 mm | Common | Array |
| **3** | 7.8 mm | Separate | Array |
| **4** | 7.8 mm | Common | Array |
| **5** | 9.5 mm | Separate | Array |
| **6** | 7 mm | Common | Array |
| **7** | 7 mm | Separate | Array |
| **8** | 6.4 mm | Common | Edge |
| **9** | 6.4 mm | Separate | Edge |
| **A** | 5.5 mm | Common | Edge |
| **B** | 5.5 mm | Separate | Edge |
| **D** | 6.0mm | Separate | Edge |
| **E** | 5.0mm | Separate | Edge |
| **F** | 4.7mm | Common | Edge |
| **G** | 3.7mm | Separate | EL |

10 = **T:** TN **S**: STN **B:** STN Blue **G:** STN Grey **F:** FSTN **F2:** FFSTN

11 = **P:** Positive **N**: Negative

12 = **R:** Reflective **M**: Transmissive **T:** Transflective

13 = **Backlight: Blank:** Reflective **L:** LED

14 = **Backlight Colour: Y:** Yellow-Green **W:** White **B:** Blue **R:** Red **A:** Amber **O:** Orange **G:** Green **RGB:** R.G.B.

15 = **Driver Chip: Blank:** Standard **I:** I²C **T:** Toshiba T6963C **A:** Avant SAP1024B **R:** Raio RA8835

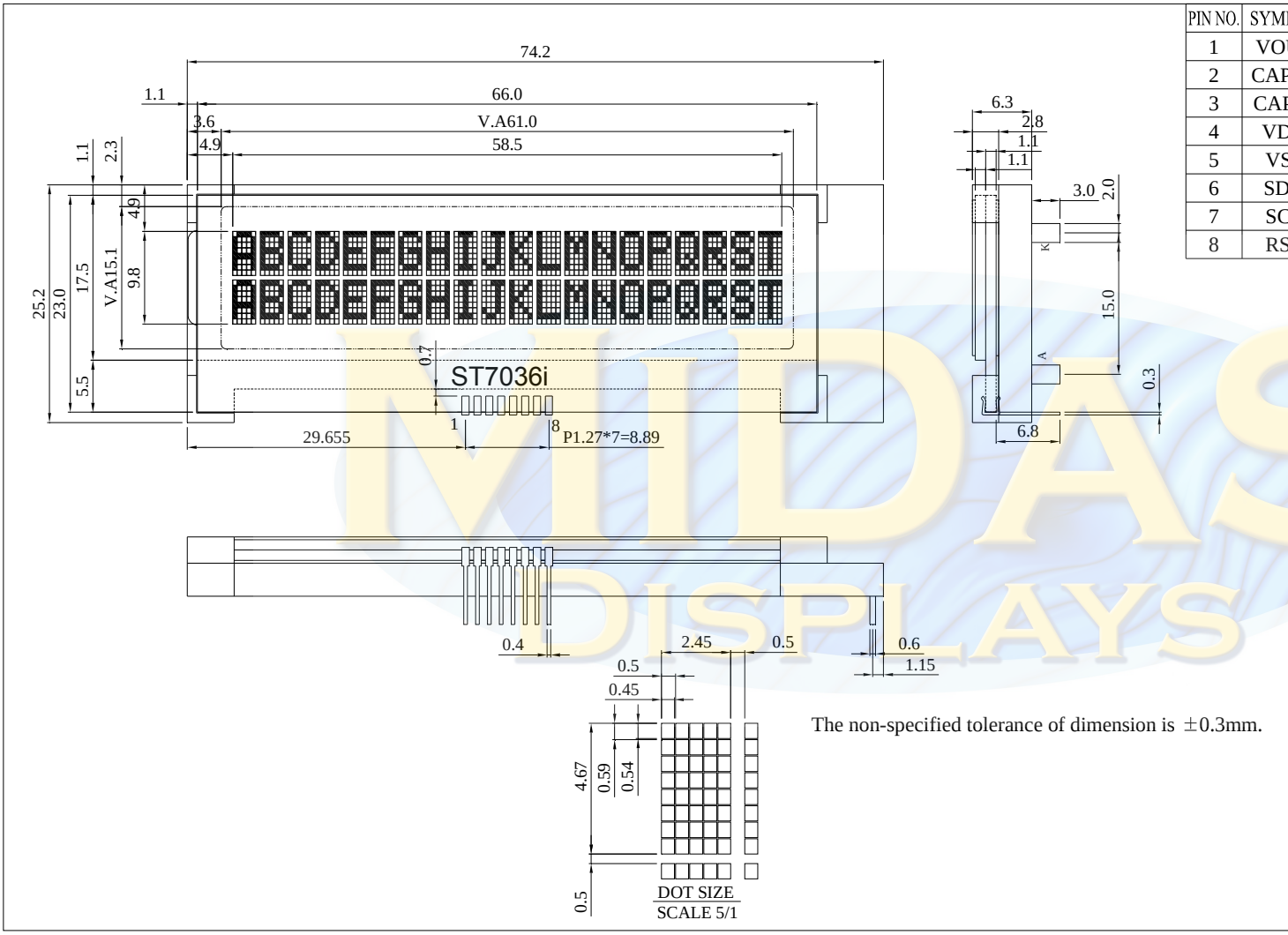
16 = **Voltage Variant**: e.g. **3** = 3v

# 4. Interface Pin Function

| Pin No. | Symbol | Level | Description |
|---|---|---|---|
| 1 | VOUT | | DC/DC voltage converter. Connect a capacitor between this terminal and VIN when the built-in booster is used. |
| 2 | CAP1N | | For voltage booster circuit(VDD-VSS)<br>External capacitor about 0.1u~4.7uf |
| 3 | CAP1P | | |
| 4 | VDD | 3.0/5.0V | Power supply |
| 5 | VSS | | GND |
| 6 | SDA | | (In I2C interface DB7 (SDA) is input data.<br>SDA and SCL must connect to I2C bus (I2C bus is to connect a resister between SDA/SCL and the power of I2C bus ). |
| 7 | SCL | | (In I2C interface DB6 (SCL) is clock input.<br>SDA and SCL must connect to I2C bus (I2C bus is to connect a resister between SDA/SCL and the power of I2C bus ). |
| 8 | RST | | RESET * |

* Please note, if you do not wish to use Reset, it should be tied high

# 5. Outline Dimension

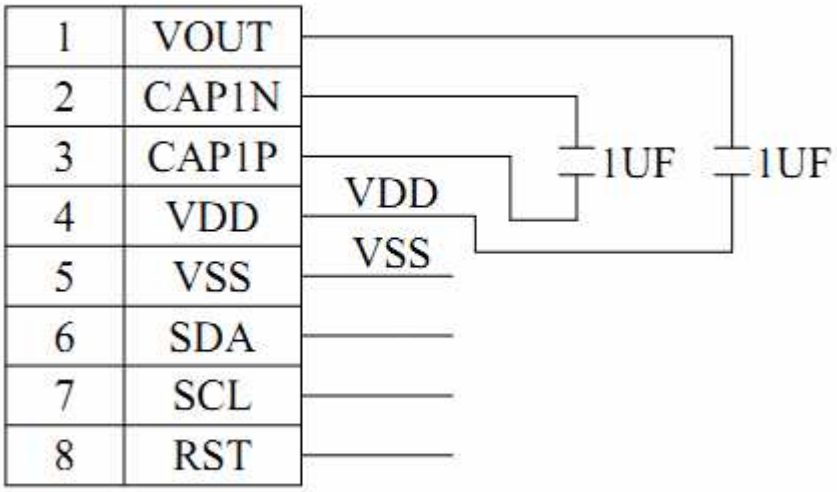



| PIN NO. | SYM |
|---|---|
| 1 | VO |
| 2 | CAP |
| 3 | CAP |
| 4 | VD |
| 5 | VS |
| 6 | SD |
| 7 | SC |
| 8 | RS |

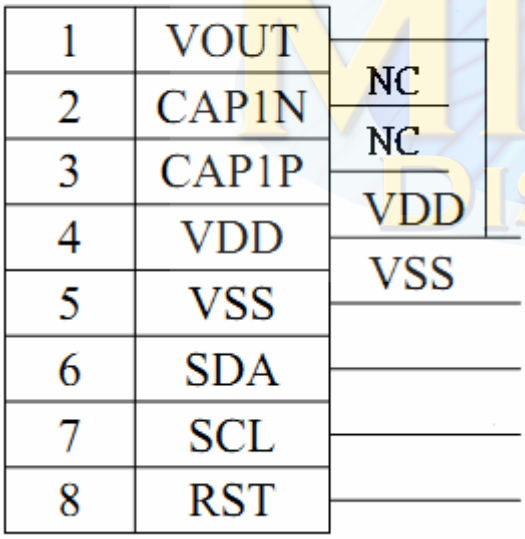
The non-specified tolerance of dimension is ±0.3mm.

## Application schematic

VDD=3.0V




VDD=5.0V



**INITIALIZE: (3V)**

```
MOV     I2C_CONTROL,#00H ;WRITE COMMAND
MOV     I2C_DATA,#38H    ;Function Set
LCALL   WRITE_CODE
MOV     I2C_CONTROL,#00H ;WRITE COMMAND
MOV     I2C_DATA,#39H    ;Function Set
LCALL   WRITE_CODE
MOV     I2C_DATA,#14H    ;Internal OSC frequency
LCALL   WRITE_CODE
MOV     I2C_DATA,#74H    ;Contrast set
LCALL   WRITE_CODE
MOV     I2C_DATA,#54H        ;Power/ICON control/Contrast set
LCALL   WRITE_CODE
MOV     I2C_DATA,#6FH        ;Follower control
LCALL   WRITE_CODE
MOV     I2C_DATA,#0CH    ;Display ON/OFF
LCALL   WRITE_CODE
MOV     I2C_DATA,#01H    ;Clear Display
LCALL   WRITE_CODE
```

**INITIALIZE: (5V)**

```
MOV     I2C_CONTROL,#00H;WRITE COMMAND
MOV     I2C_DATA,#38H    ;Function Set
LCALL   WRITE_CODE
MOV     I2C_CONTROL,#00H;WRITE COMMAND
MOV     I2C_DATA,#39H    ;Function Set
LCALL   WRITE_CODE
MOV     I2C_DATA,#14H    ;Internal OSC frequency
LCALL   WRITE_CODE
MOV     I2C_DATA,#79H    ;Contrast set
LCALL   WRITE_CODE
MOV     I2C_DATA,#50H        ;Power/ICON control/Contrast set
LCALL   WRITE_CODE
MOV     I2C_DATA,#6CH        ;Follower control
LCALL   WRITE_CODE
MOV     I2C_DATA,#0CH    ;Display ON/OFF
LCALL   WRITE_CODE
MOV     I2C_DATA,#01H    ;Clear Display
LCALL   WRITE_CODE
```

# 6.Absolute Maximum Ratings

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Temperature | $T_{OP}$ | -20 | — | +70 | ℃ |
| Storage Temperature | $T_{ST}$ | -30 | — | +80 | ℃ |
| Supply voltage for Logic | $V_{DD}$ | -0.3 | — | 6.0 | V |
| LCD Driver Voltage | $V_{LCD}$ | 7.0- $V_{SS}$ | | -0.3+ $V_{SS}$ | V |

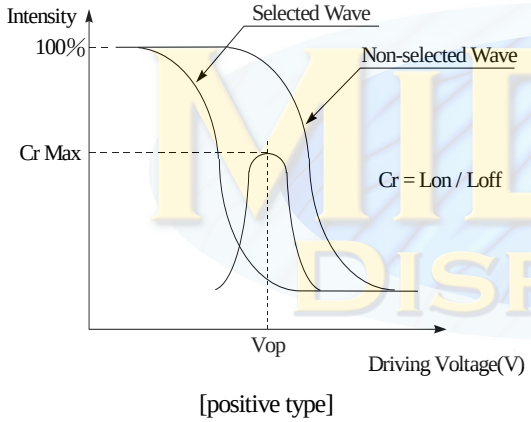
# 7.Electrical Characteristics

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage For Logic | $V_{DD}$-$V_{SS}$ | — | 3 | 3.3 | 5 (bon=1 max=3.5V) | V |
| Supply Voltage For LCD | $V_{LCD}$ | Ta=-20℃<br>Ta=25℃<br>Ta=70℃ | —<br>—<br>— | —<br>4.5<br>— | —<br>—<br>— | V<br>V<br>V |
| Input High Volt. | $V_{IH}$ | — | 0.7 $V_{DD}$ | — | $V_{DD}$ | V |
| Input Low Volt. | $V_{IL}$ | — | — | — | 0.2 $V_{DD}$ | V |
| Output High Volt. | $V_{OH}$ | — | 0.8 $V_{DD}$ | — | $V_{DD}$ | V |
| Output Low Volt. | $V_{OL}$ | — | — | — | 0.2$V_{DD}$ | V |
| Supply Current(No include LED Backlight) | $I_{DD}$ | — | — | 0.2 | — | mA |

# 8.Optical Characteristics

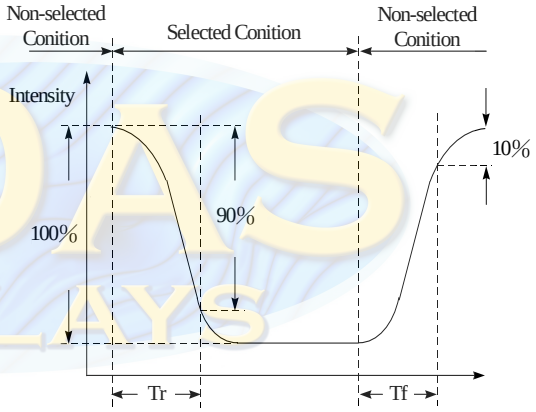
| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| View Angle | (V)θ | CR≧2 | 30 | — | 60 | deg |
| | (H)φ | CR≧2 | -45 | — | 45 | deg |
| Contrast Ratio | CR | — | — | 5 | — | — |
| Response Time | T rise | — | — | 250 | 400 | ms |
| | T fall | — | — | 100 | 250 | ms |

**Definition of Operation Voltage (Vop)**




[positive type]

**Definition of Response Time ( Tr , Tf )**



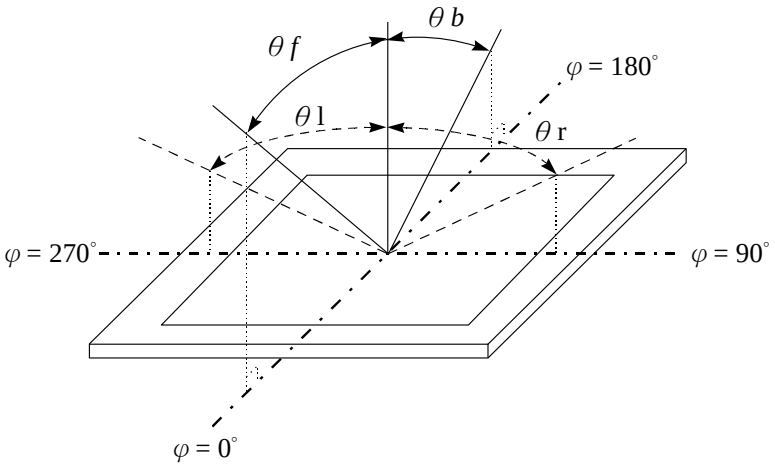

[positive type]

**Conditions :**

Operating Voltage : Vop Viewing Angle(θ，φ) : 0°， 0°

Frame Frequency : 64 HZ Driving Waveform : 1/N duty , 1/a bias

**Definition of viewing angle(CR≧2)**



# 9.Function Description

**● System Interface**

This chip has all four kinds of interface type with MPU: 4-bit bus, 8-bit bus, serial and fast I2C interface. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from

DDRAM/CGRAM/ICON RAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM/ICON RAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

| RS | R/W | Operation |
|---|---|---|
| L | L | Instruction Write operation (MPU writes Instruction code into IR) |
| L | H | Read Busy Flag(DB7) and address counter (DB0 ~ DB6) |
| H | L | Data Write operation (MPU writes data into DR) |
| H | H | Data Read operation (MPU reads data from DR) |

Table 1. Various kinds of operations according to RS and R/W bits.

**I2C interface**

**It just only could write Data or Instruction to ST7036 by the IIC Interface.**

**It could not read Data or Instruction from ST7036 (except Acknowledge signal).**

SCL: serial clock input

SDA_IN: serial data input

SDA_OUT: acknowledge response output

**Slaver address could set from “0111100” to “0111111”.**

The I2C interface send RAM data and executes the commands sent via the I2C Interface. It could send data in to the RAM.

The I2C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

**BIT TRANSFER**

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.1.

**START AND STOP CONDITIONS**

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.2.

**SYSTEM CONFIGURATION**

The system configuration is illustrated in Fig.3.

· Transmitter: the device, which sends the data to the bus

· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer

· Slave: the device addressed by a master

· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message

· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted

· Synchronization: procedure to synchronize the clock signals of two or more devices.

**ACKNOWLEDGE**

**Acknowledge signal (ACK) is not BF signal in parallel interface.**

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is
addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP
condition. Acknowledgement on the I2C Interface is illustrated in Fig.4.

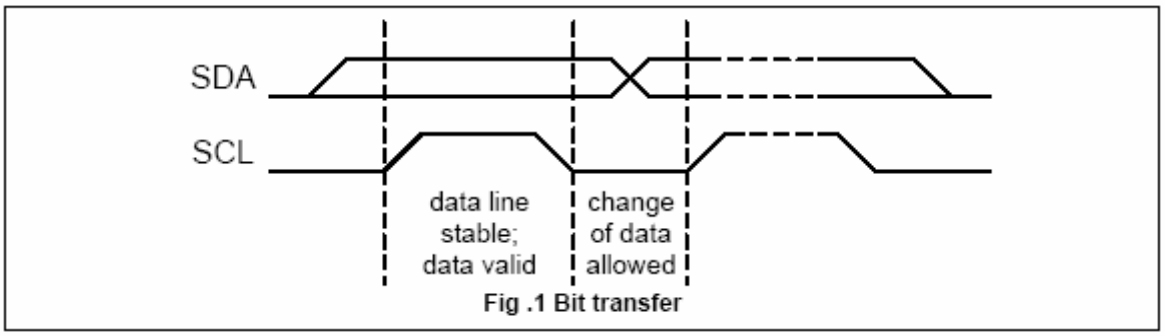


Fig .1 Bit transfer

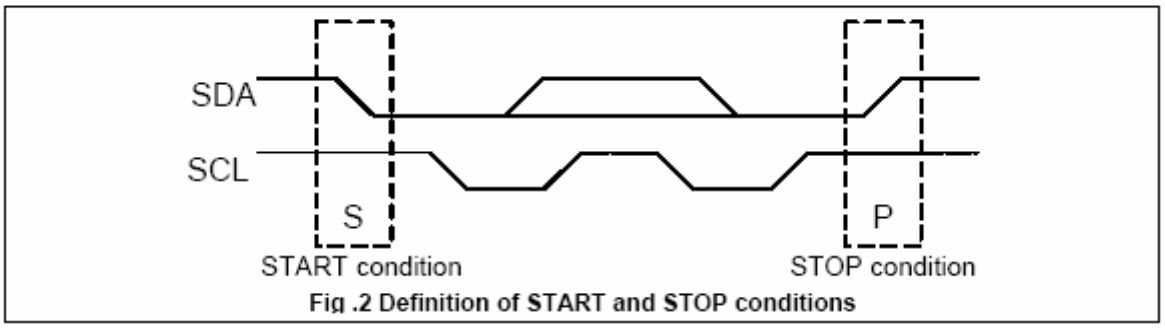


Fig .2 Definition of START and STOP conditions

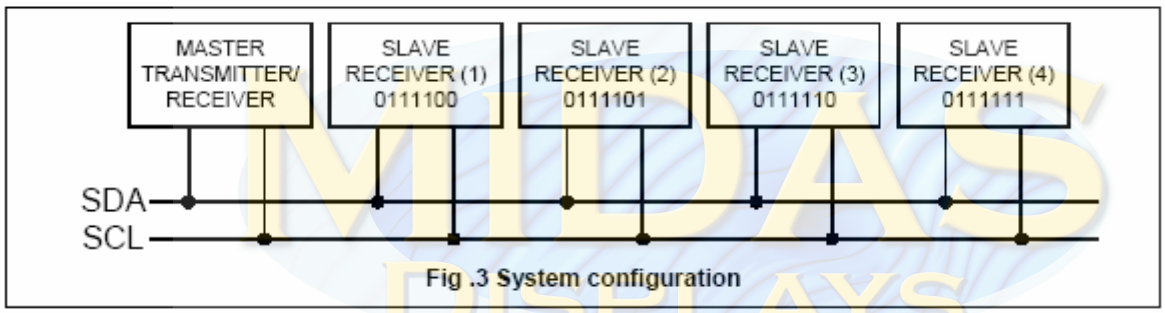


Fig .3 System configuration

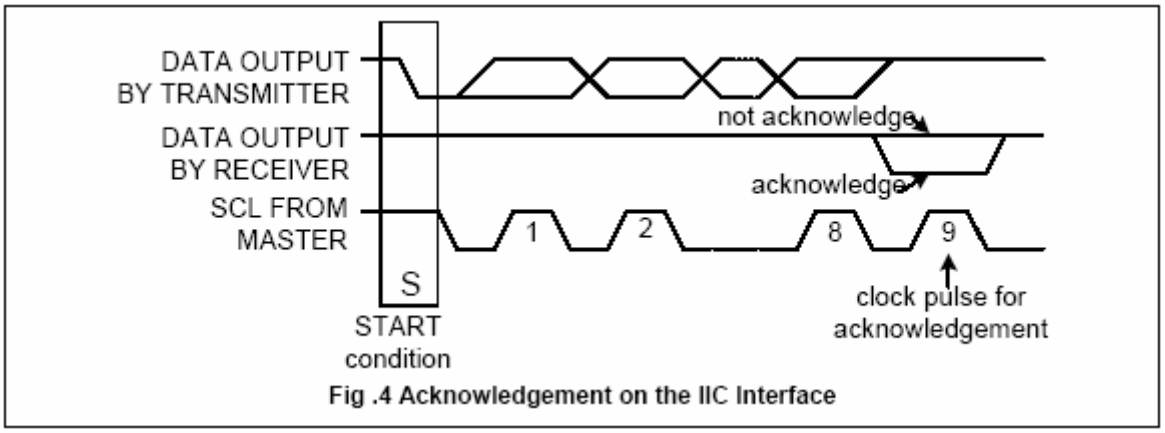


Fig .4 Acknowledgement on the IIC Interface

**I2C Interface protocol**

The ST7036 supports command, data write addressed slaves on the bus.

Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100 to 0111111) are reserved for the ST7036. The R/W is assigned to 0 for Write only.

The I2C Interface protocol is illustrated in Fig.5.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address.

All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of a control byte, which defines Co and RS, plus a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co).

After a control byte with a cleared Co bit, only data bytes will follow. The state of the RS bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the RS bit setting; either a series of display data bytes or command data bytes may follow. If the RS bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7036i device. If the RS bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I2C INTERFACE-bus master issues a STOP condition (P).

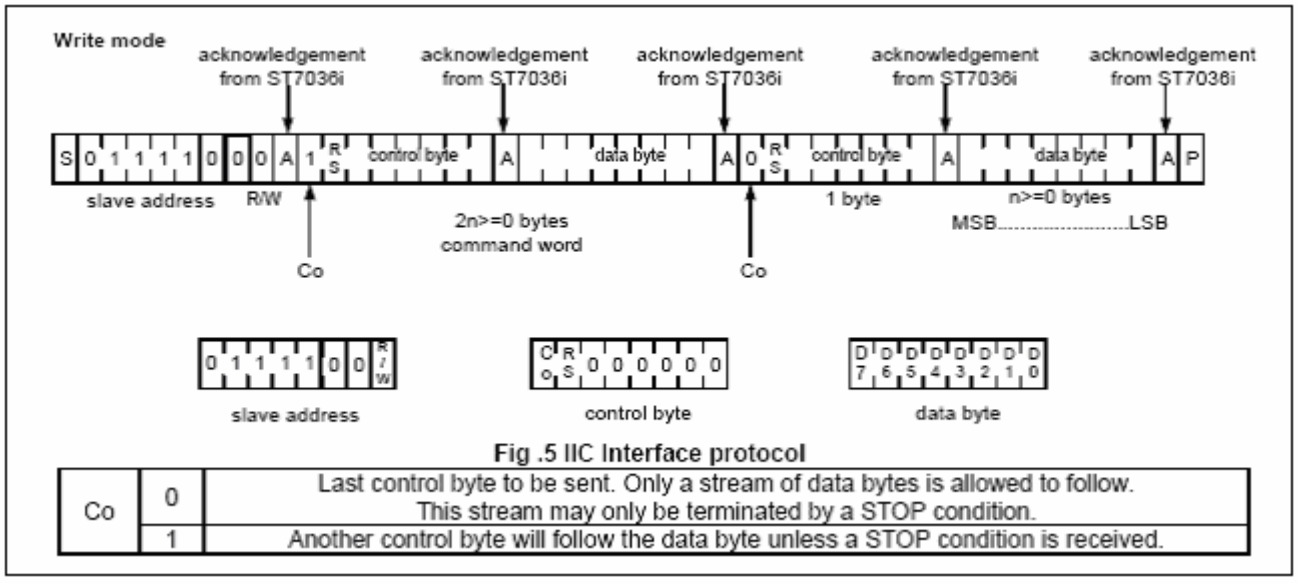



Fig .5 IIC Interface protocol

| | | |
|---|---|---|
| Co | 0 | Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition. |
| | 1 | Another control byte will follow the data byte unless a STOP condition is received. |

During write operation, two 8-bit registers are used. One is data register (DR), the other is instruction
register(IR).
The data register(DR) is used as temporary data storage place for being written into DDRAM/CGRAM/ICON
RAM, target RAM is selected by RAM address setting instruction. Each internal operation, writing into RAM, is done automatically. So to speak, after MPU writes data to DR, the data in DR is transferred into
DDRAM/CGRAM/ICON RAM automatically.
The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.
To select register, use RS bit input in IIC interface.

| RS | R/W | Operation |
|---|---|---|
| L | L | Instruction Write operation (MPU writes Instruction code into IR) |
| H | L | Data Write operation (MPU writes data into DR) |

Table 2. Various kinds of operations according to RS and R/W bits.

● **Busy Flag (BF)**
When BF = "High", it indicates that the internal operation is being processed. So during this time the next
instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High.
● **Address Counter (AC)**
Address Counter(AC) stores DDRAM/CGRAM/ICON RAM address, transferred from IR.
After writing into (reading from) DDRAM/CGRAM/ICON RAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.
● **Display Data RAM (DDRAM)**
Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80x 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 6 for the relationships between DDRAM addresses and positions on the liquid crystal display.
The DDRAM address (ADD ) is set in the address counter (AC) as hexadecimal.
● **1-line display (N3=0,N = 0) (Figure 7)**
When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the ST7036, 20 characters are displayed. See Figure 7.
When the display shift operation is performed, the DDRAM address shifts. See Figure 8.

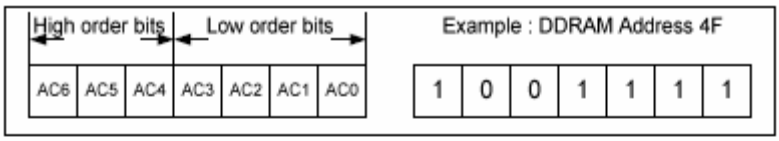



**Fig. 6 DDRAM Address**

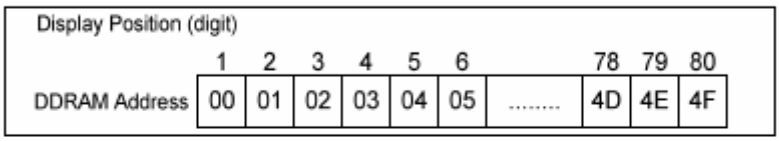



**Fig. 7 1-Line Display**

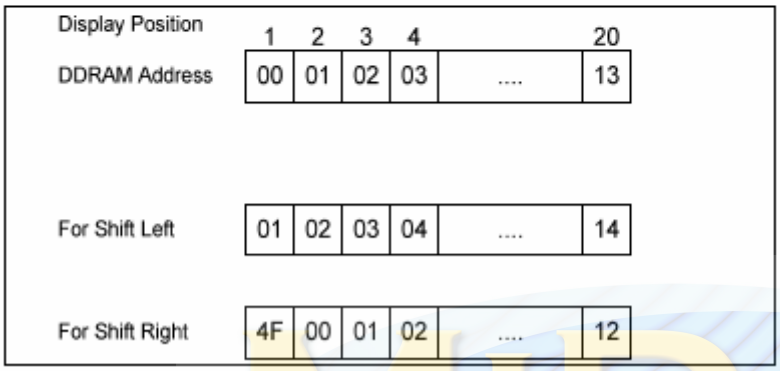



**Fig. 8 1-Line by 20-Character Display Example**



● **2-line display (N3=0,N = 1) (Figure 9)**

Case 1: When the number of display characters is less than 40 x _2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the ST7036 is used, 20 characters x _2 lines are displayed. See Figure 9.

When display shift operation is performed, the DDRAM address shifts. See Figure 10.

| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | | 38 | 39 | 40 |
|---|---|---|---|---|---|---|---|---|---|---|
| DDRAM Address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | 05 | ..... | 25 | 26 | 27 |
| | 40 | 41 | 42 | 43 | 44 | 45 | ..... | 65 | 66 | 67 |

Fig. 9 2-Line Display

| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | ..... | 10 | 11 | 12 | 13 |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | ..... | 50 | 51 | 52 | 53 |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | ..... | 11 | 12 | 13 | 14 |
| | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | ..... | 51 | 52 | 53 | 54 |
| For Shift Right | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | ..... | 0F | 10 | 11 | 12 |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | ..... | 4F | 50 | 51 | 52 |

Fig. 10 2-Line by 20-Character Display Example

**_ 3-line display (N3=1,N =1) (Figure 11)**

Case 1: When the number of display characters is less than 16 x _3 lines, the tree lines are displayed from the head. For example, when just the ST7036 is used, 16 characters x _3 lines are displayed. See Figure 11. When display shift operation is performed, the DDRAM address shifts. See Figure 12.

Display Position

| | 1 | 2 | 3 | 4 | 5 | 6 | | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|
| DDRAM Address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | 05 | ..... | 0D | 0E | 0F |
| | 10 | 11 | 12 | 13 | 14 | 15 | ..... | 1D | 1E | 1F |
| | 20 | 21 | 22 | 23 | 24 | 25 | ..... | 2D | 2E | 2F |

Fig. 11 3-Line Display

Display Position

| | 1 | 2 | 3 | 4 | 5 | 6 | | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|
| DDRAM Address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | 05 | ..... | 0D | 0E | 0F |
| | 10 | 11 | 12 | 13 | 14 | 15 | ..... | 1D | 1E | 1F |
| | 20 | 21 | 22 | 23 | 24 | 25 | ..... | 2D | 2E | 2F |

| | 1 | 2 | 3 | 4 | 5 | 6 | | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | ..... | 0E | 0F | 00 |
| | 11 | 12 | 13 | 14 | 15 | 16 | ..... | 1E | 1F | 10 |
| | 21 | 22 | 23 | 24 | 25 | 26 | ..... | 2E | 2F | 20 |

| | 1 | 2 | 3 | 4 | 5 | 6 | | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|
| For Shift Right | 0F | 00 | 01 | 02 | 03 | 04 | ..... | 0C | 0D | 0E |
| | 1F | 10 | 11 | 12 | 13 | 14 | ..... | 1C | 1D | 1E |
| | 2F | 20 | 21 | 22 | 23 | 24 | ..... | 2C | 2D | 2E |

Fig. 12 3-Line Display



● **Character Generator ROM (CGROM)**

The character generator ROM generates 5 x 8 dot character patterns from 8-bit character codes. It can generate 240/250/248/256 5 x 8 dot character patterns(select by OPR1/2 ITO pin). User-defined character patterns are also available by mask-programmed ROM.

● **Character Generator RAM (CGRAM)**

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 5 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

● **ICON RAM**

**In the ICON RAM, the user can rewrite icon pattern by program.**

**There are totally 80 dots for icon can be written.**

**See Table 6 for the relationship between ICON RAM address and data and the display patterns.**

● **Timing Generation Circuit**

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.

● **LCD Driver Circuit(N3=0)**

LCD Driver circuit has 17 common and 100 segment signals for LCD driving. Data from CGRAM/CGROM/ICON is transferred to 100 bit segment latch serially, and then it is stored to 100 bit shift latch. When each common is selected by 17 bit common register, segment data also output through segment driver from 100 bit segment latch. In case of 1-line display mode, COM1 ~ COM8(with COMI) have 1/9 duty, and in 2-line mode, COM1 ~ COM16(with COMI) have 1/17 duty ratio.

● **LCD Driver Circuit(N3=1)**

LCD Driver circuit has 25 common and 80 segment signals for LCD driving. Data from CGRAM/CGROM/ICON is transferred to 80 bit segment latch serially, and then it is stored to 80 bit shift latch. When each common is selected by 25 bit common register, segment data also output through segment driver from 80 bit segment latch. In case of 3-line display mode, COM1 ~ COM24(with COMI) have 1/25 duty.

*COM/SEG Output pins*

| N3 | COMI1 | COM [1:8] | SEG [1:5] | SEG [6:10] | SEG [11:90] | SEG [91:96] | SEG [97:100] | COM [9:16] | COMI2 |
|---|---|---|---|---|---|---|---|---|---|
| VSS | COMI1 | COM [1:8] | SEG [1:5] | SEG [6:10] | SEG [11:90] | SEG [91:96] | SEG [97:100] | COM [9:16] | COMI2 |
| VDD | NC | COM [5:12] | COM[4:1] + COMI1 | NC | SEG [1:80] | NC | COM [13:16] | COM [17:24] | COMI2 |

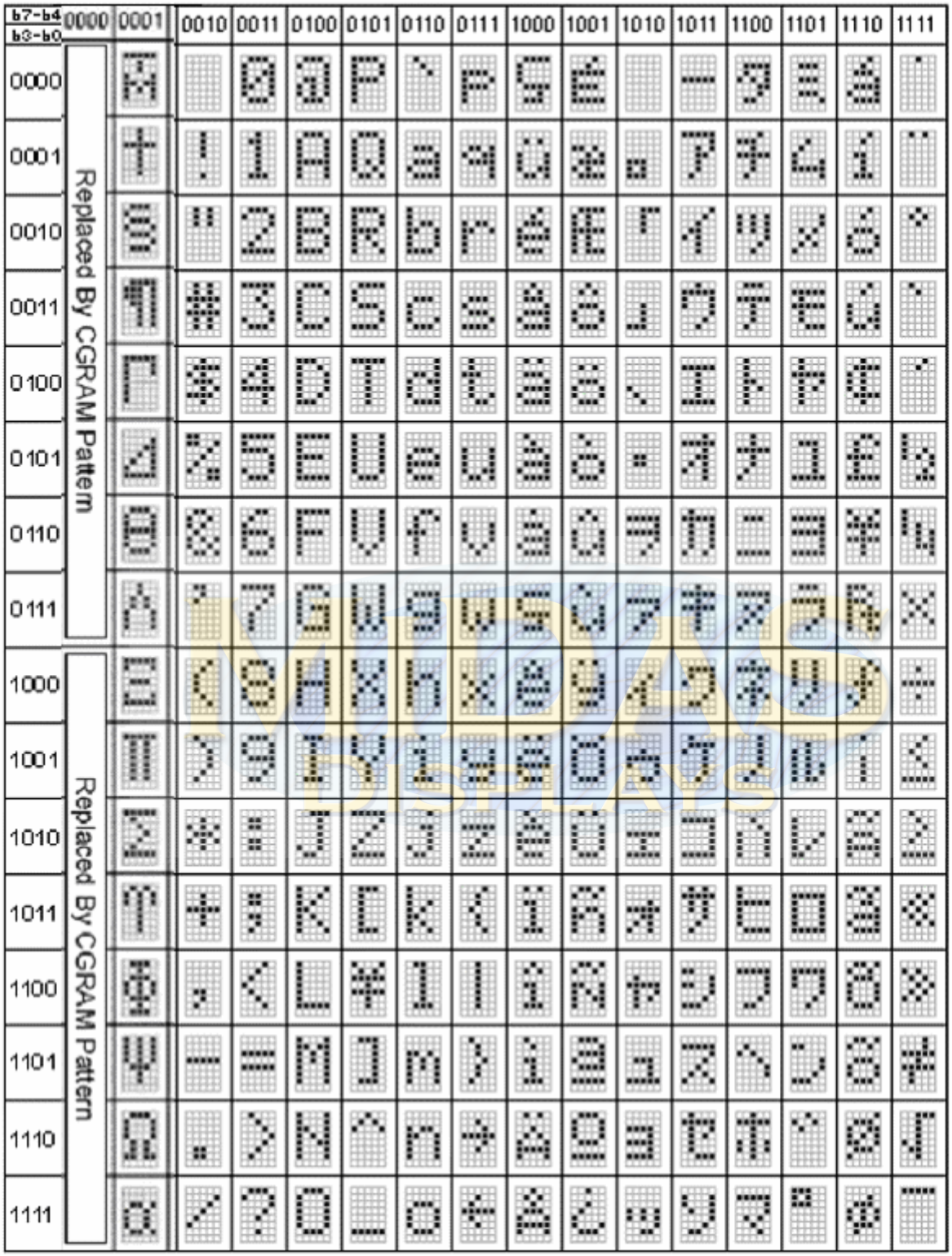
**Table 3. COM/SEG output define**

● **Cursor/Blink Control Circuit**

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Table 3. Correspondence between Character Codes and Character Patterns

ST7036 (ITO option OPR1=0, OPR2=0)



| Character Code (DDRAM Data) | | | | | | | | CGRAM Address | | | | | | Character Patterns (CGRAM Data) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | b5 | b4 | b3 | b2 | b1 | b0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 0 | 0 | 0 | 0 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | 1 | 1 |
| | | | | | 0 | 0 | 0 | | | | 0 | 0 | 1 | | | | 0 | 0 | 1 | 0 | 0 |
| | | | | | 0 | 0 | 0 | | | | 0 | 1 | 0 | | | | 0 | 0 | 1 | 0 | 0 |
| | | | | | 0 | 0 | 0 | | | | 0 | 1 | 1 | | | | 0 | 0 | 1 | 0 | 0 |
| | | | | | 0 | 0 | 0 | | | | 1 | 0 | 0 | | | | 0 | 0 | 1 | 0 | 0 |
| | | | | | 0 | 0 | 0 | | | | 1 | 0 | 1 | | | | 0 | 0 | 1 | 0 | 0 |
| | | | | | 0 | 0 | 0 | | | | 1 | 1 | 0 | | | | 0 | 0 | 1 | 0 | 0 |
| | | | | | 0 | 0 | 0 | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | - | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | 1 | 0 |
| | | | | | 0 | 0 | 1 | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 |
| | | | | | 0 | 0 | 1 | | | | 0 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 |
| | | | | | 0 | 0 | 1 | | | | 0 | 1 | 1 | | | | 1 | 1 | 1 | 1 | 0 |
| | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | | | | 1 | 0 | 1 | 0 | 0 |
| | | | | | 0 | 0 | 1 | | | | 1 | 0 | 1 | | | | 1 | 0 | 0 | 1 | 0 |
| | | | | | 0 | 0 | 1 | | | | 1 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 |
| | | | | | 0 | 0 | 1 | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 |

Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the T display example above can be selected by either character code 00H or 08H.
5. “1” for CGRAM data corresponds to display selection and “0” to non-selection,“-“ Indicates no effect.
6. Different OPR1/2 ITO option can select different CGRAM size.

When ICON RAM data is filled the corresponding position displayed is described as the following table.

When SHLS=1, ICON RAM map refer below table

| ICON Address | ICON RAM bits | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | D7~D5 | D4 | | D3 | | D2 | | D1 | | D0 | |
| | | N3 = 0 | N3 = 1 | N3 = 0 | N3 = 1 | N3 = 0 | N3 = 1 | N3 = 0 | N3 = 1 | N3 = 0 | N3 = 1 |
| 00H | - | S1/S81 | S1 | S2/S82 | S2 | S3/S83 | S3 | S4/S84 | S4 | S5/S85 | S5 |
| 01H | - | S6/S86 | S6 | S7/S87 | S7 | S8/S88 | S8 | S9/S89 | S9 | S10/S90 | S10 |
| 02H | - | S11/S91 | S11 | S12/S92 | S12 | S13/S93 | S13 | S14/S94 | S14 | S15/S95 | S15 |
| 03H | - | S16/S96 | S16 | S17/S97 | S17 | S18/S98 | S18 | S19/S99 | S19 | S20/S100 | S20 |
| 04H | - | S21 | S21 | S22 | S22 | S23 | S23 | S24 | S24 | S25 | S25 |
| 05H | - | S26 | S26 | S27 | S27 | S28 | S28 | S29 | S29 | S30 | S30 |
| 06H | - | S31 | S31 | S32 | S32 | S33 | S33 | S34 | S34 | S35 | S35 |
| 07H | - | S36 | S36 | S37 | S37 | S38 | S38 | S39 | S39 | S40 | S40 |
| 08H | - | S41 | S41 | S42 | S42 | S43 | S43 | S44 | S44 | S45 | S45 |
| 09H | - | S46 | S46 | S47 | S47 | S48 | S48 | S49 | S49 | S50 | S50 |
| 0AH | - | S51 | S51 | S52 | S52 | S53 | S53 | S54 | S54 | S55 | S55 |
| 0BH | - | S56 | S56 | S57 | S57 | S58 | S58 | S59 | S59 | S60 | S60 |
| 0CH | - | S61 | S61 | S62 | S62 | S63 | S63 | S64 | S64 | S65 | S65 |
| 0DH | - | S66 | S66 | S67 | S67 | S68 | S68 | S69 | S69 | S70 | S70 |
| 0EH | - | S71 | S71 | S72 | S72 | S73 | S73 | S74 | S74 | S75 | S75 |
| 0FH | - | S76 | S76 | S77 | S77 | S78 | S78 | S79 | S79 | S80 | S80 |

When SHLS=0, ICON RAM map refer below table

| ICON Address | ICON RAM bits | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | D7~D5 | D4 | | D3 | | D2 | | D1 | | D0 | |
| | | N3 = 0 | N3 = 1 | N3 = 0 | N3 = 1 | N3 = 0 | N3 = 1 | N3 = 0 | N3 = 1 | N3 = 0 | N3 = 1 |
| 00H | - | S100/S20 | S80 | S99/S19 | S79 | S98/S18 | S78 | S97/S17 | S77 | S96/S16 | S76 |
| 01H | - | S95/S15 | S75 | S94/S14 | S74 | S93/S13 | S73 | S92S12 | S72 | S91/S11 | S71 |
| 02H | - | S90/S10 | S70 | S89/S9 | S69 | S88/S8 | S68 | S87/S7 | S67 | S86/S6 | S66 |
| 03H | - | S85/S5 | S65 | S84/S4 | S64 | S83/S3 | S63 | S82/S2 | S62 | S81/S1 | S61 |
| 04H | - | S80 | S60 | S79 | S59 | S78 | S58 | S77 | S57 | S76 | S56 |
| 05H | - | S75 | S55 | S74 | S54 | S73 | S53 | S72 | S52 | S71 | S51 |
| 06H | - | S70 | S50 | S69 | S49 | S68 | S48 | S67 | S47 | S66 | S46 |
| 07H | - | S65 | S45 | S64 | S44 | S63 | S43 | S62 | S42 | S61 | S41 |
| 08H | - | S60 | S40 | S59 | S39 | S58 | S38 | S57 | S37 | S56 | S36 |
| 09H | - | S55 | S35 | S54 | S34 | S53 | S33 | S52 | S32 | S51 | S31 |
| 0AH | - | S50 | S30 | S49 | S29 | S48 | S28 | S47 | S27 | S46 | S26 |
| 0BH | - | S45 | S25 | S44 | S24 | S43 | S23 | S42 | S22 | S41 | S21 |
| 0CH | - | S40 | S20 | S39 | S19 | S38 | S18 | S37 | S17 | S36 | S16 |
| 0DH | - | S35 | S15 | S34 | S14 | S33 | S13 | S32 | S12 | S31 | S11 |
| 0EH | - | S30 | S10 | S29 | S9 | S28 | S8 | S27 | S7 | S26 | S6 |
| 0FH | - | S25 | S5 | S24 | S4 | S23 | S3 | S22 | S2 | S21 | S1 |

Table 6 ICON RAM map

## ■ Instructions

There are four categories of instructions that:

- **Designate ST7036 functions, such as display format, data length, etc.**
- **Set internal RAM addresses**
- **Perform data transfer with internal RAM**
- **Others**
- **instruction table at “Normal mode”**

(when “EXT” option pin connect to VDD, the instruction set follow below table)

| Instruction | Instruction Code | | | | | | | | | | Description | Instruction Execution Time | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | OSC= 380kHz | OSC= 540kHz | OSC= 700kHz |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM. and set DDRAM address to "00H" from AC | 1.08 ms | 0.76 ms | 0.59 ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.08 ms | 0.76 ms | 0.59 ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor move direction and specifies display shift. These operations are performed during data write and read. | 26.3 µs | 18.5 µs | 14.3 µs |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | D=1:entire display on<br>C=1:cursor on<br>B=1:cursor position on | 26.3 µs | 18.5 µs | 14.3 µs |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | S/C and R/L:<br>Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. | 26.3 µs | 18.5 µs | 14.3 µs |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | X | X | X | DL: interface data is 8/4 bits<br>N: number of line is 2/1 | 26.3 µs | 18.5 µs | 14.3 µs |
| Set CGRAM | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter | 26.3 µs | 18.5 µs | 14.3 µs |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter | 26.3 µs | 18.5 µs | 14.3 µs |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0 | 0 | 0 |
| Write Data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM) | 26.3 µs | 18.5 µs | 14.3 µs |
| Read Data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM) | 26.3 µs | 18.5 µs | 14.3 µs |

Note:

Be sure the ST7036 is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7036. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

## ➢ instruction table at “Extension mode”

(when “EXT” option pin connect to Vss, the instruction set follow below table)

| Instruction | Instruction Code | | | | | | | | | | Description | Instruction Execution Time | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | OSC= 380kHz | OSC= 540kHz | OSC= 700kHz |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM. and set DDRAM address to "00H" from AC | 1.08 ms | 0.76 ms | 0.59 ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.08 ms | 0.76 ms | 0.59 ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor move direction and specifies display shift. These operations are performed during data write and read. | 26.3 µs | 18.5 µs | 14.3 µs |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | D=1:entire display on<br>C=1:cursor on<br>B=1:cursor position on | 26.3 µs | 18.5 µs | 14.3 µs |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | DH | IS2 | IS1 | DL: interface data is 8/4 bits<br>N: number of line is 2/1<br>DH: double height font<br>IS[2:1]: instruction table select | 26.3 µs | 18.5 µs | 14.3 µs |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter | 26.3 µs | 18.5 µs | 14.3 µs |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0 | 0 | 0 |
| Write Data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM/ICONRAM) | 26.3 µs | 18.5 µs | 14.3 µs |
| Read Data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM/ICONRAM) | 26.3 µs | 18.5 µs | 14.3 µs |

| Instruction table 0(IS[2:1]=[0,0]) | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | S/C and R/L:<br>Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. | 26.3 µs | 18.5 µs | 14.3 µs |
| Set CGRAM | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter | 26.3 µs | 18.5 µs | 14.3 µs |

| Instruction table 1(IS[2:1]=[0,1]) | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bias Set | 0 | 0 | 0 | 0 | 0 | 1 | BS | 1 | 0 | FX | BS=1:1/4 bias<br>BS=0:1/5 bias<br>FX: fixed on high in 3-line application and fixed on low in other applications. | 26.3 µs | 18.5 µs | 14.3 µs |
| Set ICON Address | 0 | 0 | 0 | 1 | 0 | 0 | AC3 | AC2 | AC1 | AC0 | Set ICON address in address counter. | 26.3 µs | 18.5 µs | 14.3 µs |
| Power/ICON Control/ Contrast Set | 0 | 0 | 0 | 1 | 0 | 1 | Ion | Bon | C5 | C4 | Ion: ICON display on/off<br>Bon: set booster circuit on/off<br>C5,C4: Contrast set for internal follower mode. | 26.3 µs | 18.5 µs | 14.3 µs |
| Follower Control | 0 | 0 | 0 | 1 | 1 | 0 | Fon | Rab 2 | Rab 1 | Rab 0 | Fon: set follower circuit on/off<br>Rab2~0:<br>select follower amplified ratio. | 26.3 µs | 18.5 µs | 14.3 µs |
| Contrast Set | 0 | 0 | 0 | 1 | 1 | 1 | C3 | C2 | C1 | C0 | Contrast set for internal follower mode. | 26.3 µs | 18.5 µs | 14.3 µs |

| Instruction table 2(IS[2:1]=[1,0]) | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Double Height Position Select | 0 | 0 | 0 | 0 | 0 | 1 | UD | X | x | x | UD: Double height position select | 26.3 µs | 18.5 µs | 14.3 µs |
| Reserved | 0 | 0 | 0 | 1 | X | X | X | X | X | X | Do not use (reserved for test) | 26.3 µs | 18.5 µs | 14.3 µs |

*Instruction table 3(IS[2:1]=[1,1]):Do not use (reserved for test)*

# 10.Instruction Description

- **Clear Display**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

- **Return Home**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X |

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

- **Entry Mode Set**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

Set the moving direction of cursor and display.

➢ **I/D : Increment / decrement of DDRAM address (cursor or blink)**
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

➢ **S: Shift of entire display**
When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

| S | I/D | Description |
|---|---|---|
| H | H | Shift the display to the left |
| H | L | Shift the display to the right |

- **Display ON/OFF**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.

- **D : Display ON/OFF control bit**
  When D = "High", entire display is turned on.
  When D = "Low", display is turned off, but display data is remained in DDRAM.
- **C : Cursor ON/OFF control bit**
  When C = "High", cursor is turned on.
  When C = "Low", cursor is disappeared in current display, but I/D register remains its data.
- **B : Cursor Blink ON/OFF control bit**
  When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
  When B = "Low", blink is off.


- **Cursor or Display Shift**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X |

- **S/C: Screen/Cursor select bit**
  When S/C="High", Screen is controlled by R/L bit.
  When S/C="Low", Cursor is controlled by R/L bit.
- **R/L: Right/Left**
  When R/L="High", set direction to right.
  When R/L="Low", set direction to left.

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

| S/C | R/L | Description | AC Value |
|---|---|---|---|
| L | L | Shift cursor to the left | AC=AC-1 |
| L | H | Shift cursor to the right | AC=AC+1 |
| H | L | Shift display to the left. Cursor follows the display shift | AC=AC |
| H | H | Shift display to the right. Cursor follows the display shift | AC=AC |

- **Function Set**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | DL | N | DH | IS2 | IS1 |

➢ **DL : Interface data length control bit**

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

➢ **N : Display line number control bit**

When N = "High", 2-line display mode is set.

When N = "Low", it means 1-line display mode.

When "N3" option pin connect to VDD, N must set "N=1".

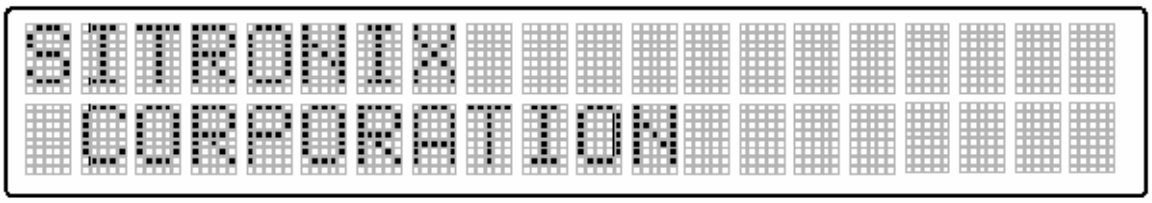
➢ **DH : Double height font type control bit**

When DH = " High " and N= "Low", display font is selected to double height mode(5x16 dot),RAM address can only use 00H~27H.

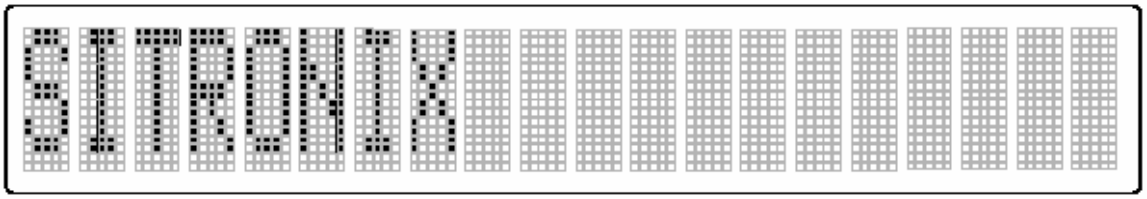
When DH= "High" and N= "High", it is forbidden.

When DH = " Low ", display font is normal (5x8 dot).

| N | DH | EXT option pin connect to high | | EXT option pin connect to low | |
|---|---|---|---|---|---|
| | | Display Lines | Character Font | Display Lines | Character Font |
| L | L | 1 | 5x8 | 1 | 5x8 |
| L | H | 1 | 5x8 | 1 | 5x16 |
| H | L | 2 | 5x8 | 2 | 5x8 |
| H | H | 2 | 5x8 | Forbidden | |



2 line mode normal display (DH=0/N=1)



1 line mode with double height font (DH=1/N=0)

➢ **IS[2:1]: instruction table select**

When IS[2:1]=(0,0): normal instruction be selected(refer instruction table 0)

When IS[2:1]=(0,1):extension instruction be selected(refer instruction table 1 )

When IS[2:1]=(1,0):extension instruction be selected(refer instruction table 2 )

When IS[2:1]=(1,1):Do not use (reserved for test)

● **Double height position set: IS[2:1]=(1,0)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | UD | X | X | X |

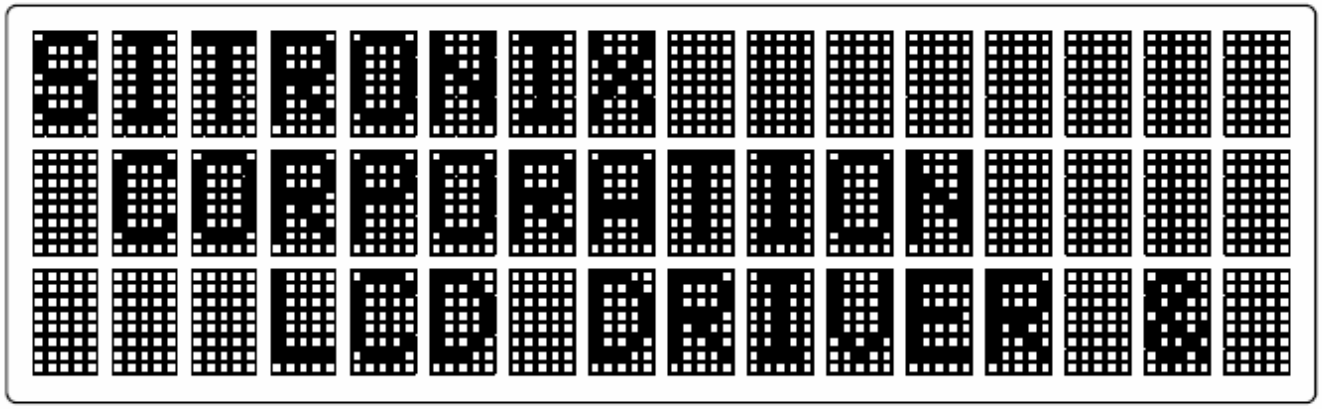
➢ **UD: Select double height font display position of screen.(N3=VDD)**

When UD = "High", double height font is show on Com1~Com16.

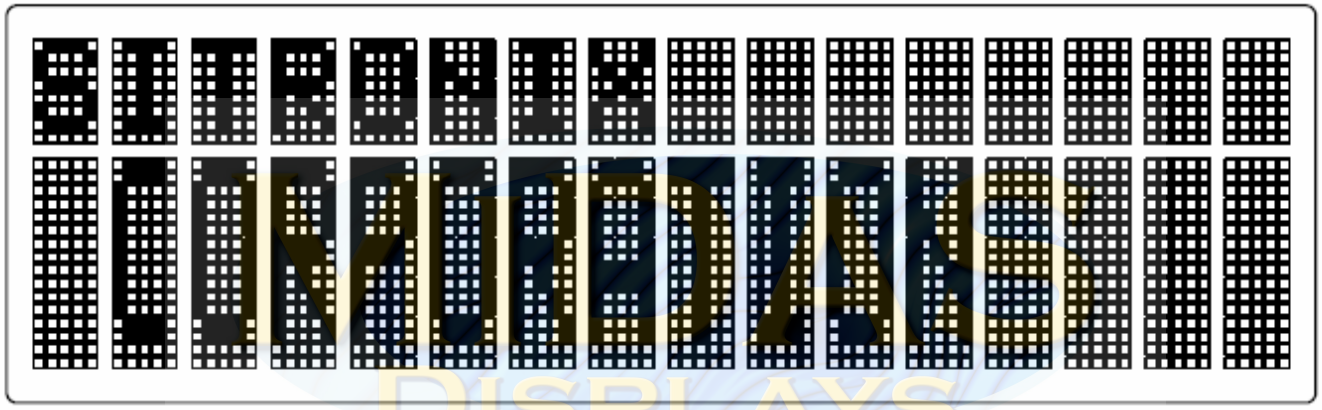
| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | AC3 | AC2 | AC1 | AC0 |

When UD = "Low", double height font is show on Com9~Com24.

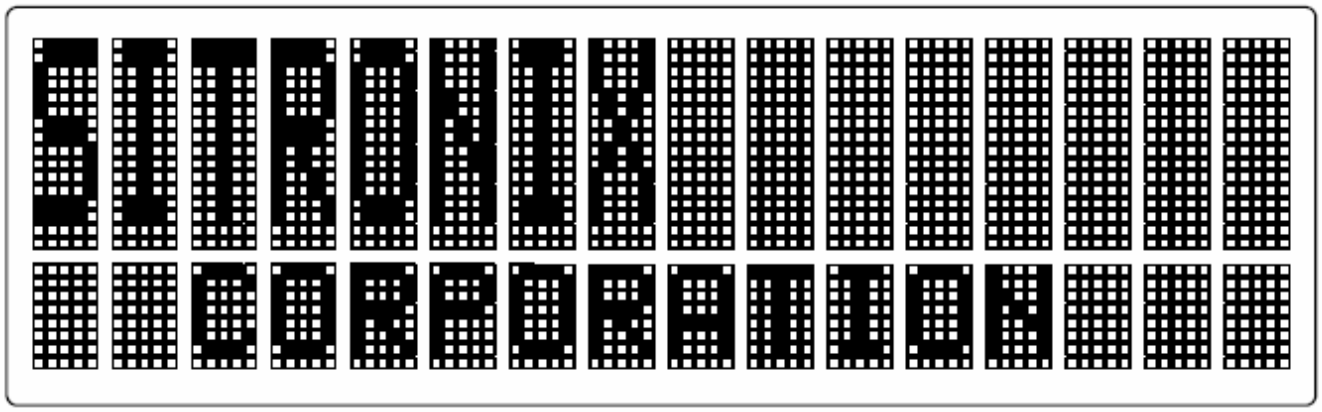
| DH | UD | 2 LINES(N3=VSS) | 3 LINES(N3=VDD) |
|---|---|---|---|
| H | H | Com1~Com16 Double Height | Com1~Com16 Double Height<br>Com17~Com24 Normal Display |
| H | L | Com1~Com16 Double Height | Com1~Com8 Normal Display<br>Com9~Com24 Double Height |
| L | X | Normal Display | Normal Display |



3 Line mode normal display (DH = 0 / N = 1 / UD = don`t care )



COM1 ..8 is normal , COM9 .. 24 is a double height font (DH = 1 / N = 1 / UD = 0 )



COM17 ..24 is normal , COM1 .. 16 is a double height font (DH = 1 / N = 1 / UD = 1 )

- **Set CGRAM Address**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

- **Set DDRAM Address**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

In 3-line display mode (N3=1, N=1), DDRAM address in the 1st line is from "00H" to "OFH", DDRAM in the 2nd line is from "10H" to "1FH", and DDRAM in the 3rd line is from "20H" to "2FH".

- **Read Busy Flag and Address**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

When BF = "High", indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

- **Write Data to CGRAM,DDRAM or ICON RAM**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Write binary 8-bit data to **CGRAM,DDRAM or ICON RAM**

The selection of RAM from DDRAM, CGRAM or ICON RAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set, ICON RAM address set. RAM set instruction can also determine the AC

direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from CGRAM,DDRAM or ICON RAM**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Read binary 8-bit data from DDRAM/CGRAM./ICON RAM

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

- **Bias Set**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | BS | 1 | 0 | FX |

➢ **BS: bias selection**
When BS="High", the bias will be 1/4
When BS="Low", the bias will be 1/5
BS will be invalid when external bias resistors are used(OPF1=1,OPF2=1)

➢ **FX:** must be fixed on high in 3-line application and fixed on low in other applications.

- **Set ICON RAM address**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | AC3 | AC2 | AC1 | AC0 |

Set ICON RAM address to AC.

This instruction makes ICON data available from MPU.

When IS=1 at Extension mode,

The ICON RAM address is from "00H" to "0FH".

- **Power/ICON control/Contrast set(high byte)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 1 | Ion | Bon | C5 | C4 |

- **Ion: set ICON display on/off**
  When Ion = "High", ICON display on.
  When Ion = "Low", ICON display off.
- **Bon: switch booster circuit**
  Bon can only be set when internal follower is used (OPF1=0,OPF2=0).
  When Bon = "High", booster circuit is turn on.
  When Bon = "Low", booster circuit is turn off.
- **C5,C4 : Contrast set(high byte)**
  C5,C4,C3,C2,C1,C0 can only be set when internal follower is used (OPF1=0,OPF2=0).They can more precisely adjust the input reference voltage of V0 generator. The details please refer to the supply voltage for LCD driver.

- **Follower control**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | Fon | Rab 2 | Rab 1 | Rab 0 |

- **Fon: switch follower circuit**
  Fon can only be set when internal follower is used (OPF1=0,OPF2=0).
  When Fon = "High", internal follower circuit is turn on.
  When Fon = "Low", internal follower circuit is turn off.
  Note that Fon must be set to "Low" if (OPF1, OPF2) is not (0,0).

- **Rab2,Rab1,Rab0 : V0 generator amplified ratio**
  Rab2,Rab1,Rab0 can only be set when internal follower is used (OPF1=0,OPF2=0).They can adjust the amplified ratio of V0 generator. The details please refer to the supply voltage for LCD driver.

- **Contrast set(low byte)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | C3 | C2 | C1 | C0 |

- **C3,C2,C1,C0:Contrast set(low byte)**
  C5,C4,C3,C2,C1,C0 can only be set when internal follower is used (OPF1=0,OPF2=0).They can more precisely adjust the input reference voltage of V0 generator. The details please refer to the supply voltage for LCD driver.

# 11. Backlight Information

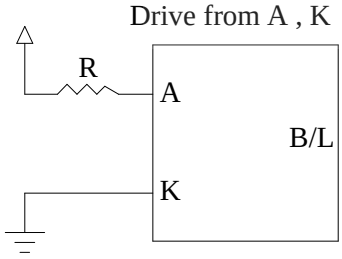
## Specification

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | TEST CONDITION |
|---|---|---|---|---|---|---|
| Supply Current | ILED | 28.8 | 32 | 50 | mA | V=3.5V |
| Supply Voltage | V | 3.4 | 3.5 | 3.6 | V | |
| Reverse Voltage | VR | — | — | 5 | V | — |
| Luminous Intensity (Without LCD) | IV | 409.6 | 512.0 | — | $CD/M^2$ | ILED=32mA |
| LED Life Time | — | — | 50000 | — | Hr. | $I_{LED} \leqq 32mA$ |
| Color | White | | | | | |

**Note: The LED of B/L is drive by current only；driving voltage is only for reference**
**To make driving current in safety area (waste current between minimum and maximum).**

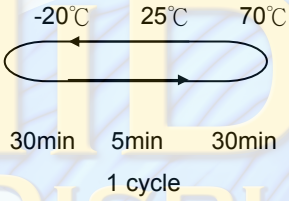
**Note1 :50K hours is only an estimate for reference.**

LED B\L Drive Method
Drive from A , K



# 12. Reliability

### Content of Reliability Test (wide temperature, -20℃~70℃)

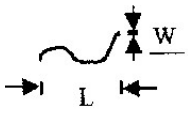
| Environmental Test | | | |
|---|---|---|---|
| **Test Item** | **Content of Test** | **Condition** | **Note** |
| High Temperature storage | Endurance test applying the high storage temperature for a long time. | 80℃<br>200hrs | 2 |
| Low Temperature storage | Endurance test applying the high storage temperature for a long time. | -30℃<br>200hrs | 1,2 |
| High Temperature Operation | Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time. | 70℃<br>200hrs | - |
| Low Temperature Operation | Endurance test applying the electric stress under low temperature for a long time. | -20℃<br>200hrs | 1 |
| High Temperature/<br>Humidity Operation | The module should be allowed to stand at 60℃,90%RH max<br>For 96hrs under no-load condition excluding the polarizer,<br>Then taking it out and drying it at normal temperature. | 60℃,90%RH<br>96hrs | 1,2 |
| Thermal shock resistance | The sample should be allowed stand the following 10 cycles of operation<br>  <br> | -20℃/70℃<br>10 cycles | - |
| Vibration test | Endurance test applying the vibration during transportation and using. | fixed amplitude: 15mm<br>Vibration. Frequency: 10~55Hz.<br>One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes | 3 |
| Static electricity test | Endurance test applying the electric stress to the terminal. | VS=800V,RS=1.5kΩ<br>CS=100pF<br>1 time | —— |

**Note1: No dew condensation to be observed.**

**Note2: The function test shall be conducted after 4 hours storage at the normal temperature and humidity after remove from the test chamber.**

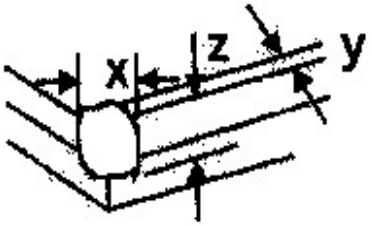
**Note3: Vibration test will be conducted to the product itself without putting it in a container.**

# 13. Inspection specification

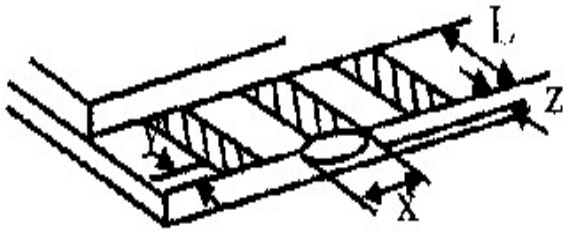
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.<br>1.2 Missing character, dot or icon.<br>1.3 Display malfunction.<br>1.4 No function or no display.<br>1.5 Current consumption exceeds product specifications.<br>1.6 LCD viewing angle defect.<br>1.7 Mixed product types.<br>1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on LCD (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.<br>2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing<br>Φ=( x + y ) / 2</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)<br> 

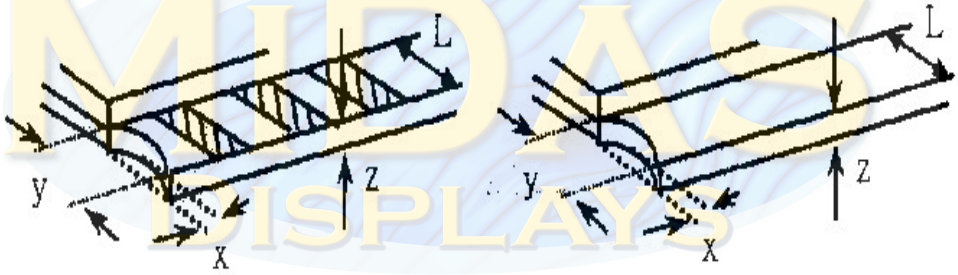
<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><th>Size Φ</th><th>Acceptable Q TY</th></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50＜Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00＜Φ</td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
</table>

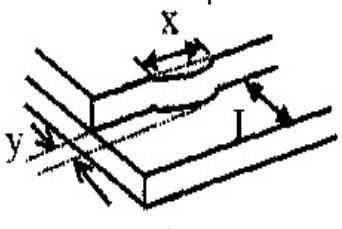
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 LCD black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>
Symbols Define:<br>
x: Chip length y: Chip width z: Chip thickness<br>
k: Seal width t: Glass thickness a: LCD side length<br>
L: Electrode pad length:<br><br>
6.1 General glass chip :<br>
6.1.1 Chip on panel surface and crack between panels:<br>


<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is total length of each chip.<br><br>
6.1.2 Corner crack:<br>


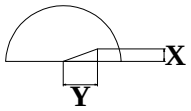
<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is the total length of each chip.
</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>06</td><td>Glass crack</td><td>
Symbols :<br>
x: Chip length y: Chip width z: Chip thickness<br>
k: Seal width t: Glass thickness a: LCD side length<br>
L: Electrode pad length<br>
6.2 Protrusion over terminal :<br>
6.2.1 Chip on electrode pad :<br>


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
6.2.2 Non-conductive portion:<br>


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦ L</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.<br>
⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.<br>
6.2.3 Substrate protuberance and internal crack.<br>


<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>x ≦ a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

| NO | Item | Criterion | AQL |
|---|---|---|---|
| 07 | Cracked glass | The LCD with extensive crack is not acceptable. | 2.5 |
| 08 | Backlight elements | 8.1 Illumination source flickers when lit.<br>8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards.<br>8.3 Backlight doesn't light or color wrong. | 0.65<br>2.5<br><br>0.65 |
| 09 | Bezel | 9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination.<br>9.2 Bezel must comply with job specifications. | 2.5<br>0.65 |
| 10 | PCB、COB | 10.1 COB seal may not have pinholes larger than 0.2mm or contamination.<br>10.2 COB seal surface may not have pinholes through to the IC.<br>10.3 The height of the COB should not exceed the height indicated in the assembly diagram.<br>10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places.<br>10.5 No oxidation or contamination PCB terminals.<br>10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts.<br>10.7 The jumper on the PCB should conform to the product characteristic chart.<br>10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down.<br>10.9 The Scraping testing standard for Copper Coating of PCB<br>  <br>**X * Y<=2mm$^2$** | 2.5<br><br>2.5<br>0.65<br><br>2.5<br><br>2.5<br>0.65<br><br><br>0.65<br><br>2.5<br><br>2.5 |
| 11 | Soldering | 11.1 No un-melted solder paste may be present on the PCB.<br>11.2 No cold solder joints, missing solder connections, oxidation or icicle.<br>11.3 No residue or solder balls on PCB.<br>11.4 No short circuits in components on PCB. | 2.5<br>2.5<br><br>2.5<br>0.65 |

| NO | Item | Criterion | AQL |
|---|---|---|---|
| 12 | General appearance | 12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP.<br>12.2 No cracks on interface pin (OLB) of TCP.<br>12.3 No contamination, solder residue or solder balls on product.<br>12.4 The IC on the TCP may not be damaged, circuits.<br>12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it causes the interface pin to sever.<br>12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color.<br>12.7 Sealant on top of the ITO circuit has not hardened.<br>12.8 Pin type must match type in specification sheet.<br>12.9 LCD pin loose or missing pins.<br>12.10 Product packaging must the same as specified on packaging specification sheet.<br>12.11 Product dimension and structure must conform to product specification sheet. | 2.5<br>0.65<br>2.5<br>2.5<br>2.5<br>2.5<br>2.5<br>0.65<br>0.65<br>0.65<br>0.65 |

## 14. Precautions in use of LCD Modules

1. Avoid applying excessive shocks to the module or making any alterations or modifications to it.
2. Don’t make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
3. Don’t disassemble the LCM.
4. Don’t operate it above the absolute maximum rating.
5. Don’t drop, bend or twist LCM.
6. Soldering: only to the I/O terminals.
7. Storage: please storage in anti-static electricity container and clean environment.
8. Midas have the right to change the passive components
   (Resistors,capacitors and other passive components will have different appearance and color caused by the different supplier.)
9. Midas have the right to change the PCB Rev.

# 15. Material List of Components for RoHs

1. Midas hereby declares that all of or part of products, including, but not limited to, the LCM, accessories or packages, manufactured and/or delivered to your company (including your subsidiaries and affiliated company) directly or indirectly by our company (including our subsidiaries or affiliated companies) do not intentionally contain any of the substances listed in all applicable EU directives and regulations, including the following substances.

Exhibit A：The Harmful Material List

| Material | (Cd) | (Pb) | (Hg) | (Cr6+) | PBBs | PBDEs |
|---|---|---|---|---|---|---|
| Limited Value | 100 ppm | 1000 ppm | 1000 ppm | 1000 ppm | 1000 ppm | 1000 ppm |
| Above limited value is set up according to RoHS. | | | | | | |

2. Process for RoHS requirement：
   (1) Use the Sn/Ag/Cu soldering surface；the surface of Pb-free solder is rougher than we used before.
   (2) Heat-resistance temp.：
   Reflow：250℃, 30 seconds Max.；
   Connector soldering wave or hand soldering：320℃, 10 seconds max.
   (3) Temp. curve of reflow, max. Temp.：235±5℃；
   Recommended customer's soldering temp. of connector：280℃, 3 seconds.

# 16. Recommendable storage

1. Place the panel or module in the temperature 25°C±5℃ and the humidity below 65% RH
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module

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