Address: Midas Components Ltd, Electra House, 32 Southtown Road, Great Yarmouth, Norfolk, England, NR31 ODU
Email:sales@midascomponents.co.uk
Website:www.midascomponents.co.uk
Tel:+44(0)1493 602602
Fax:+44(0)1493 665111

Midas LCD Part Number System

MC	COG	132033	A	*	6	W	*	*	-	S	N	T	L	W	*	*
1	2	3	4	5	6	7	8	9	-	10	11	12	13	14	15	16

1 = **MC:** Midas Components

2 = **Blank:** COB (chip on board) **COG:** chip on glass

3 = **No of dots** (e.g. 240064 = 240 x 64 dots) (e.g. 21605 = 2 x 16 5mm C.H.)

4 = **Series**

5 = **Series Variant:** A to Z **– see addendum**

6 = **3:** 3 o'clock **6:** 6 o'clock **9:** 9 o'clock **12:** 12 o'clock

7 = S: Normal (0 to + 50 deg C) **W:** Wide temp. (-20 to + 70 deg C) **X:** Extended temp (-30 + 80 Deg C)

8 = **Character Set**

Blank: Standard (English/Japanese)
C: Chinese Simplified (Graphic Displays only)
CB: Chinese Big 5 (Graphic Displays only)
H: Hebrew
K: European (std) (English/German/French/Greek)
L: English/Japanese (special)
M: European (English/Scandinavian)
R: Cyrillic
W: European (English/Greek)
U: European (English/Scandinavian/Icelandic)

9 = **Bezel Height** (where applicable / available)

	Top of Bezel to Top of PCB	Common (via pins 1 and 2)	Array or Edge Lit
Blank	9.5mm / not applicable	Common	Array
2	8.9 mm	Common	Array
3	7.8 mm	Separate	Array
4	7.8 mm	Common	Array
5	9.5 mm	Separate	Array
6	7 mm	Common	Array
7	7 mm	Separate	Array
8	6.4 mm	Common	Edge
9	6.4 mm	Separate	Edge
A	5.5 mm	Common	Edge
B	5.5 mm	Separate	Edge
D	6.0mm	Separate	Edge
E	5.0mm	Separate	Edge
F	4.7mm	Common	Edge
G	3.7mm	Separate	EL

10 = **T:** TN **S:** STN **B:** STN Blue **G:** STN Grey **F:** FSTN **F2:** FFSTN

11 = **P:** Positive **N:** Negative

12 = **R:** Reflective **M:** Transmissive **T:** Transflective

13 = **Backlight: Blank:** Reflective **L:** LED

14 = **Backlight Colour: Y:** Yellow-Green **W:** White **B:** Blue **R:** Red **A:** Amber **O:** Orange **G:** Green **RGB:** R.G.B.

15 = **Driver Chip:** **Blank:** Standard **I:** I²C **T:** Toshiba T6963C **A:** Avant SAP1024B **R:** Raio RA8835

16 = **Voltage Variant**: e.g. **3** = 3v

2. General Specification

The Features of the Module is description as follow:

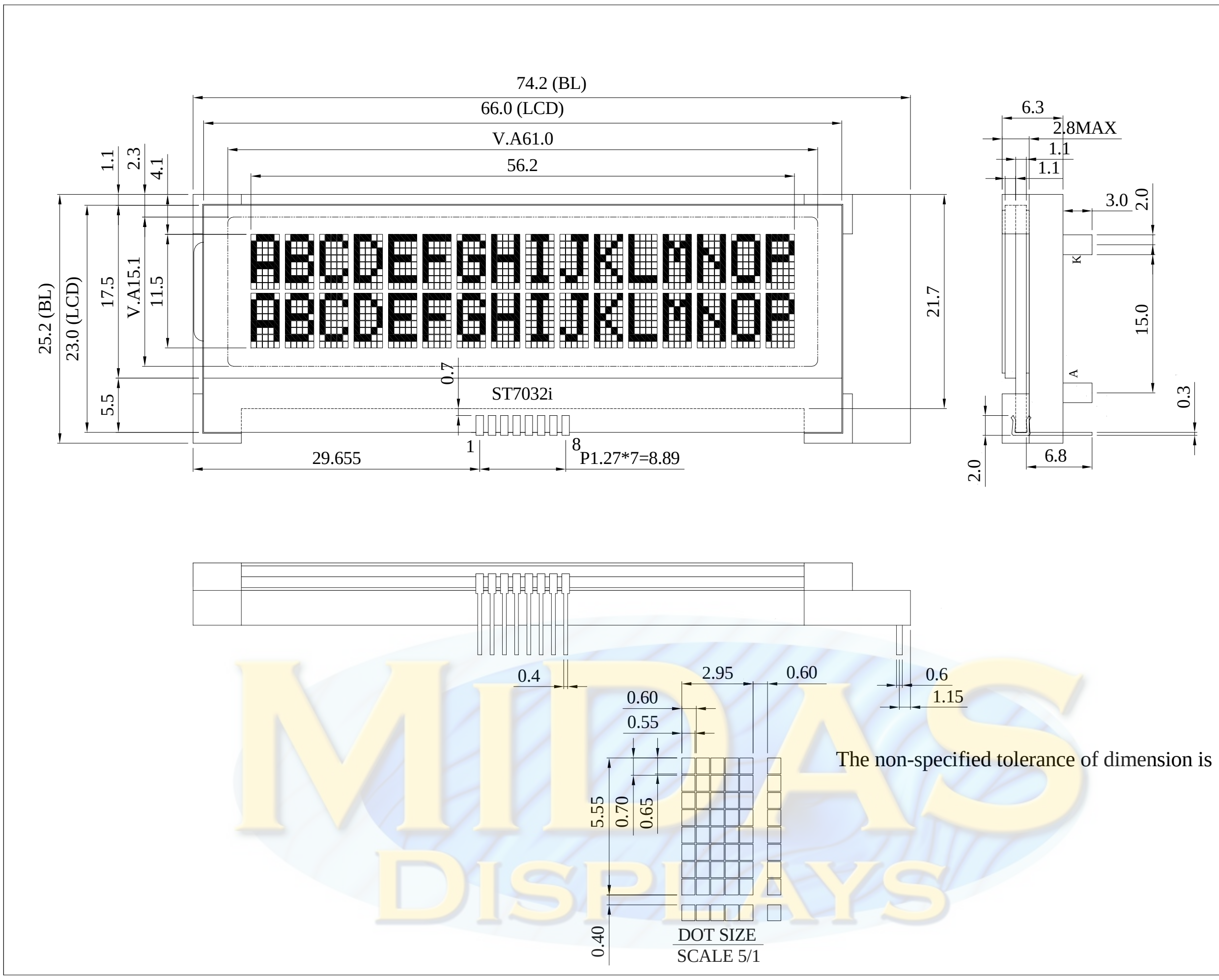
- Module dimension: 74.2x 25.2 x6.3 (max.) mm3
- View area: 61.0 x 15.1 mm2
- Active area: 56.2 x 11.5 mm2
- Number of Characters: 16 characters x 2 Lines
- Dot size: 0.55 x 0.65 mm2
- Dot pitch: 0.60 x 0.70 mm2
- Character size: 2.95 x 5.55 mm2
- Character pitch: 3.55 x 5.95 mm2
- LCD type: STN Positive, Yellow Green Transflective
- Duty: 1/16 , 1/5 Bias
- View direction: 6 o'clock
- Backlight Type: LED, White

4. Interface Pin Function

Pin No.	Symbol	Level	Description
1	VOUT		DC/DC voltage converter. Connect a capacitor between this terminal and VIN when the built-in booster is used.
2	CAP1N		For voltage booster circuit(VDD-VSS) External capacitor about 0.1u~4.7uf
3	CAP1P		
4	VDD	3.0/5.0V	Power supply
5	VSS		GND
6	SDA		(In I2C interface DB7 (SDA) is input data. SDA and SCL must connect to I2C bus (I2C bus is to connect a resister between SDA/SCL and the power of I2C bus).
7	SCL		(In I2C interface DB6 (SCL) is clock input. SDA and SCL must connect to I2C bus (I2C bus is to connect a resister between SDA/SCL and the power of I2C bus).
8	RST		RESET *

* Please note, if you do not wish to use Reset, it should be tied high

5.Outline dimension

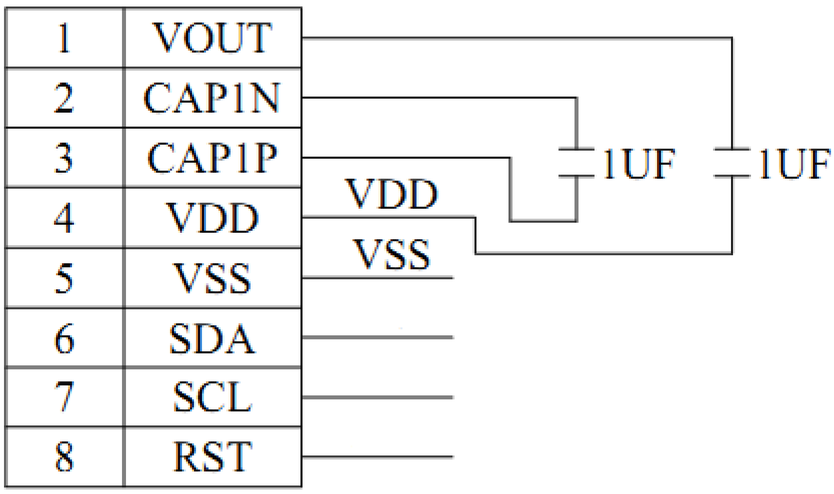


PIN NO.	SYMBOL
1	VOUT
2	CAP1N
3	CAP1P
4	VDD
5	VSS
6	SDA
7	SCL
8	RST

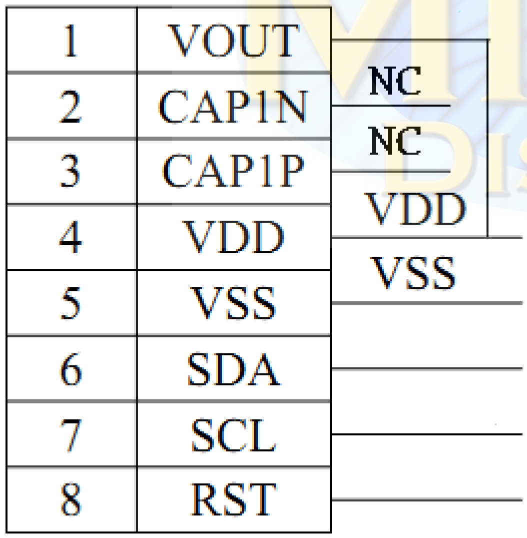
The non-specified tolerance of dimension is ±0.2mm.

Application schematic

VDD=3.0V



VDD=5.0V



INITIALIZE: (3V)

```
MOV    I2C_CONTROL,#00H ;WRITE COMMAND
MOV    I2C_DATA,#38H    ;Function Set
LCALL  WRITE_CODE
MOV    I2C_CONTROL,#00H ;WRITE COMMAND
MOV    I2C_DATA,#39H    ;Function Set
LCALL  WRITE_CODE
MOV    I2C_DATA,#14H    ;Internal OSC frequency
LCALL  WRITE_CODE
MOV    I2C_DATA,#74H    ;Contrast set
LCALL  WRITE_CODE
MOV    I2C_DATA,#54H        ;Power/ICON control/Contrast set
LCALL  WRITE_CODE
MOV    I2C_DATA,#6FH        ;Follower control
LCALL  WRITE_CODE
MOV    I2C_DATA,#0CH    ;Display ON/OFF
LCALL  WRITE_CODE
MOV    I2C_DATA,#01H    ;Clear Display
LCALL  WRITE_CODE
```

INITIALIZE: (5V)

```
MOV     I2C_CONTROL,#00H;WRITE COMMAND
MOV     I2C_DATA,#38H      ;Function Set
LCALL   WRITE_CODE
MOV     I2C_CONTROL,#00H;WRITE COMMAND
MOV     I2C_DATA,#39H      ;Function Set
LCALL   WRITE_CODE
MOV     I2C_DATA,#14H      ;Internal OSC frequency
LCALL   WRITE_CODE
MOV     I2C_DATA,#79H      ;Contrast set
LCALL   WRITE_CODE
MOV     I2C_DATA,#50H          ;Power/ICON control/Contrast set
LCALL   WRITE_CODE
MOV     I2C_DATA,#6CH          ;Follower control
LCALL   WRITE_CODE
MOV     I2C_DATA,#0CH      ;Display ON/OFF
LCALL   WRITE_CODE
MOV     I2C_DATA,#01H      ;Clear Display
LCALL   WRITE_CODE
```

6. Function Description

System Interface

This chip has all four kinds of interface type with MPU: 4-bit bus, 8-bit bus. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR); the other is instruction register (IR).

The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/ICON RAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM/ICON RAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

Using RS input pin to select command or data in 4-bit/8-bit bus mode.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy Flag(DB7) and address counter (DB0 ~ DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Table 1. Various kinds of operations according to RS and R/W bits.

I2C interface

It just only could write Data or Instruction to ST7032 by the IIC Interface.

It could not read Data or Instruction from ST7032 (except Acknowledge signal).

SCL: serial clock input

SDA: serial data input

Slaver address could only set to 0111110, no other slaver address could be set

The I2C interface send RAM data and executes the commands sent via the I2C Interface. It could send data bit to the RAM.

The I2C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.1.

START AND STOP CONDITIONS

line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.2.

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.3.

· Transmitter: the device, which sends the data to the bus

· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer

· Slave: the device addressed by a master

· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message

· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted

· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Acknowledge is not Busy Flag in I2C interface.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated in Fig.4.

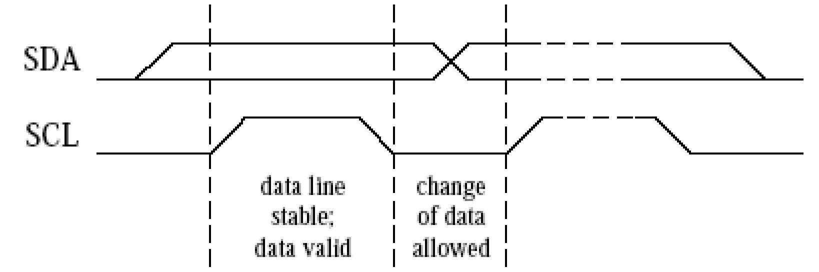


Figure 1. Bit transfer

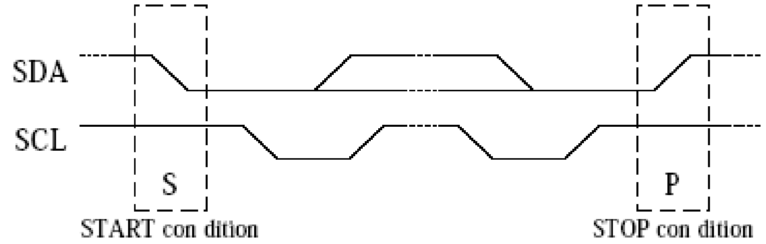


Figure 2. Definition of START and STOP conditions

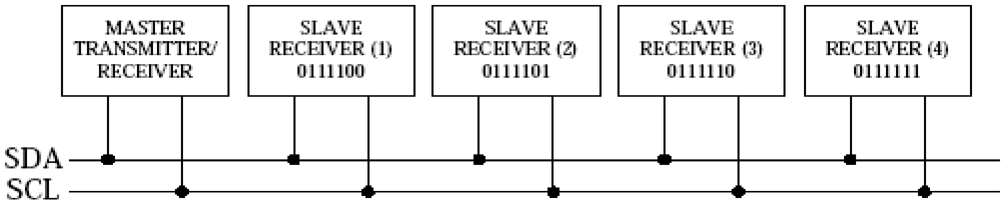


Figure 3. System configuration

I2C Interface protocol

The ST7032 supports command, data write addressed slaves on the bus.

Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first.

Only one 7-bit slave addresses (0111110) is reserved for the ST7032. The R/W is assigned to 0 for Write only.

The I2C Interface protocol is illustrated in Fig.5.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address.

All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of a control byte, which defines Co and RS, plus a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the RS bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the RS bit setting; either a series of display data bytes or command data bytes may follow. If the RS bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7032i device. If the RS bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I2C INTERFACE-bus master issues a STOP condition (P).

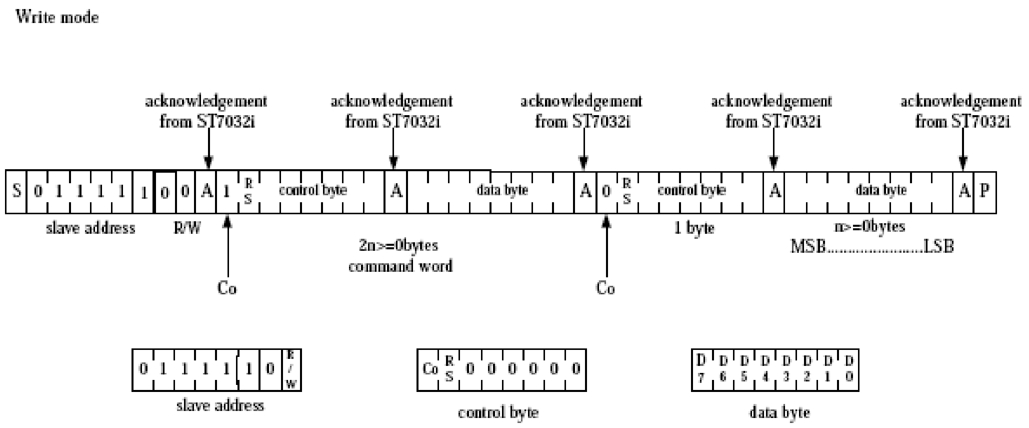


Figure 5. 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition.
	1	Another control byte will follow the data byte unless a STOP condition is received.

During write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register
(IR).
The data register (DR) is used as temporary data storage place for being written into DDRAM/CGRAM/ICON
RAM, target RAM is selected by RAM address setting instruction. Each internal operation, writing into RAM, is
done automatically. So to speak, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.
The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.
To select register, use RS input in I2C interface.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
H	L	Data Write operation (MPU writes data into DR)

Table 2. Various kinds of operations according to RS and R/W bits.

Busy Flag (BF)

When BF = "High”, it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High.

Address Counter (AC)

Address Counter (AC) stores DDRAM/CGRAM/ICON RAM address, transferred from IR.

After writing into (reading from) DDRAM/CGRAM/ICON RAM, AC is automatically increased (decreased) by 1.

When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.

Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 x 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 7 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (ADD) is set in the address counter (AC)as hexadecimal.

Ø 1-line display (N = 0) (Figure 8)

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the ST7032, 16 characters are displayed. See Figure 8.

When the display shift operation is performed, the DDRAM address shifts. See Figure 9.

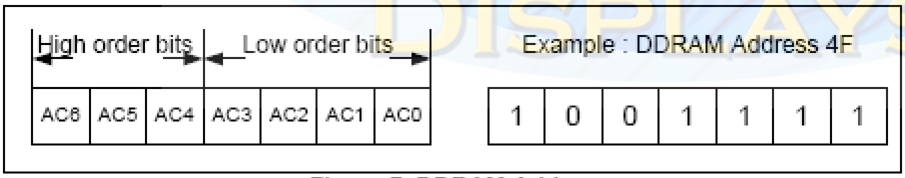


Figure 7. DDRAM Address

Display Position (digit)	1	2	3	4	5	6		78	79	80
DDRAM Address	00	01	02	03	04	05	....	4D	4E	4F

Figure 8. 1-Line Display

Display Position	1	2	3	4		16
DDRAM Address	00	01	02	03	....	0F
For Shift Left	01	02	03	04	....	10
For Shift Right	4F	00	01	02	....	0E

Figure 9. 1-Line by 16-Character Display Example

Ø 2-line display (N = 1) (Figure 10)

Case 1: When the number of display characters is less than 40 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. See Figure 10.

Display Position	1	2	3	4	5	6		38	39	40
DDRAM Address (hexadecimal)	00	01	02	03	04	05	....	25	26	27
	40	41	42	43	44	45	....	65	66	67

Figure 10. 2-Line Display

Case 2: For a 16-character 2-line display See Figure 11.

When display shift operation is performed, the DDRAM address shifts. See Figure 11.

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
For Shift Left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
For Shift Right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

Figure 11. 2-Line by 16-Character Display Example

Character Generator ROM (CGROM)

The character generator ROM generates 5 x 8 dot character patterns from 8-bit character codes. It can generate 240/250/248/256 5 x 8 dot character patterns (select by OPR1/2 ITO pin). User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 3 to show the character patterns stored in CGRAM.

See Table 4 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

ICON RAM

In the ICON RAM, the user can rewrite icon pattern by program.

There are totally 80 dots for icon can be written.

See Table 5 for the relationship between ICON RAM address and data and the display patterns.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.(In I2C interface the reading function is invalid.)

LCD Driver Circuit

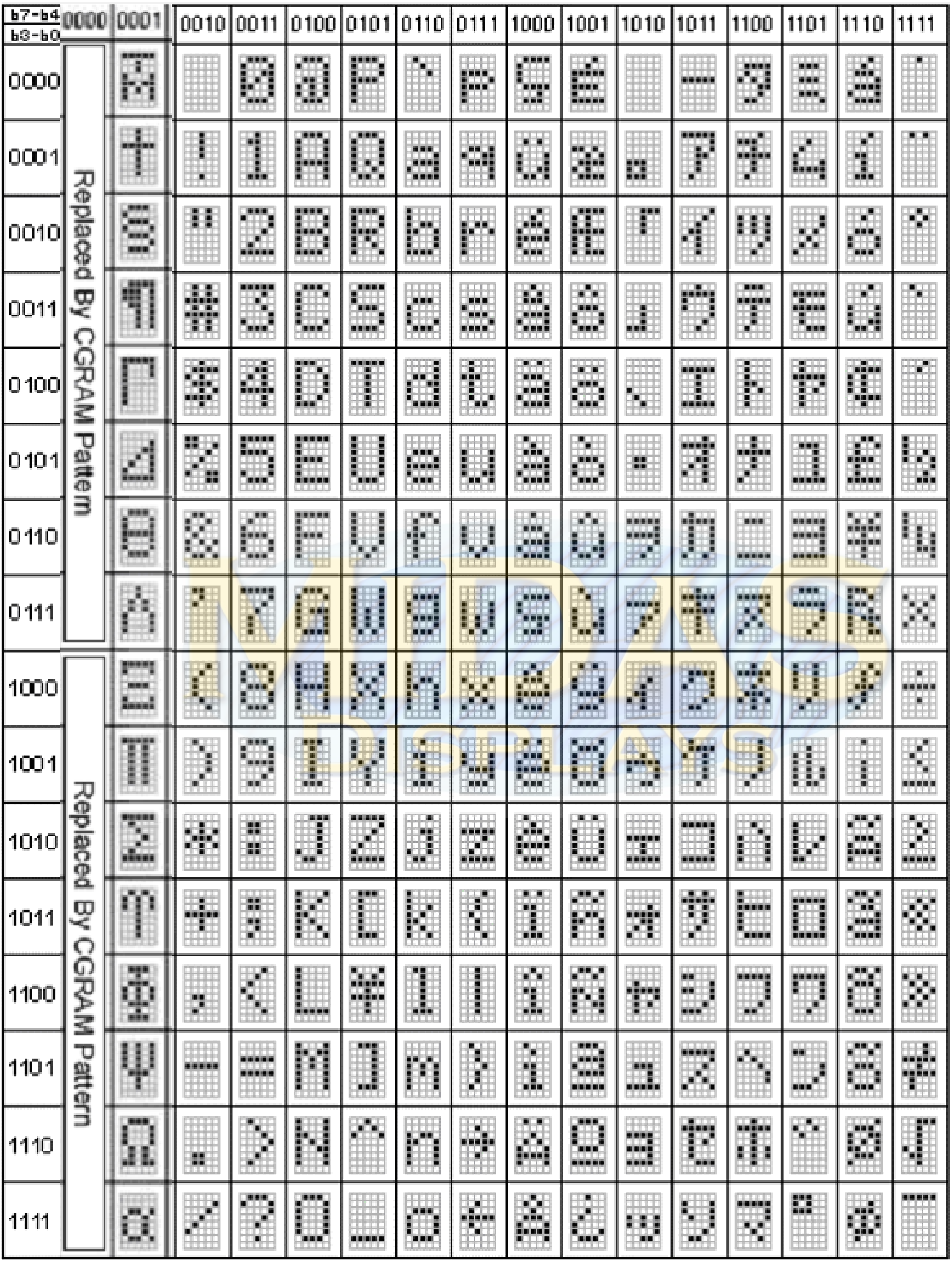
LCD Driver circuit has 17 common and 80 segment signals for LCD driving. Data from CGRAM/CGROM/ICON is transferred to 80 bit segment latch serially, and then it is stored to 80 bit shift latch. When each common is selected by 17 bit common register, segment data also output through segment driver from 80 bit segment latch.

Cursor/Blink Control Circuit

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Table 3. Correspondence between Character Codes and Character Patterns

ST7032-0D (ITO option OPR1=0, OPR2=0)



Character Code (DDRAM Data)								CGRAM Address						Character Patterns (CGRAM Data)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	-	0	0	0	0	0	0	0	0	0	-	-	-	1	1	1	1	1
					0	0	0				0	0	1				0	0	1	0	0
					0	0	0				0	1	0				0	0	1	0	0
					0	0	0				0	1	1				0	0	1	0	0
					0	0	0				1	0	0				0	0	1	0	0
					0	0	0				1	0	1				0	0	1	0	0
					0	0	0				1	1	0				0	0	1	0	0
					0	0	0				1	1	1				0	0	0	0	0
0	0	0	0	-	0	0	1	0	0	1	0	0	0	-	-	-	1	1	1	1	0
					0	0	1				0	0	1				1	0	0	0	1
					0	0	1				0	1	0				1	0	0	0	1
					0	0	1				0	1	1				1	1	1	1	0
					0	0	1				1	0	0				1	0	1	0	0
					0	0	1				1	0	1				1	0	0	1	0
					0	0	1				1	1	0				1	0	0	0	1
					0	0	1				1	1	1				0	0	0	0	0

Table 4. Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 4, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. “1” for CGRAM data corresponds to display selection and “0” to non-selection,“-“ Indicates no effect.
6. Different OPR1/2 ITO option can select different CGRAM size.

When SHLS=1, ICON RAM map refer below table

ICON address	ICON RAM bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	-	-	-	S1	S2	S3	S4	S5
01H	-	-	-	S6	S7	S8	S9	S10
02H	-	-	-	S11	S12	S13	S14	S15
03H	-	-	-	S16	S17	S18	S19	S20
04H	-	-	-	S21	S22	S23	S24	S25
05H	-	-	-	S26	S27	S28	S29	S30
06H	-	-	-	S31	S32	S33	S34	S35
07H	-	-	-	S36	S37	S38	S39	S40
08H	-	-	-	S41	S42	S43	S44	S45
09H	-	-	-	S46	S47	S48	S49	S50
0AH	-	-	-	S51	S52	S53	S54	S55
0BH	-	-	-	S56	S57	S58	S59	S60
0CH	-	-	-	S61	S62	S63	S64	S65
0DH	-	-	-	S66	S67	S68	S69	S70
0EH	-	-	-	S71	S72	S73	S74	S75
0FH	-	-	-	S76	S77	S78	S79	S80

When SHLS=0, ICON RAM map refer below table

ICON address	ICON RAM bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	-	-	-	S80	S79	S78	S77	S76
01H	-	-	-	S75	S74	S73	S72	S71
02H	-	-	-	S70	S69	S68	S67	S66
03H	-	-	-	S65	S64	S63	S62	S61
04H	-	-	-	S60	S59	S58	S57	S56
05H	-	-	-	S55	S54	S53	S52	S51
06H	-	-	-	S50	S49	S48	S47	S46
07H	-	-	-	S45	S44	S43	S42	S41
08H	-	-	-	S40	S39	S38	S37	S36
09H	-	-	-	S35	S34	S33	S32	S31
0AH	-	-	-	S30	S29	S28	S27	S26
0BH	-	-	-	S25	S24	S23	S22	S21
0CH	-	-	-	S20	S19	S18	S17	S16
0DH	-	-	-	S15	S14	S13	S12	S11
0EH	-	-	-	S10	S9	S8	S7	S6
0FH	-	-	-	S5	S4	S3	S2	S1

Table 5. ICON RAM map

When ICON RAM data is filled the corresponding position displayed is described as the following table.

. Instructions

There are four categories of instructions that:

- **Designate ST7032 functions, such as display format, data length, etc.**
- **Set internal RAM addresses**
- **Perform data transfer with internal RAM**
- **Others**

. **instruction table at “Normal mode”**

Ø **instruction table at “Extension mode”**

(when “EXT” option pin connect to VSS, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 380KHz	OSC= 540kHz	OSC= 700KHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	DH	*0	IS	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS: instruction table select	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us

Note * : this bit is for test command , and must always set to “0”

Instruction table 0(IS=0)														
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us

Instruction table 1(IS=1)														
Internal OSC frequency	0	0	0	0	0	1	BS	F2	F1	F0	BS=1:1/4 bias BS=0:1/5 bias F2~0: adjust internal OSC frequency for FR frequency.	26.3 us	18.5 us	14.3 us
Set ICON address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.	26.3 us	18.5 us	14.3 us
Power/ICON control/Contrast set	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion: ICON display on/off Bon: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us
Follower control	0	0	0	1	1	0	Fon	Rab 2	Rab 1	Rab 0	Fon: set follower circuit on/off Rab2~0: select follower amplified ratio.	26.3 us	18.5 us	14.3 us
Contrast set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us

7.Instruction Description

- Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

- Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM do not change.

- Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

Ø I/D : Increment / decrement of DDRAM address (cursor or blink)

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

Ø S: Shift of entire display

When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If

S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1": shift left, I/D = "0" : shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

- Display ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

Ø D : Display ON/OFF control bit

When D = "High", entire display is turned on.

When D = "Low", display is turned off, but display data is remained in DDRAM.

Ø C : Cursor ON/OFF control bit

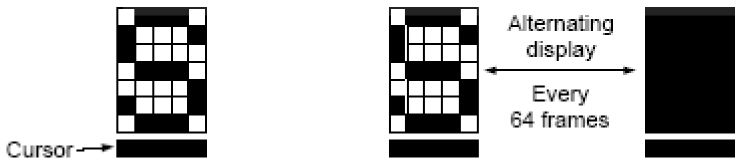
When C = "High", cursor is turned on.

When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

Ø B : Cursor Blink ON/OFF control bit

When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.

When B = "Low", blink is off.



- Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

Ø S/C: Screen/Cursor select bit

When S/C="High", Screen is controlled by R/L bit.

When S/C="Low", Cursor is controlled by R/L bit.

Ø **R/L: Right/Left**

When R/L=”High”, set direction to right.

When R/L=”Low”, set direction to left.

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC Value
L	L	Shift cursor to the left	AC=AC-1
L	H	Shift cursor to the right	AC=AC+1
H	L	Shift display to the left. Cursor follows the display shift	AC=AC
H	H	Shift display to the right. Cursor follows the display shift	AC=AC

- **Function Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	DH	0	IS

Ø **DL : Interface data length control bit**

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When in 4-bit bus mode, it needs to transfer 4-bit data by two times.

Ø **N : Display line number control bit**

When N = "High", 2-line display mode is set.

When N = "Low", it means 1-line display mode.

Ø **DH : Double height font type control bit**

When DH = " High " and N= “Low”, display font is selected to double height mode(5x16 dot),RAM address can only use 00H~27H.

When DH= “High” and N= “High”, it is forbidden.

When DH = " Low ", display font is normal (5x8 dot).

N	DH	EXT option pin connect to high		EXT option pin connect to low	
		Display Lines	Character Font	Display Lines	Character Font
L	L	1	5x8	1	5x8
L	H	1	5x8	1	5x16
H	L	2	5x8	2	5x8
H	H	2	5x8	Forbidden	

Ø **IS : normal/extension instruction select**

When IS=" High", extension instruction be selected (refer extension instruction table)

When IS=" Low", normal instruction be selected (refer normal instruction table)

- **Set CGRAM Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

- **Set DDRAM Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

- **Read Busy Flag and Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

When BF = “High”, indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

- **Write Data to CGRAM,DDRAM or ICON RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to **CGRAM, DDRAM or ICON RAM**

The selection of RAM from DDRAM, CGRAM or ICON RAM, is set by the previous address set instruction

: DDRAM address set, CGRAM address set, ICON RAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from CGRAM,DDRAM or ICON RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/ICON RAM

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

※ **Read data must be “set address” before this instruction.**

- **Bias selection/Internal OSC frequency adjust**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	BS	F2	F1	F0

Ø **BS: bias selection**

When BS=”High”, the bias will be 1/4

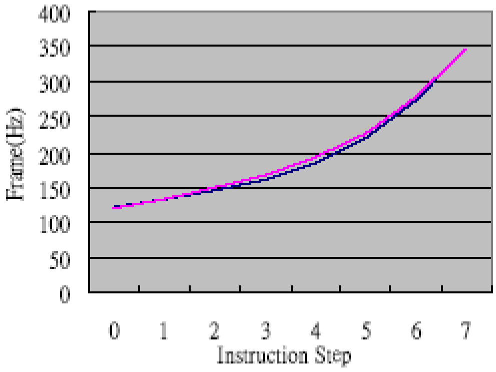
When BS=”Low”, the bias will be 1/5

BS will be invalid when external bias resistors are used (OPF1=1, OPF2=1)

Ø **F2,F1,F0 : Internal OSC frequency adjust**

When CLS connect to high, that instruction can adjust OSC and Frame frequency.

Internal frequency adjust			Frame frequency (Hz) (2 line mode)	
F2	F1	F0	VDD = 3.0 V	VDD = 5.0 V
0	0	0	122	120
0	0	1	131	133
0	1	0	144	149
0	1	1	161	167
1	*0*	*0*	*183*	*192*
1	0	1	221	227
1	1	0	274	277
1	1	1	347	347



- **Set ICON RAM address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	AC3	AC2	AC1	AC0

Set ICON RAM address to AC.

This instruction makes ICON data available from MPU.

When IS=1 at Extension mode,

The ICON RAM address is from "00H" to "0FH".

- **Power/ICON control/Contrast set(high byte)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	ION	BON	C5	C4

Ø Ion: set ICON display on/off

When Ion = "High", ICON display on.

When Ion = "Low", ICON display off.

Ø Bon: switch booster circuit

Bon can only be set when internal follower is used (OPF1=0, OPF2=0).

When Bon = "High", booster circuit is turn on.

When Bon = "Low", booster circuit is turn off.

Ø C5,C4 : Contrast set(high byte)

C5,C4,C3,C2,C1,C0 can only be set when internal follower is used (OPF1=0,OPF2=0).They can more precisely adjust the input reference voltage of V0 generator. The details please refer to the supply voltage for LCD driver.

- **Follower control**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	FON	Rab 2	Rab 1	Rab 0

Ø **Fon: switch follower circuit**

Fon can only be set when internal follower is used (OPF1=0,OPF2=0).

When Fon = "High", internal follower circuit is turn on.

When Fon = "Low", internal follower circuit is turn off.

Ø **Rab2,Rab1,Rab0 : V0 generator amplified ratio**

Rab2,Rab1,Rab0 can only be set when internal follower is used (OPF1=0,OPF2=0).They can adjust the amplified ratio of V0 generator. The details please refer to the supply voltage for LCD driver.

- Contrast set(low byte)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	C3	C2	C1	C0

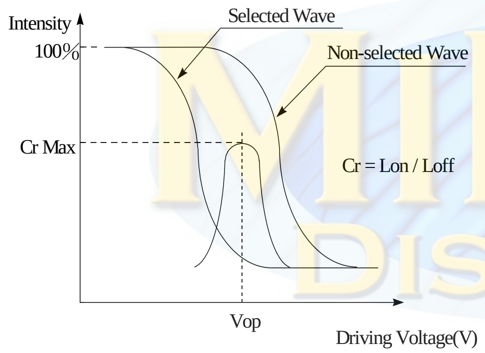
Ø **C3,C2,C1,C0:Contrast set(low byte)**

C5,C4,C3,C2,C1,C0 can only be set when internal follower is used (OPF1=0,OPF2=0).They can more precisely adjust the input reference voltage of V0 generator. The details please refer to the supply voltage for LCD driver.

8. Optical Characteristics

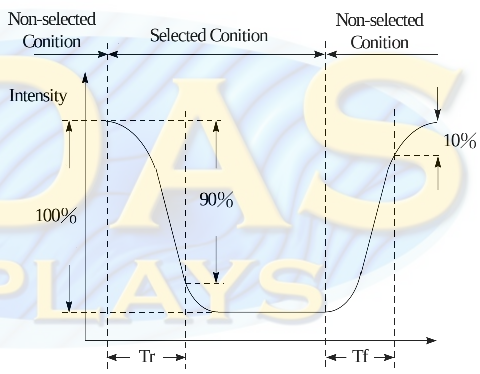
Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ	CR≧2	20	—	40	deg
	(H)φ	CR≧2	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	250	400	ms
	T fall	—	—	100	250	ms

Definition of Operation Voltage, Vop.



[positive type]

Definition of Response Time, Tr and Tf.



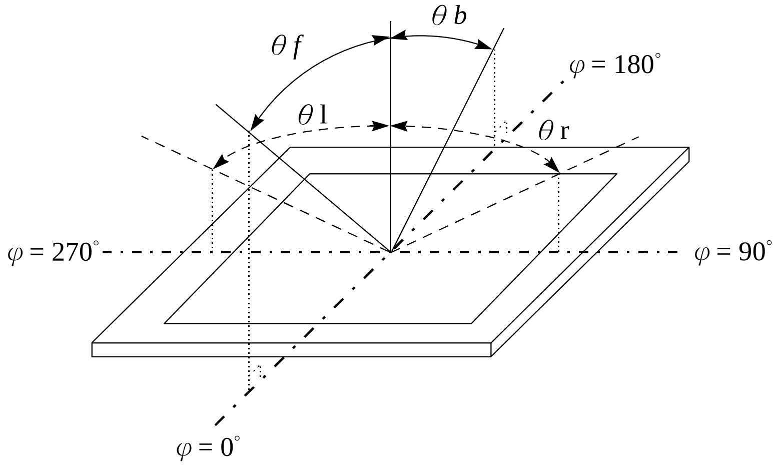
[positive type]

Conditions:

Operating Voltage : Vop　　　Viewing Angle(θ，φ) : 0°，0°

Frame Frequency: 64 HZ　　　Driving Waveform: 1/N duty, 1/a bias

Definition of viewing angle (CR≧2)



9. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃
Supply voltage for Logic	V_{DD}	-0.3	—	6.0	V
LCD Driver Voltage	V_{LCD}	7.0- V_{SS}		-0.3+ V_{SS}	V

10. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	3	3.3	5 (bon=1 max=3.5V)	V
Supply Voltage For LCD	V_{LCD}	Ta=-20℃	—	—	—	V
		Ta=25℃	—	4.5	—	V
		Ta=70℃	—	—	—	V
Input High Volt.	V_{IH}	—	0.7 V_{DD}	—	V_{DD}	V
Input Low Volt.	V_{IL}	—	—	—	0.2 V_{DD}	V
Output High Volt.	V_{OH}	—	0.8 V_{DD}	—	V_{DD}	V
Output Low Volt.	V_{OL}	—	—	—	0.2V_{DD}	V
Supply Current(No include LED Backlight)	I_{DD}	—	—	0.19		mA

11. Backlight Information

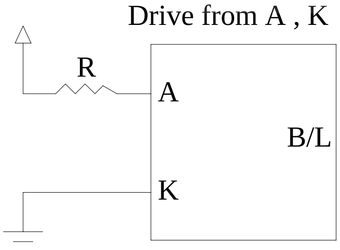
Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED	28.8	32	50	mA	V=3.5V
Supply Voltage	V	3.4	3.5	3.6	V	
Reverse Voltage	VR	—	—	5	V	—
Luminous Intensity (Without LCD)	IV	422.4	528.0	—	CD/M^2	ILED=32mA
LED Life Time	—	—	50000	—	Hr.	I_{LED}≦32mA
Color	White					

Note: The LED of B/L is drive by current only；driving voltage is only for reference To make driving current in safety area (waste current between minimum and maximum).

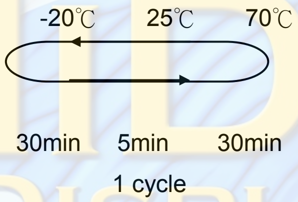
Note1 :50K hours is only an estimate for reference.

LED B\L Drive Method
Drive from A , K



12. Reliability

Content of Reliability Test (wide temperature, -20℃~70℃)

Environmental Test			
Test Item	**Content of Test**	**Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation 	-20℃/70℃ 10 cycles	-
Vibration test	Endurance test applying the vibration during transportation and using.	fixed amplitude: 15mm Vibration. Frequency: 10~55Hz. One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal temperature and humidity after remove from the test chamber.

Note3: Vibration test will be conducted to the product itself without putting it in a container.