3 nV/√Hz, Low Power Instrumentation Amplifier

Enhanced Product

AD8421-EP

FEATURES

Specified from −55°C to 125°C
- **0.9 µV/°C maximum input offset voltage drift**
- **5 ppm/°C maximum gain drift (G = 1)**

Low power
- **2.3 mA maximum supply current**

Low noise
- **3.2 nV/√Hz maximum input voltage noise at 1 kHz**
- **200 fA/√Hz current noise at 1 kHz**

Excellent ac specifications
- **2 MHz bandwidth (G = 100)**
- **0.6 µs settling time to 0.001% (G = 10)**
- **80 dB minimum CMRR at 20 kHz (G = 1)**

High precision dc performance
- **84 dB CMRR minimum (G = 1)**
- **2 nA maximum input bias current**

Inputs protected to 40 V from opposite supply

Gain set with a single resistor (G = 1 to 10,000)

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

PIN CONNECTION DIAGRAM

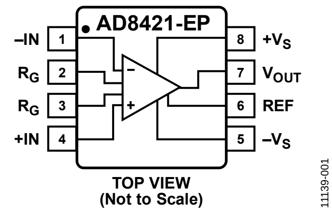

Figure 1.

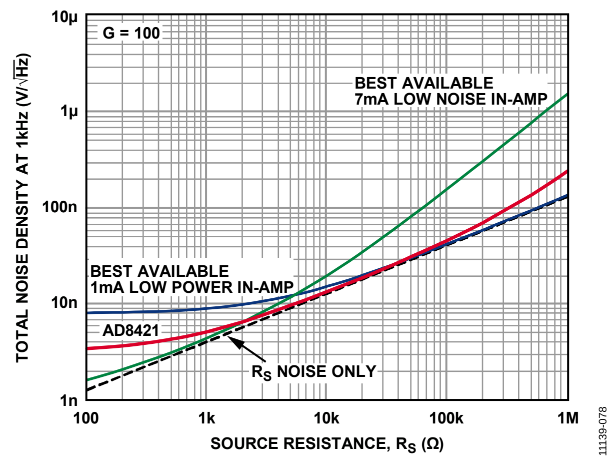

Figure 2. Noise Density vs. Source Resistance

GENERAL DESCRIPTION

The AD8421-EP is a low cost, low power, extremely low noise, ultralow bias current, high speed instrumentation amplifier that is ideally suited for a broad spectrum of signal conditioning and data acquisition applications. This product features extremely high CMRR, allowing it to extract low level signals in the presence of high frequency common-mode noise over a wide temperature range.

The 10 MHz bandwidth, 35 V/µs slew rate, and 0.6 µs settling time to 0.001% (G = 10) allow the AD8421-EP to amplify high speed signals and excel in applications that require high channel count, multiplexed systems. Even at higher gains, the current feedback architecture maintains high performance; for example, at G = 100, the bandwidth is 2 MHz and the settling time is 0.8 µs. The AD8421-EP has excellent distortion performance, making it suitable for use in demanding applications such as vibration analysis.

The AD8421-EP delivers 3 nV/√Hz input voltage noise and 200 fA/√Hz current noise with only 2 mA quiescent current, making it an ideal choice for measuring low level signals. For applications with high source impedance, the AD8421-EP employs innovative process technology and design techniques to provide noise performance that is limited only by the sensor.

The AD8421-EP uses unique protection methods to ensure robust inputs while still maintaining very low noise. This protection allows input voltages up to 40 V from the opposite supply rail without damage to the part.

A single resistor sets the gain from 1 to 10,000. The reference pin can be used to apply a precise offset to the output voltage.

The AD8421-EP is specified over the military temperature range of −55°C to +125°C. It is available in an 8-lead MSOP package.

Additional application and technical information can be found in the AD8421 data sheet.

Rev. 0 **Document Feedback**

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Technical Support **www.analog.com**

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REVISION HISTORY

5/13—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 2 kΩ, unless otherwise noted.

Table 1.

Parameter	Test Conditions/ Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to +10 V				
G = 1		84			dB
G = 10		104			dB
G = 100		124			dB
G = 1000		134			dB
Over Temperature, G = 1	T_A = −55°C to +125°C	80			dB
CMRR at 20 kHz	V_{CM} = −10 V to +10 V				
G = 1		80			dB
G = 10		90			dB
G = 100		100			dB
G = 1000		100			dB
NOISE					
Voltage Noise, 1 kHz[1]	V_{IN}+, V_{IN}− = 0 V				
Input Voltage Noise, e_{ni}			3	3.2	nV/√Hz
Output Voltage Noise, e_{no}				60	nV/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz				
G = 1			2		μV p-p
G = 10			0.5		μV p-p
G = 100 to 1000			0.07		μV p-p
Current Noise					
Spectral Density	f = 1 kHz		200		fA/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz		18		pA p-p
VOLTAGE OFFSET[2]					
Input Offset Voltage, V_{OSI}	V_S = ±5 V to ±15 V			70	μV
Over Temperature	T_A = −55°C to +125°C			160	μV
Average TC				0.9	μV/°C
Output Offset Voltage, V_{OSO}				600	μV
Over Temperature	T_A = −55°C to +125°C			1.5	mV
Average TC				9	μV/°C
Offset RTI vs. Supply (PSR)	V_S = ±2.5 V to ±18 V				
G = 1		90	120		dB
G = 10		110	120		dB
G = 100		124	130		dB
G = 1000		130	140		dB
INPUT CURRENT					
Input Bias Current			1	2	nA
Over Temperature	T_A = −55°C to +125°C			8	nA
Average TC			50		pA/°C
Input Offset Current			0.5	2	nA
Over Temperature	T_A = −55°C to +125°C			3	nA
Average TC			1		pA/°C

Parameter	Test Conditions/ Comments	Min	Typ	Max	Unit
DYNAMIC RESPONSE					
Small Signal Bandwidth	−3 dB				
G = 1			10		MHz
G = 10			10		MHz
G = 100			2		MHz
G = 1000			0.2		MHz
Settling Time 0.01%	10 V step				
G = 1			0.7		μs
G = 10			0.4		μs
G = 100			0.6		μs
G = 1000			5		μs
Settling Time 0.001%	10 V step				
G = 1			1		μs
G = 10			0.6		μs
G = 100			0.8		μs
G = 1000			6		μs
Slew Rate					
G = 1 to 100			35		V/μs
GAIN[3]	G = 1 + (9.9 kΩ/R_G)				
Gain Range		1		10,000	V/V
Gain Error	V_{OUT} = ±10 V				
G = 1				0.05	%
G = 10 to 1000				0.3	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V				
G = 1	R_L ≥ 2 kΩ			1	ppm
	R_L = 600 Ω		1	3	ppm
G = 10 to 1000	R_L ≥ 600 Ω		30	50	ppm
	V_{OUT} = −5 V to +5 V		5	10	ppm
Gain vs. Temperature[3]					
G = 1				5	ppm/°C
G > 1				−80	ppm/°C
INPUT					
Input Impedance					
Differential			30||3		GΩ||pF
Common Mode			30||3		GΩ||pF
Input Operating Voltage Range[4]	V_S = ±2.5 V to ±18 V	$-V_S + 2.3$		$+V_S - 1.8$	V
Over Temperature	T_A = −55°C	$-V_S + 2.5$		$+V_S - 2.0$	V
	T_A = +125°C	$-V_S + 2.1$		$+V_S - 1.8$	V
OUTPUT	R_L = 2 kΩ				
Output Swing	V_S = ±2.5 V to ±18 V	$-V_S + 1.2$		$+V_S - 1.7$	V
Over Temperature	T_A = −55°C to +125°C	$-V_S + 1.4$		$+V_S - 1.9$	V
Short-Circuit Current			65		mA
REFERENCE INPUT					
R_{IN}			20		kΩ
I_{IN}	$V_{IN}+$, $V_{IN}-$ = 0 V		20	24	μA
Voltage Range		$-V_S$		$+V_S$	V
Reference Gain to Output			1 ± 0.0001		V/V

Parameter	Test Conditions/ Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range	Dual supply	±2.5		±18	V
	Single supply	5		36	V
Quiescent Current			2	2.3	mA
Over Temperature	T_A = −55°C to +125°C			2.8	mA
TEMPERATURE RANGE					
For Specified Performance		−55		+125	°C

[1] Total voltage noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2 + e_{RG}^2)}$. See the AD8421 data sheet for more information.
[2] Total RTI $V_{OS} = (V_{OSI}) + (V_{OSO}/G)$.
[3] These specifications do not include the tolerance of the external gain setting resistor, R_G. For G > 1, add R_G errors to the specifications given in this table.
[4] Input voltage range of the AD8421-EP input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See the Typical Performance Characteristics section for more information.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at −IN or +IN[1]	$-V_S$ + 40 V
Minimum Voltage at −IN or +IN	$+V_S$ − 40 V
Maximum Voltage at REF[2]	$+V_S$ + 0.3 V
Minimum Voltage at REF	$-V_S$ − 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Maximum Junction Temperature	150°C
ESD	
Human Body Model	2 kV
Charged Device Model	1.25 kV
Machine Model	0.2 kV

[1] For voltages beyond these limits, use input protection resistors. See the AD8421 data sheet for more information.
[2] There are ESD protection diodes from the reference input to each supply, so REF cannot be driven beyond the supplies in the same way that +IN and −IN can. See the AD8421 data sheet for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

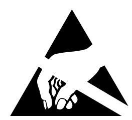
THERMAL RESISTANCE

θ_{JA} is specified for a device in free air using a 4-layer JEDEC printed circuit board (PCB).

Table 3.

Package	θ_{JA}	Unit
8-Lead MSOP	138.6	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

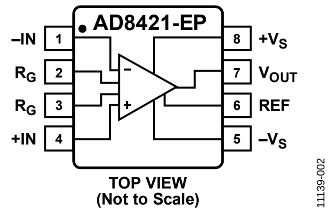


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input Terminal.
2, 3	R_G	Gain Setting Terminals. Place resistor across the R_G pins to set the gain. $G = 1 + (9.9\ k\Omega/R_G)$.
4	+IN	Positive Input Terminal.
5	$-V_S$	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level shift the output.
7	V_{OUT}	Output Terminal.
8	$+V_S$	Positive Power Supply Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15$ V, $V_{REF} = 0$ V, $R_L = 2$ kΩ, unless otherwise noted.

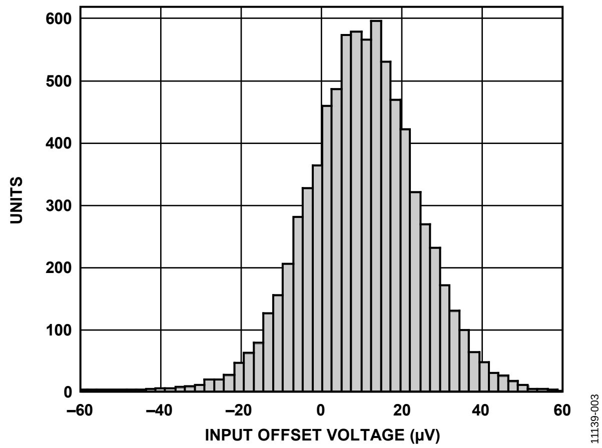


Figure 4. Typical Distribution of Input Offset Voltage

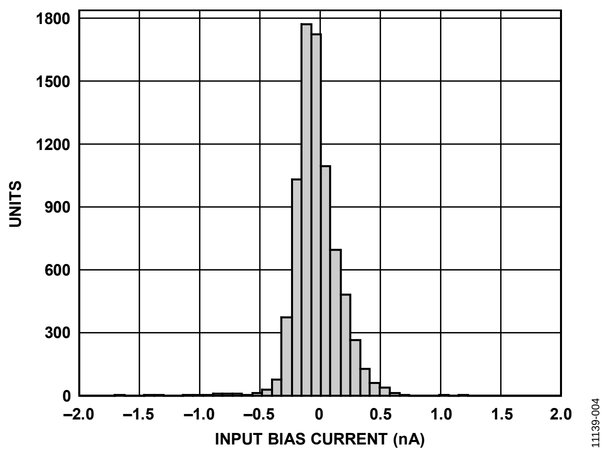


Figure 5. Typical Distribution of Input Bias Current

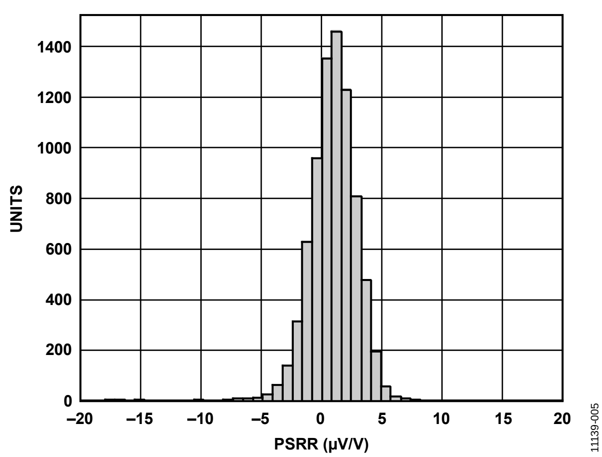


Figure 6. Typical Distribution of PSRR (G = 1)

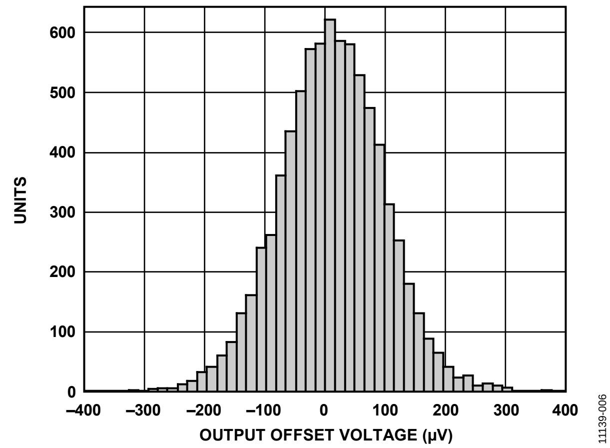


Figure 7. Typical Distribution of Output Offset Voltage

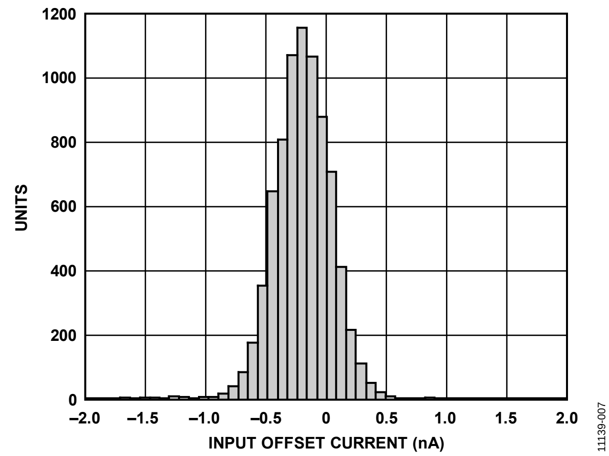


Figure 8. Typical Distribution of Input Offset Current

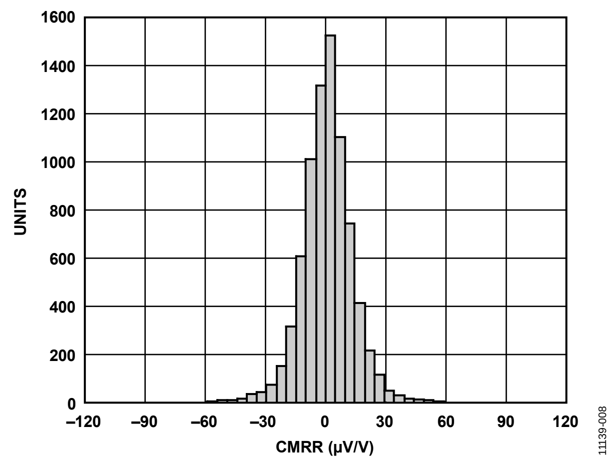


Figure 9. Typical Distribution of CMRR (G = 1)

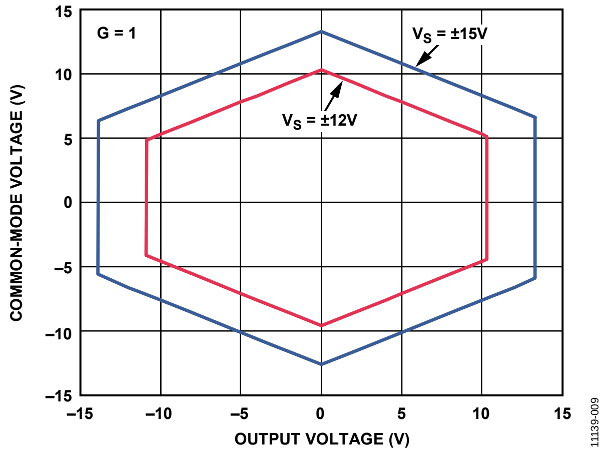


Figure 10. Input Common-Mode Voltage vs. Output Voltage; V_S = ±12 V and ±15 V (G = 1)

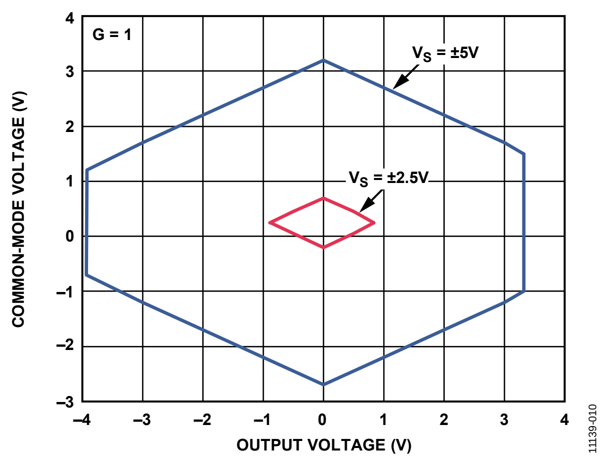


Figure 11. Input Common-Mode Voltage vs. Output Voltage; V_S = ±2.5 V and ±5 V (G = 1)

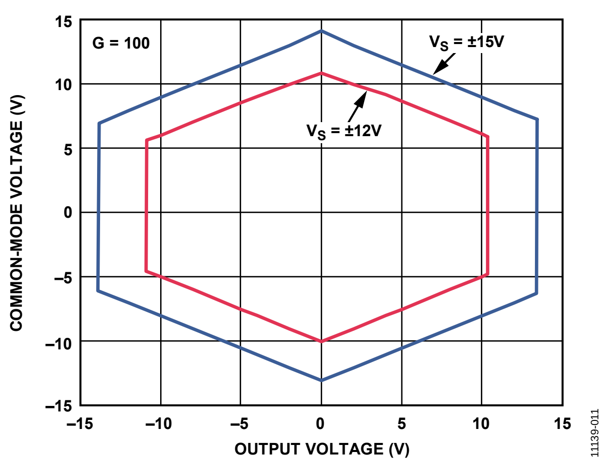


Figure 12. Input Common-Mode Voltage vs. Output Voltage; V_S = ±12 V and ±15 V (G = 100)

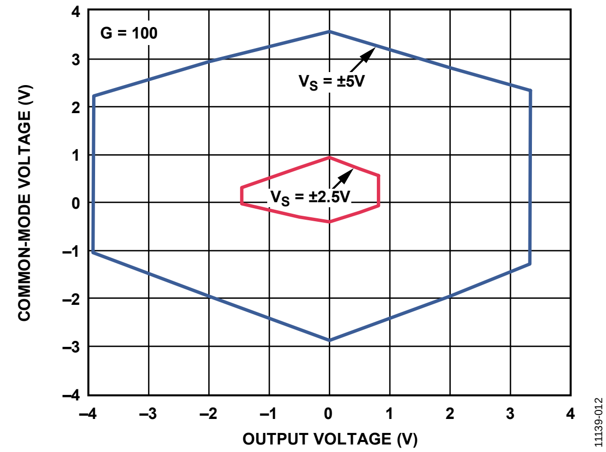


Figure 13. Input Common-Mode Voltage vs. Output Voltage; V_S = ±2.5 V and ±5 V (G = 100)

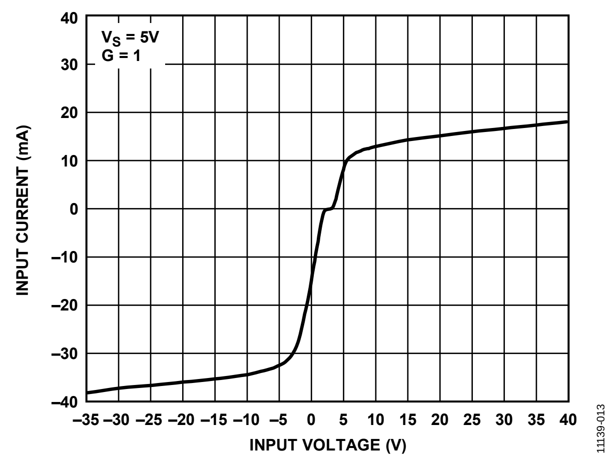


Figure 14. Input Overvoltage Performance; G = 1, $+V_S$ = 5 V, $-V_S$ = 0 V

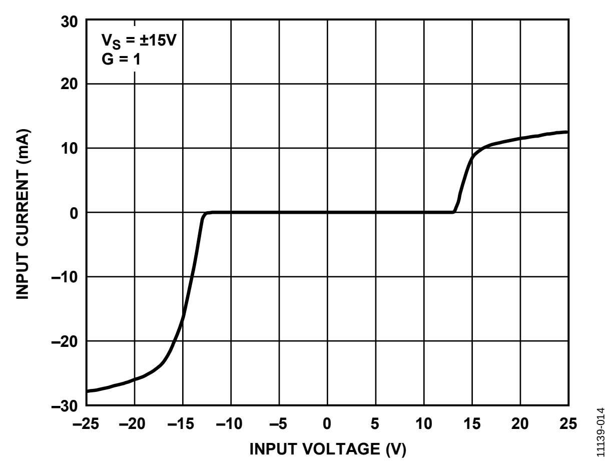


Figure 15. Input Overvoltage Performance; G = 1, V_S = ±15 V

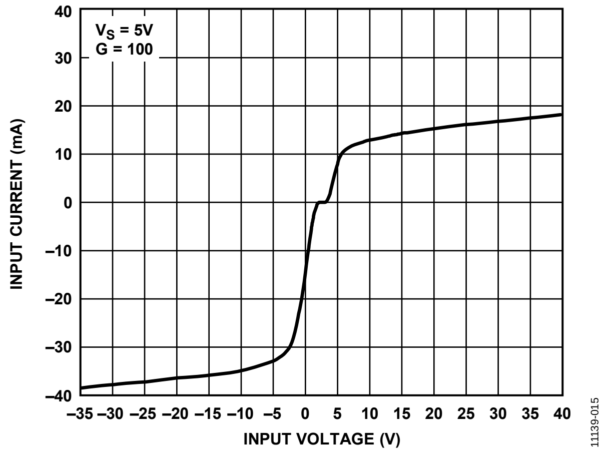


Figure 16. Input Overvoltage Performance; $+V_S = 5$ V, $-V_S = 0$ V, G = 100

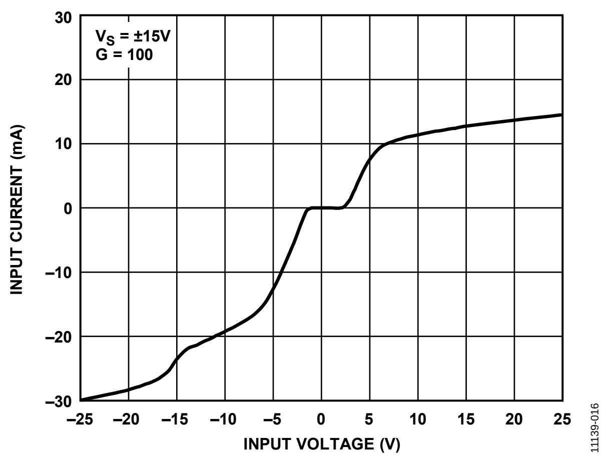


Figure 17. Input Overvoltage Performance; $V_S = \pm 15$ V, G = 100

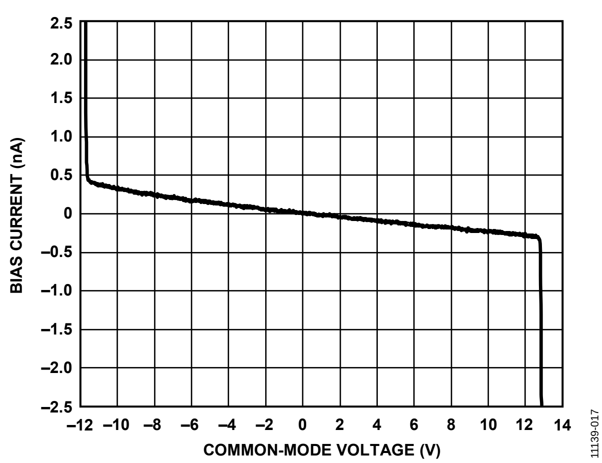


Figure 18. Input Bias Current vs. Common-Mode Voltage

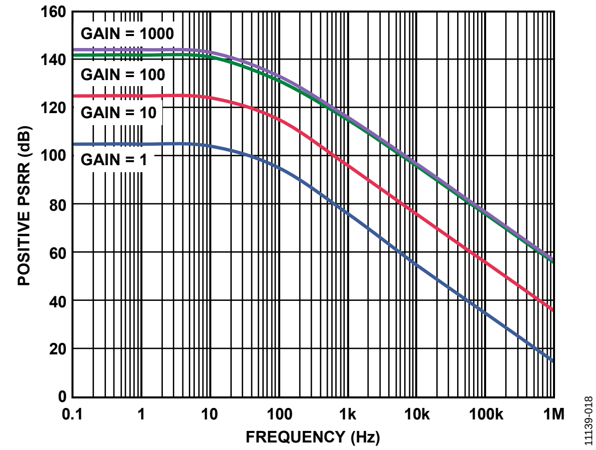


Figure 19. Positive PSRR vs. Frequency

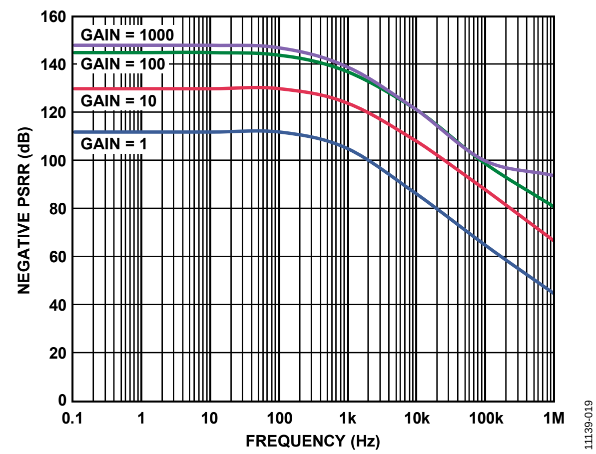


Figure 20. Negative PSRR vs. Frequency

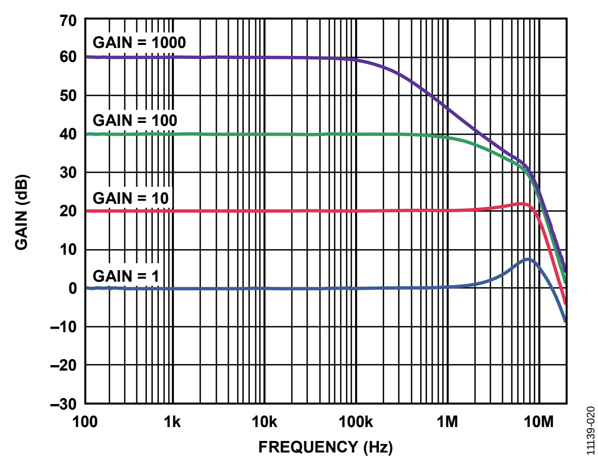


Figure 21. Gain vs. Frequency

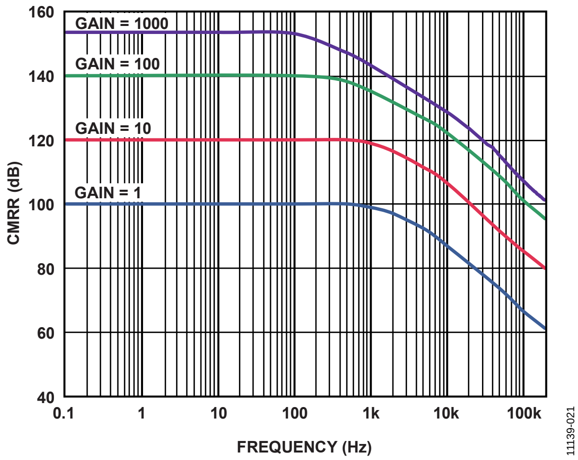


Figure 22. CMRR vs. Frequency

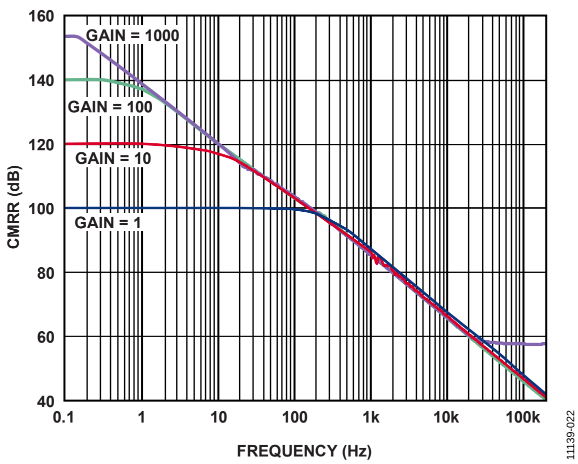


Figure 23. CMRR vs. Frequency, 1 kΩ Source Imbalance

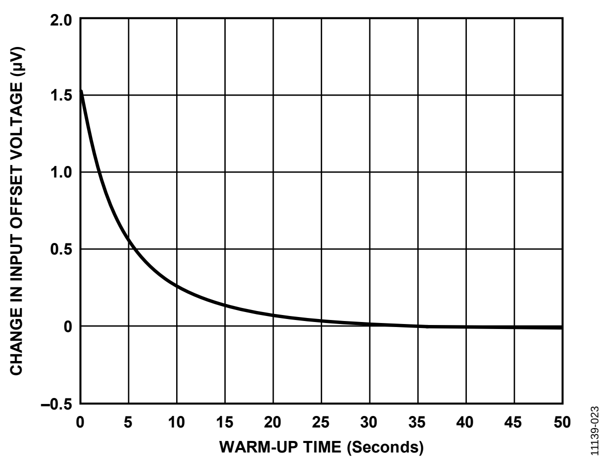


Figure 24. Change in Input Offset Voltage (V_{OSI}) vs. Warm-Up Time

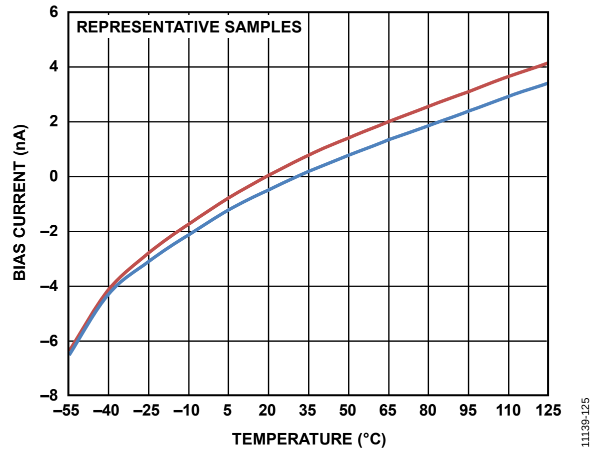


Figure 25. Input Bias Current vs. Temperature

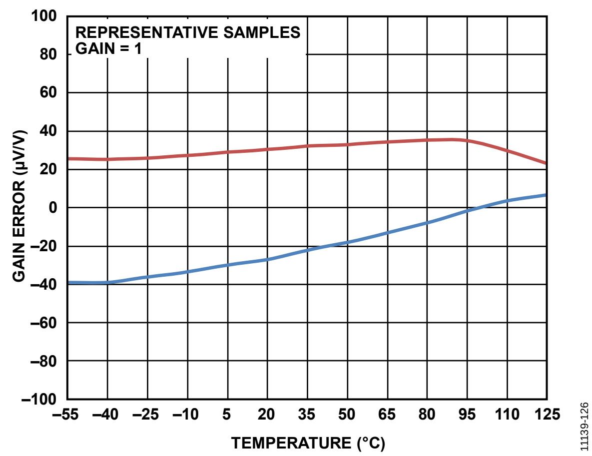


Figure 26. Gain vs. Temperature (G = 1)

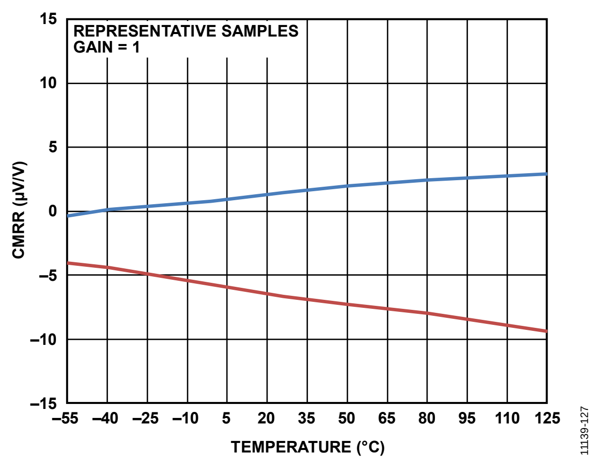


Figure 27. CMRR vs. Temperature (G = 1)

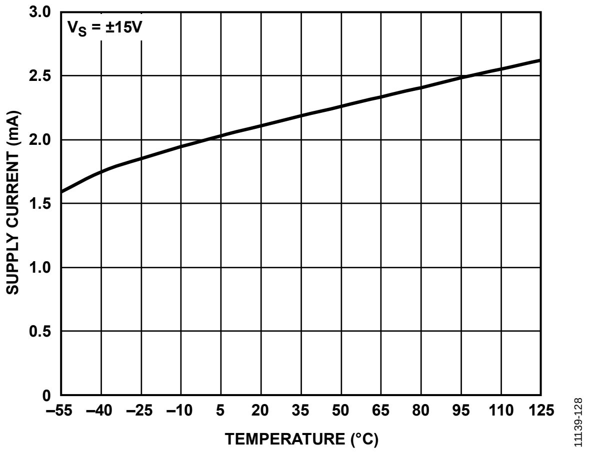


Figure 28. Supply Current vs. Temperature (G = 1)

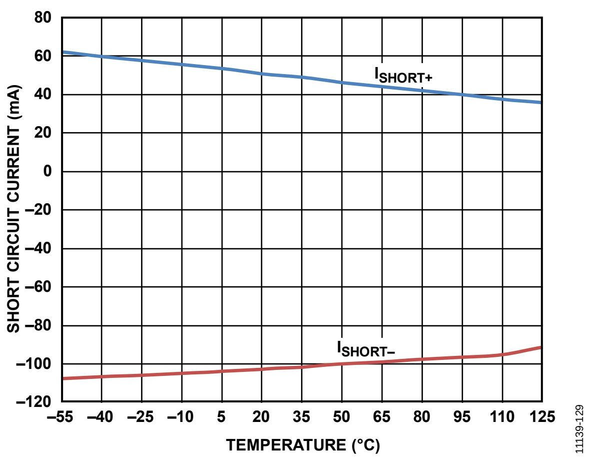


Figure 29. Short-Circuit Current vs. Temperature (G = 1)

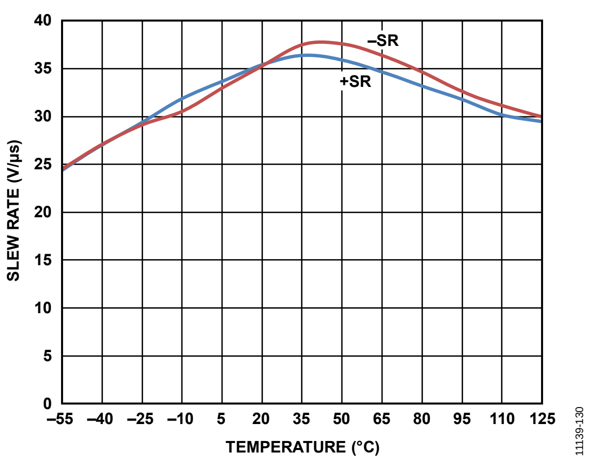


Figure 30. Slew Rate vs. Temperature, $V_S = \pm 15$ V (G = 1)

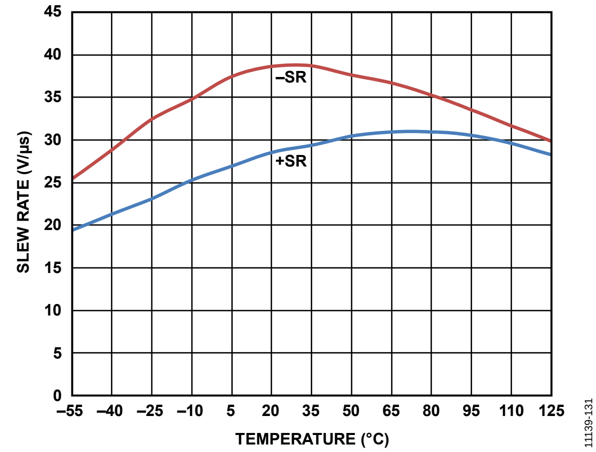


Figure 31. Slew Rate vs. Temperature, $V_S = \pm 5$ V (G = 1)

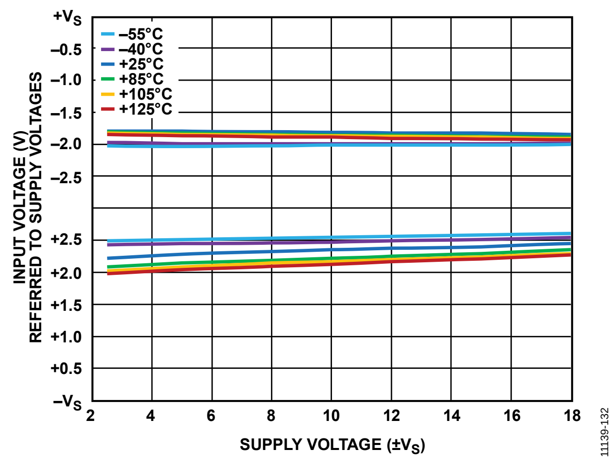


Figure 32. Input Voltage Limit vs. Supply Voltage

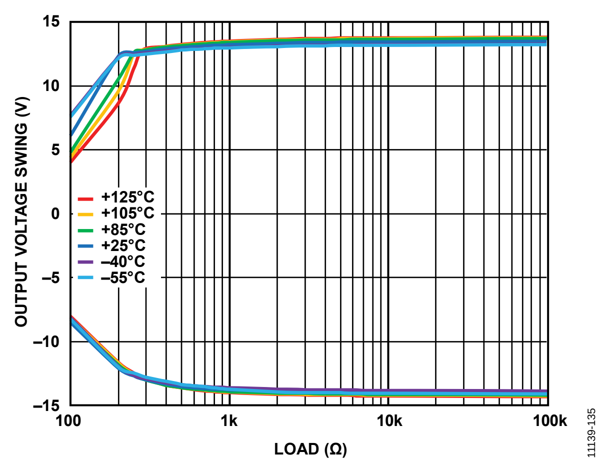


Figure 33. Output Voltage Swing vs. Load Resistance

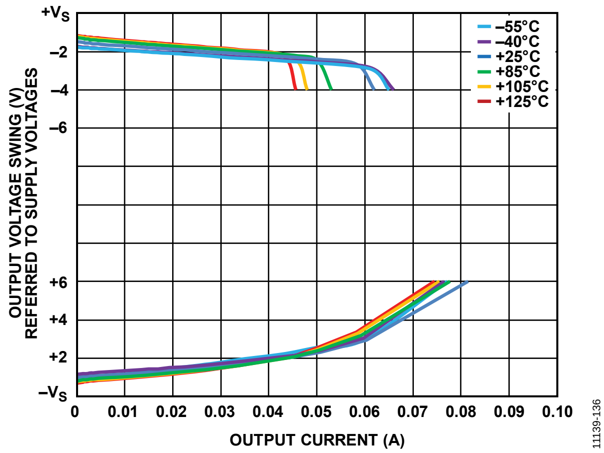


Figure 34. Output Voltage Swing vs. Output Current

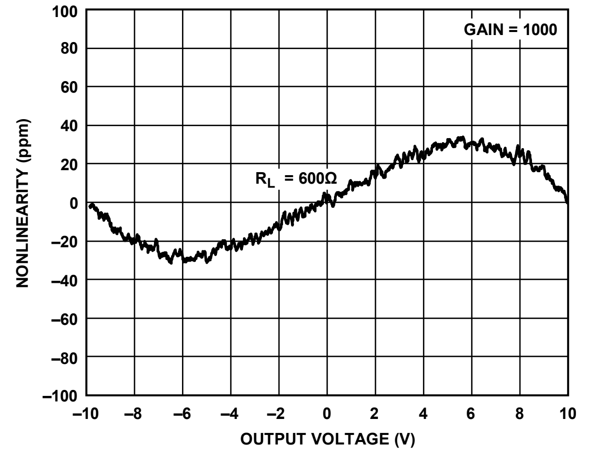


Figure 37. Gain Nonlinearity (G = 1000), R_L = 600 Ω, V_{OUT} = ±10 V

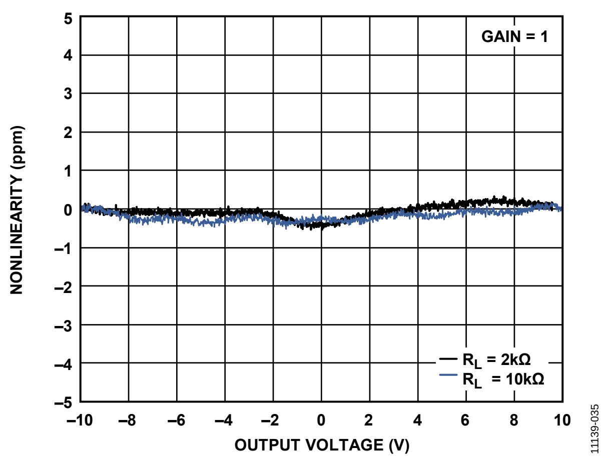


Figure 35. Gain Nonlinearity (G = 1), R_L = 10 kΩ, 2 kΩ

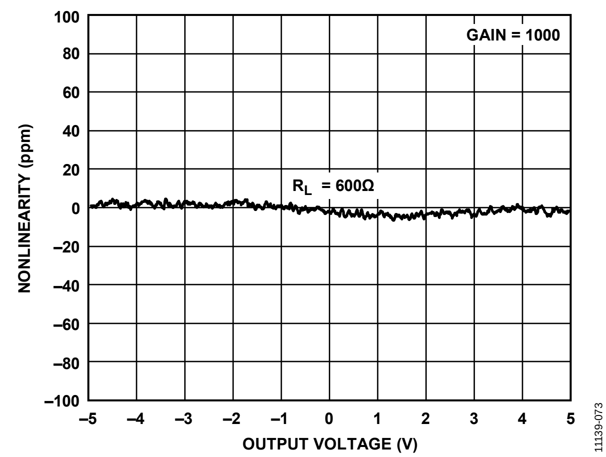


Figure 38. Gain Nonlinearity (G = 1000), R_L = 600 Ω, V_{OUT} = ±5 V

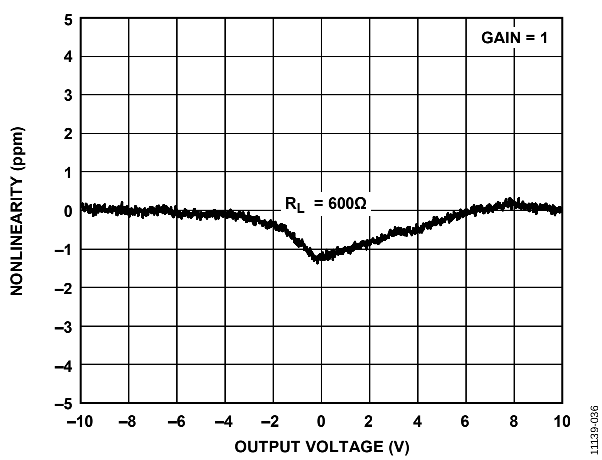


Figure 36. Gain Nonlinearity (G = 1), R_L = 600 Ω

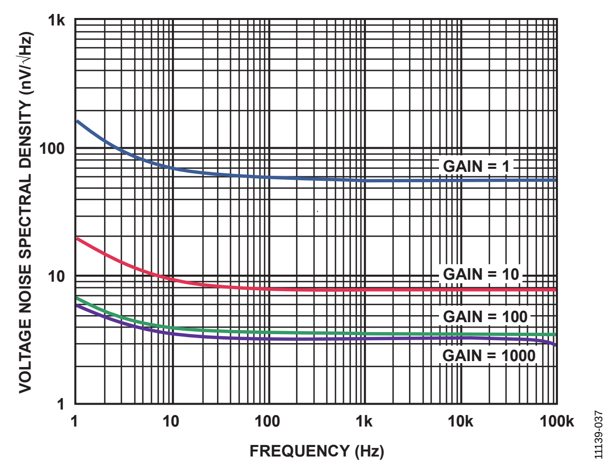


Figure 39. RTI Voltage Noise Spectral Density vs. Frequency

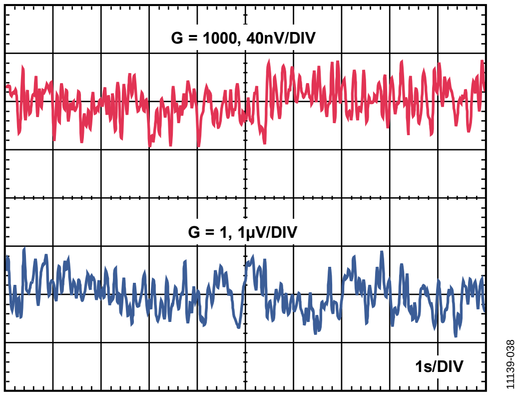


Figure 40. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1, G = 1000)

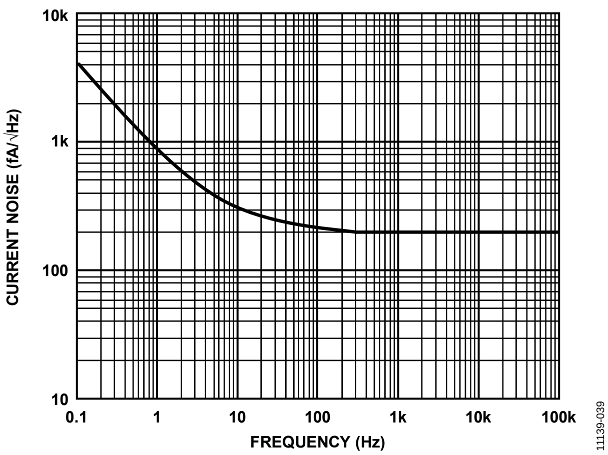


Figure 41. Current Noise Spectral Density vs. Frequency

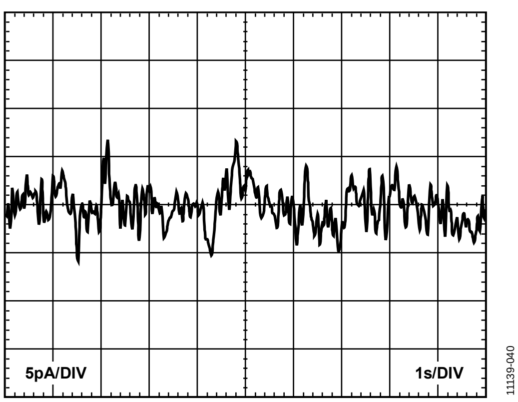


Figure 42. 0.1 Hz to 10 Hz Current Noise

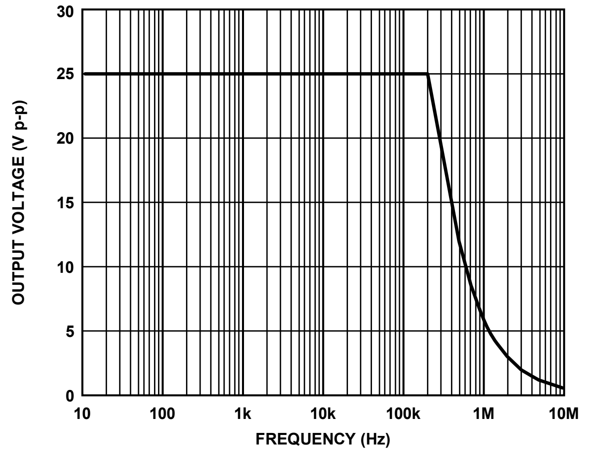


Figure 43. Large Signal Frequency Response

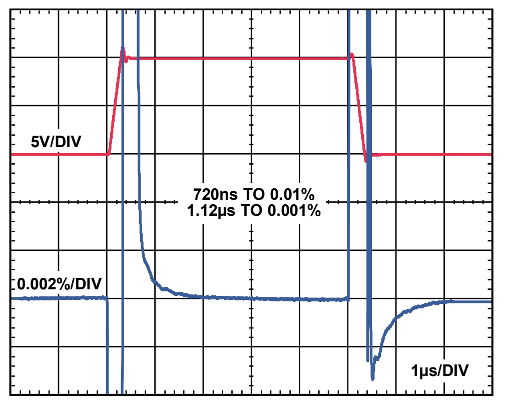


Figure 44. Large Signal Pulse Response and Settling Time (G = 1), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

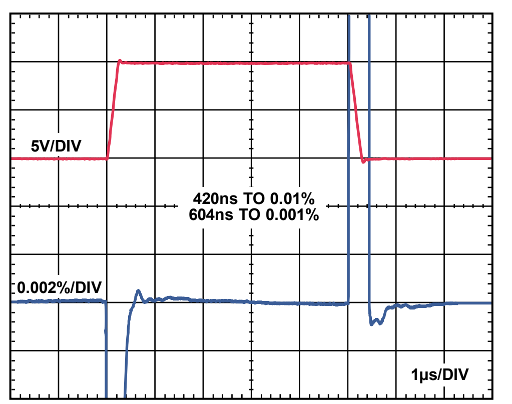


Figure 45. Large Signal Pulse Response and Settling Time (G = 10), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

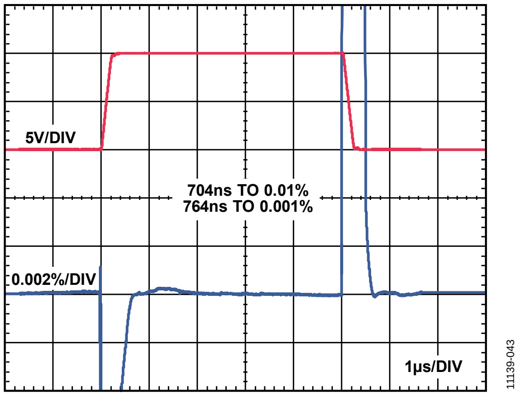


Figure 46. Large Signal Pulse Response and Settling Time (G = 100), 10 V Step, $V_S = \pm15$ V, $R_L = 2$ kΩ, $C_L = 100$ pF

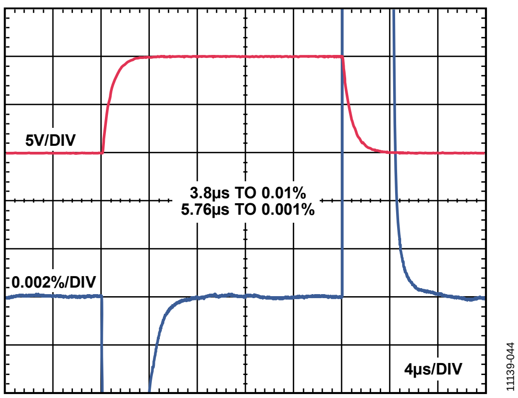


Figure 47. Large Signal Pulse Response and Settling Time (G = 1000), 10 V Step, $V_S = \pm15$ V, $R_L = 2$ kΩ, $C_L = 100$ pF

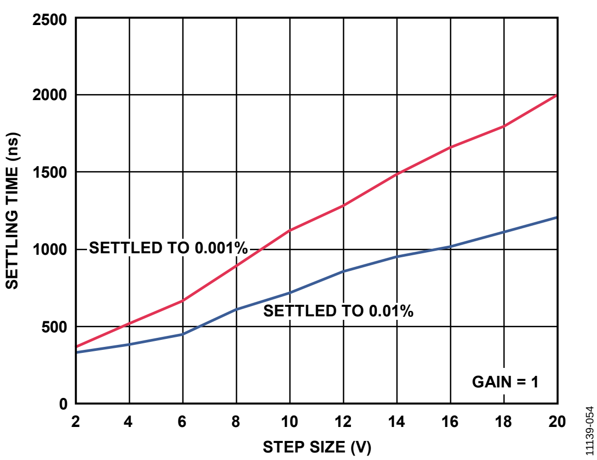


Figure 48. Settling Time vs. Step Size (G = 1), $R_L = 2$ kΩ, $C_L = 100$ pF

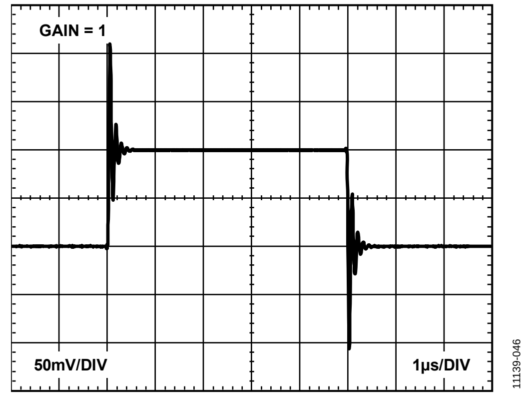


Figure 49. Small Signal Pulse Response (G = 1), $R_L = 600$ Ω, $C_L = 100$ pF

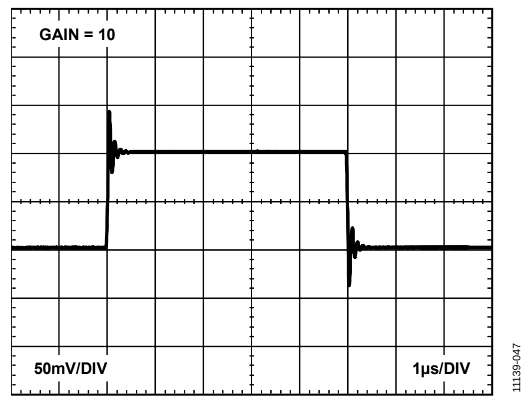


Figure 50. Small Signal Pulse Response (G = 10), $R_L = 600$ Ω, $C_L = 100$ pF

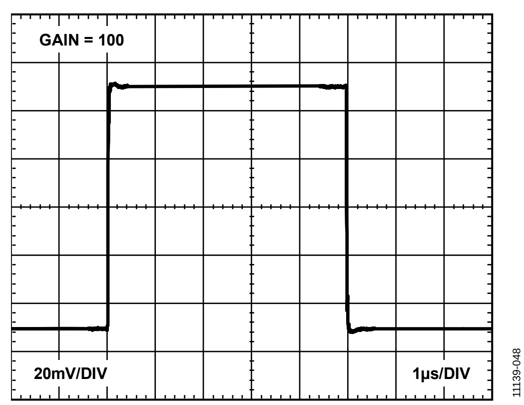


Figure 51. Small Signal Pulse Response (G = 100), RL = 600 Ω, CL = 100 pF

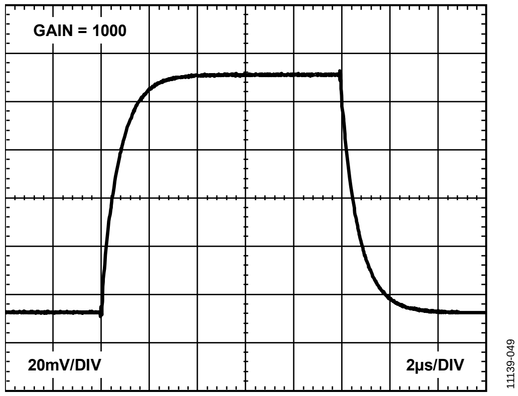


Figure 52. Small Signal Pulse Response (G = 1000), R_L = 600 Ω, C_L = 100 pF

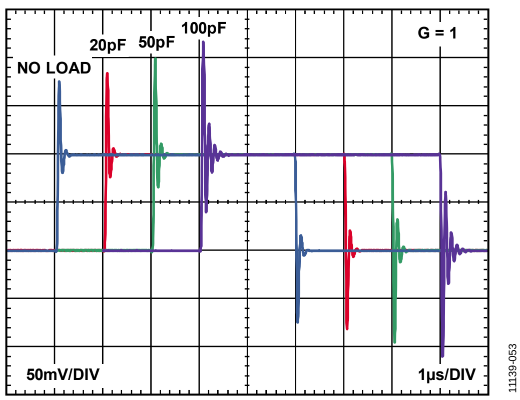


Figure 53. Small Signal Response with Various Capacitive Loads (G = 1), R_L = Infinity

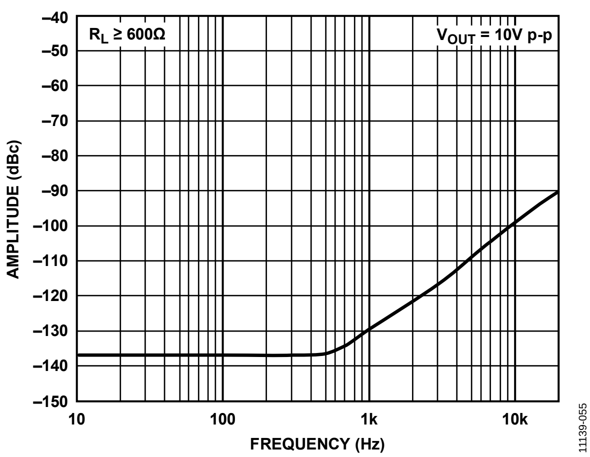


Figure 54. Second Harmonic Distortion vs. Frequency (G = 1)

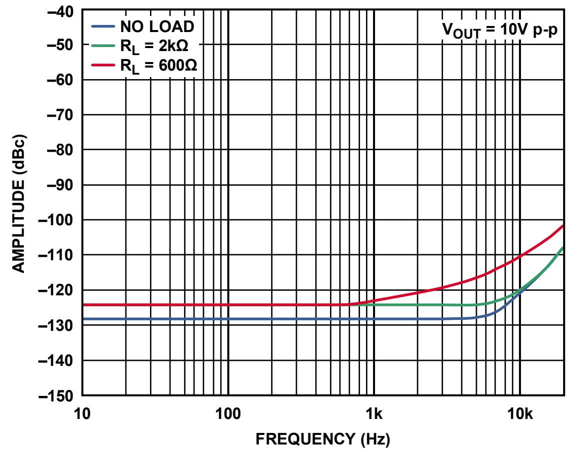


Figure 55. Third Harmonic Distortion vs. Frequency (G = 1)

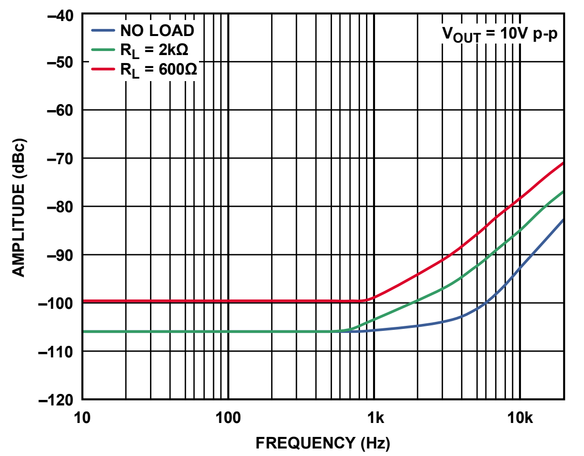


Figure 56. Second Harmonic Distortion vs. Frequency (G = 1000)

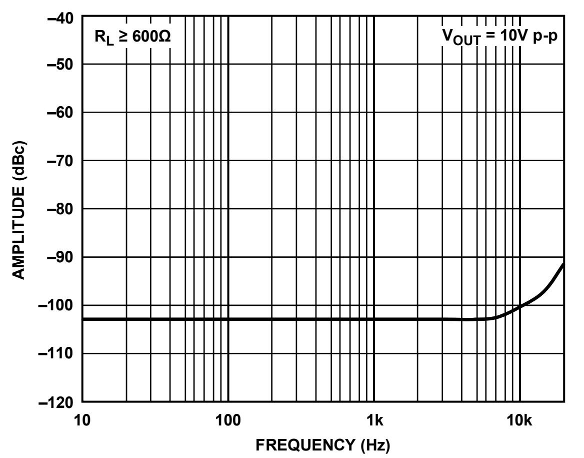


Figure 57. Third Harmonic Distortion vs. Frequency (G = 1000)

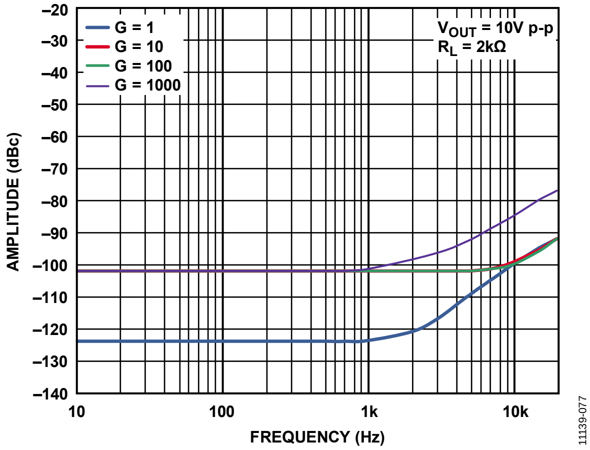


Figure 58. THD vs. Frequency

OUTLINE DIMENSIONS

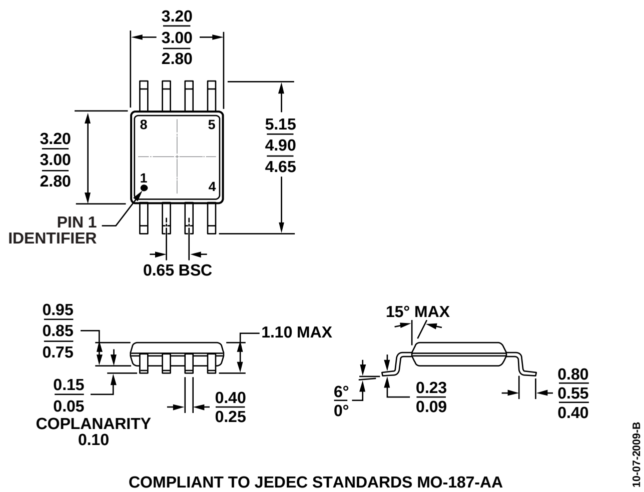


Figure 59. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8421TRMZ-EP	−55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y4T
AD8421TRMZ-EP-R7	−55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y4T

[1] Z = RoHS Compliant Part.

NOTES

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