MC33272A, MC33274A, NCV33272A, NCV33274A

Single Supply, High Slew Rate, Low Input Offset Voltage Operational Amplifiers

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip−R−Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual−doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

Features

- Input Offset Voltage Trimmed to 100 μV (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: 16 MΩ
- Low Noise: 18 nV/$\sqrt{Hz}$ @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: 10 V/μs
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ −14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or ±1.5 V to ±18 V
- ESD Diodes Provide Added Protection to the Inputs
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- Pb−Free Packages are Available
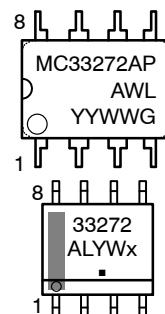
ON Semiconductor®

http://onsemi.com

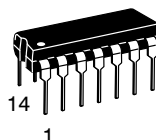### MARKING DIAGRAMS

DUAL

PDIP−8
P SUFFIX
CASE 626
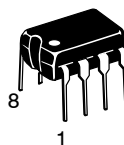
MC33272AP
AWL
YYWWG

SOIC−8
D SUFFIX
CASE 751

33272
ALYWx

x = A for MC33272AD/DR2
= N for NCV33272ADR2

QUAD

PDIP−14
P SUFFIX
CASE 646

MC33274AP
AWLYYWWG
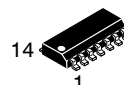
SOIC−14
D SUFFIX
CASE 751A

MC33274ADG
AWLYWW

NCV33274AG
AWLYWW
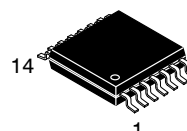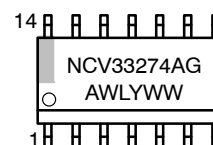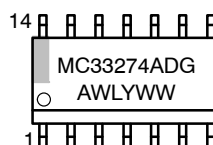
TSSOP−14
DTB SUFFIX
CASE 948G

MC33
274A
ALYW■

NCV3
3274
ALYW■
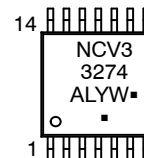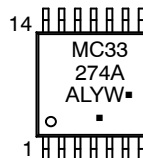
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
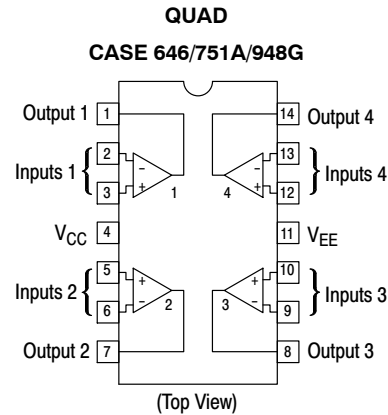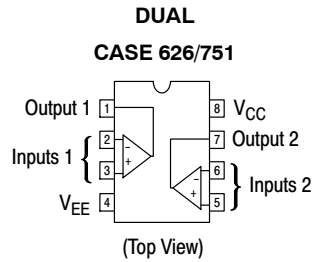WW, W = Work Week
G or ■ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

MC33272A, MC33274A, NCV33272A, NCV33274A

PIN CONNECTIONS

DUAL

CASE 626/751

Output 1 — 1
Inputs 1 { 2, 3
V_{EE} — 4
8 — V_{CC}
7 — Output 2
6, 5 } Inputs 2

(Top View)

QUAD

CASE 646/751A/948G

Output 1 — 1
Inputs 1 { 2, 3 } 1
V_{CC} — 4
Inputs 2 { 5, 6 } 2
Output 2 — 7

14 — Output 4
4 { 13, 12 } Inputs 4
11 — V_{EE}
3 { 10, 9 } Inputs 3
8 — Output 3

(Top View)

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range		V_{IDR}	Note 1	V
Input Voltage Range		V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)		t_{SC}	Indefinite	sec
Maximum Junction Temperature		T_J	+150	°C
Storage Temperature		T_{stg}	−60 to +150	°C
ESD Protection at Any Pin – Human Body Model – Machine Model		V_{esd}	 2000 200	V
Maximum Power Dissipation		P_D	Note 2	mW
Operating Temperature Range	MC33272A, MC33274A NCV33272A, NCV33274A	T_A	−40 to +85 −40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V) (V_{CC} = +15 V, V_{EE} = –15 V) T_A = +25°C T_A = –40° to +85°C T_A = –40° to +125°C (NCV33272A) T_A = –40° to +125°C (NCV33274A) (V_{CC} = 5.0 V, V_{EE} = 0) T_A = +25°C	3	$|V_{IO}|$	 – – – – –	 0.1 – – – –	 1.0 1.8 2.5 3.5 2.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = –40° to +125°C	3	$\Delta V_{IO}/\Delta T$	 –	 2.0	 –	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = T_{low} to T_{high}	4, 5	I_{IB}	 – –	 300 –	 650 800	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = T_{low} to T_{high}		$|I_{IO}|$	 – –	 3.0 –	 65 80	nA
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V) T_A = +25°C	6	V_{ICR}	V_{EE} to (V_{CC} –1.8)			V
Large Signal Voltage Gain (V_O = 0 V to 10 V, R_L = 2.0 kΩ) T_A = +25°C T_A = T_{low} to T_{high}	7	A_{VOL}	 90 86	 100 –	 – –	dB
Output Voltage Swing (V_{ID} = ±1.0 V) (V_{CC} = +15 V, V_{EE} = –15 V) R_L = 2.0 kΩ R_L = 2.0 kΩ R_L = 10 kΩ R_L = 10 kΩ (V_{CC} = 5.0 V, V_{EE} = 0 V) R_L = 2.0 kΩ R_L = 2.0 kΩ	8, 9, 12 10, 11	 V_O+ V_O- V_O+ V_O- V_{OL} V_{OH}	 13.4 – 13.4 – – 3.7	 13.9 –13.9 14 –14.7 – –	 – –13.5 – –14.1 0.2 5.0	V
Common Mode Rejection (V_{in} = +13.2 V to –15 V)	13	CMR	80	100	–	dB
Power Supply Rejection V_{CC}/V_{EE} = +15 V/ –15 V, +5.0 V/ –15 V, +15 V/ –5.0 V	14, 15	PSR	 80	 105	 –	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground) Source Sink	16	I_{SC}	 +25 –25	 +37 –37	 – –	mA
Power Supply Current Per Amplifier (V_O = 0 V) (V_{CC} = +15 V, V_{EE} = –15 V) T_A = +25°C T_A = T_{low} to T_{high} (V_{CC} = 5.0 V, V_{EE} = 0 V) T_A = +25°C	17	I_{CC}	 – – –	 2.15 – –	 2.75 3.0 2.75	mA

3. MC33272A, MC33274A T_{low} = –40°C T_{high} = +85°C
   NCV33272A, NCV33274A T_{low} = –40°C T_{high} = +125°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	18, 33	SR	8.0	10	–	V/μs
Gain Bandwidth Product (f = 100 kHz)	19	GBW	17	24	–	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	20, 21, 22	A_{VO}	–	65	–	dB
Unity Gain Bandwidth (Open Loop)		BW	–	5.5	–	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 24, 26	A_m	–	12	–	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 25, 26	ϕ_m	–	55	–	Deg
Channel Separation (f = 20 Hz to 20 kHz)	27	CS	–	−120	–	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_P	–	160	–	kHz
Total Harmonic Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	28	THD	–	0.003	–	%
Open Loop Output Impedance (V_O = 0 V, f = 6.0 MHz)	29	$|Z_O|$	–	35	–	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	–	16	–	MΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	–	3.0	–	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	30	e_n	–	18	–	nV/$\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	31	i_n	–	0.5	–	pA/$\sqrt{Hz}$
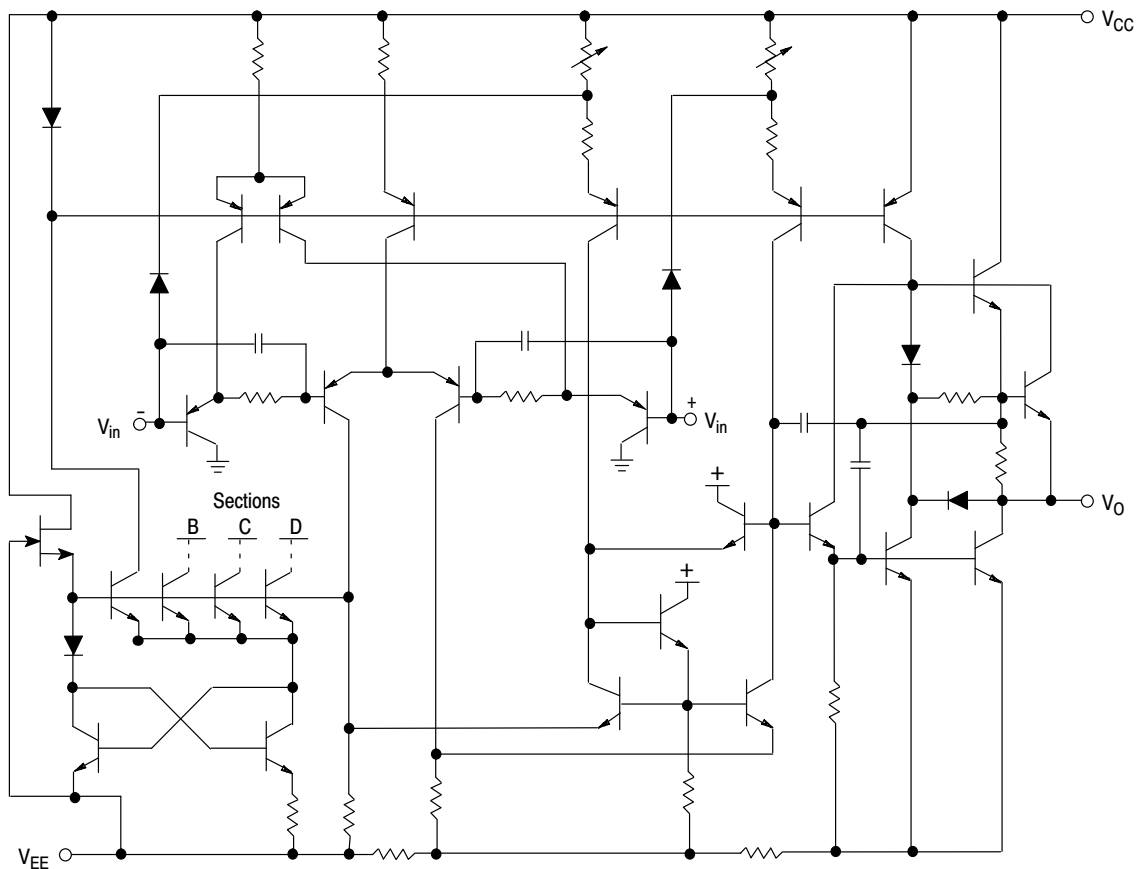
Figure 1. Equivalent Circuit Schematic
(Each Amplifier)
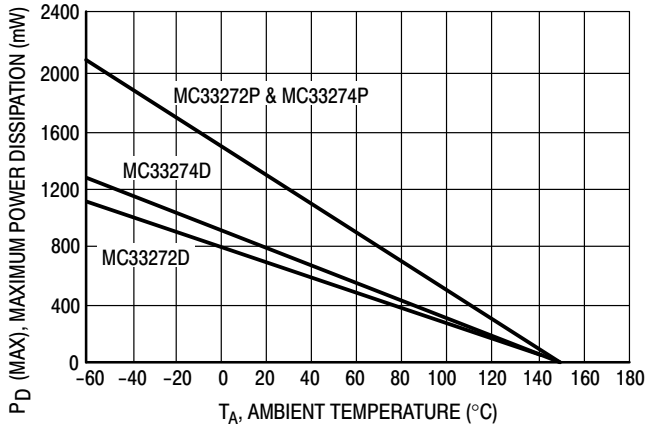
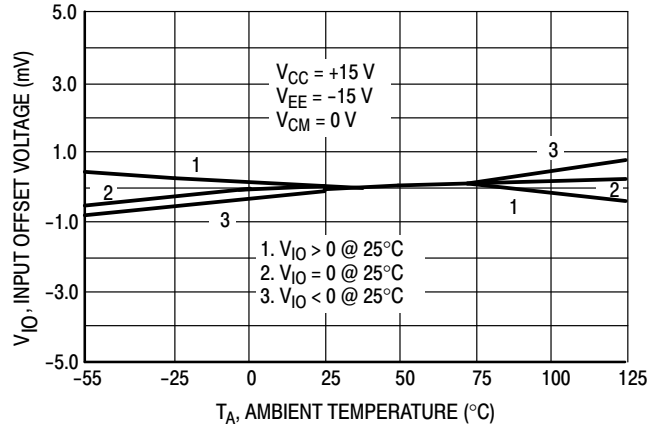**Figure 2. Maximum Power Dissipation versus Temperature**

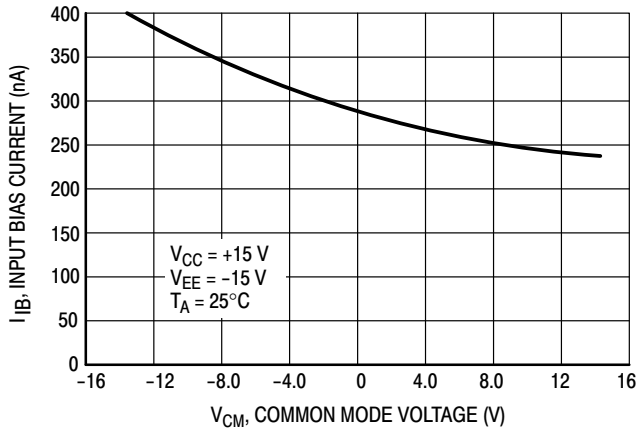**Figure 3. Input Offset Voltage versus Temperature for Typical Units**

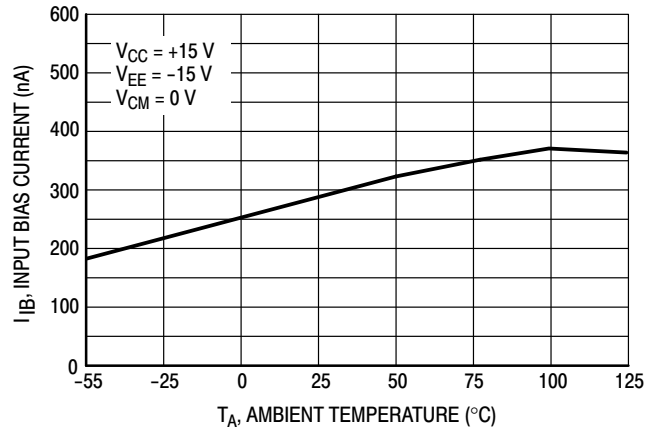**Figure 4. Input Bias Current versus Common Mode Voltage**
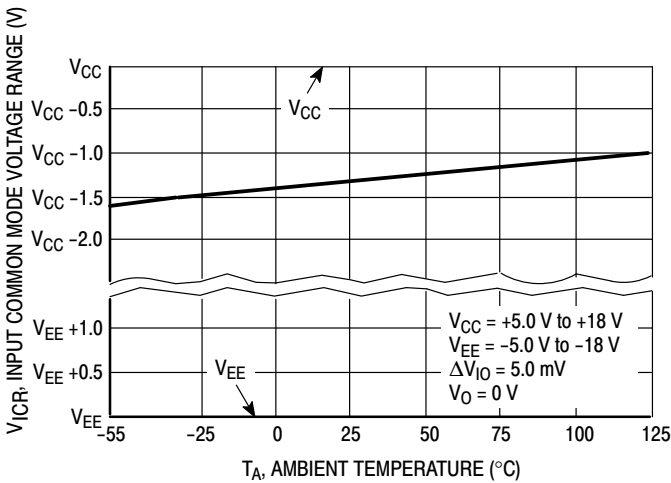
Figure 5. Input Bias Current versus Temperature

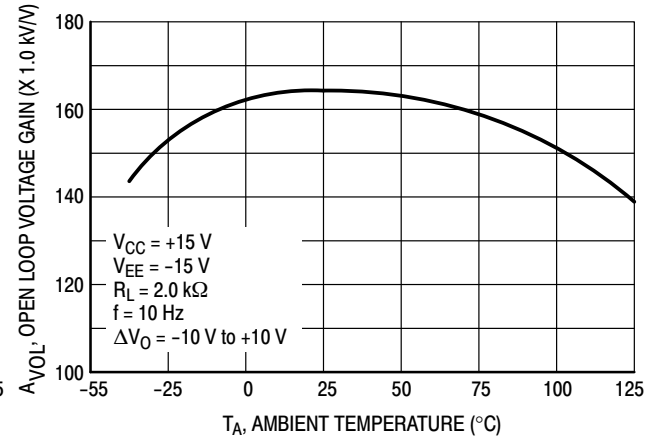**Figure 6. Input Common Mode Voltage Range versus Temperature**

Figure 7. Open Loop Voltage Gain versus Temperature
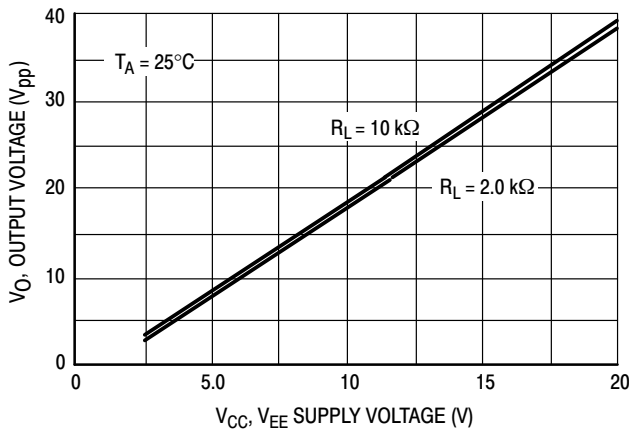
Figure 8. Split Supply Output Voltage Swing versus Supply Voltage
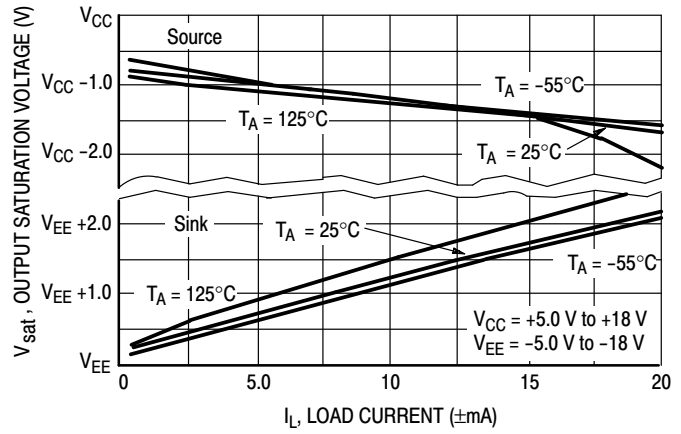
Figure 9. Split Supply Output Saturation Voltage versus Load Current
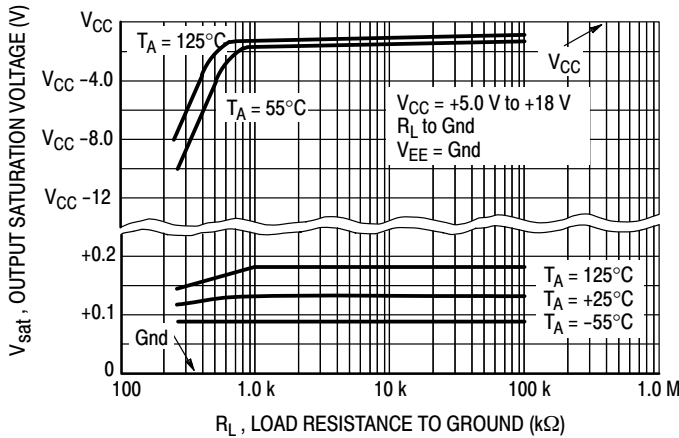
Figure 10. Single Supply Output Saturation Voltage versus Load Resistance to Ground
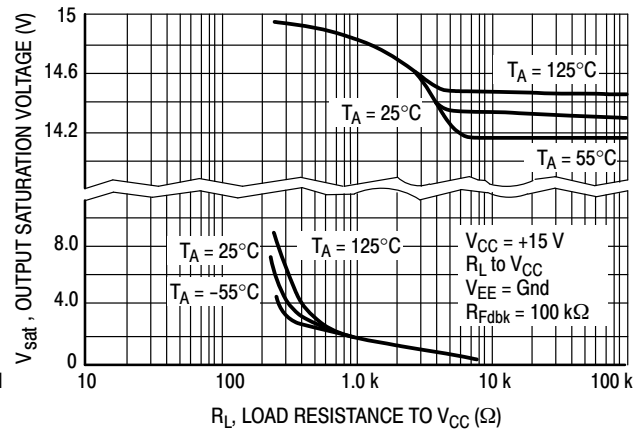
Figure 11. Single Supply Output Saturation Voltage versus Load Resistance to V_{CC}
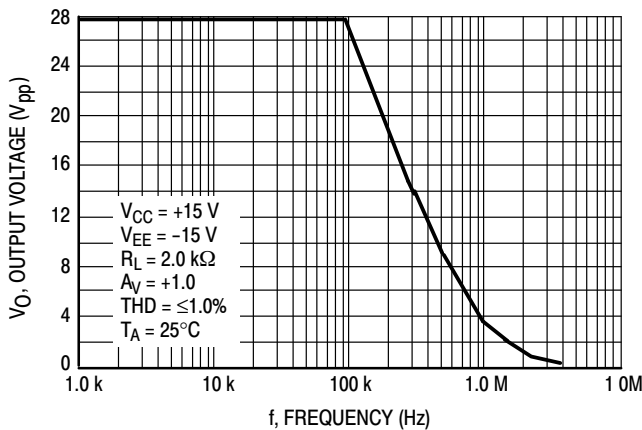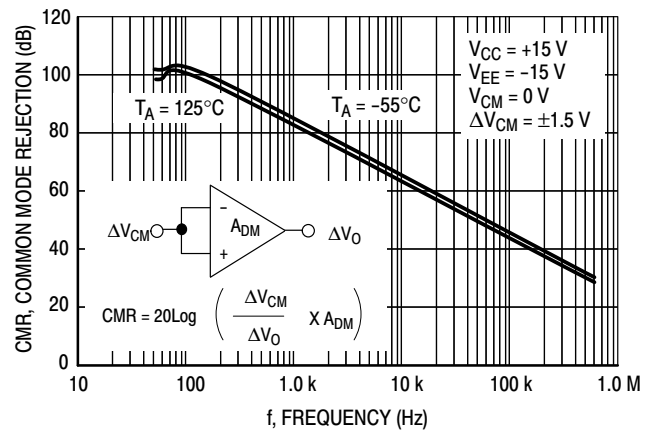
Figure 12. Output Voltage versus Frequency
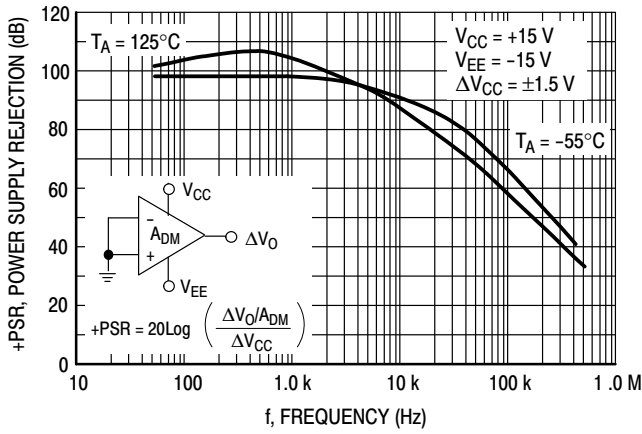
Figure 13. Common Mode Rejection versus Frequency

Figure 14. Positive Power Supply Rejection versus Frequency
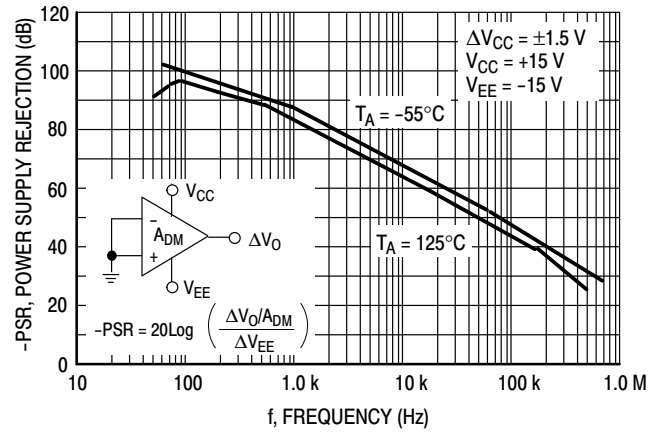

Figure 15. Negative Power Supply Rejection versus Frequency
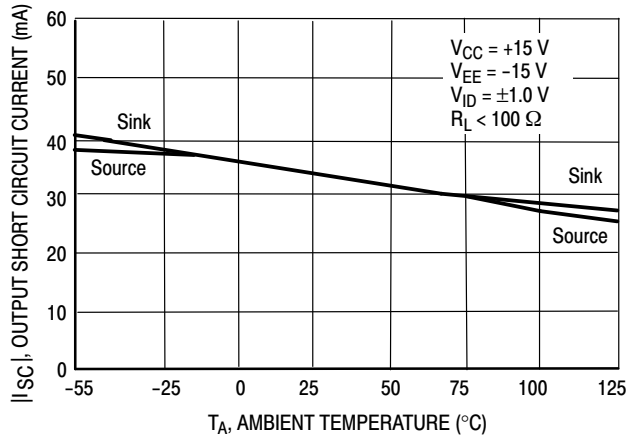

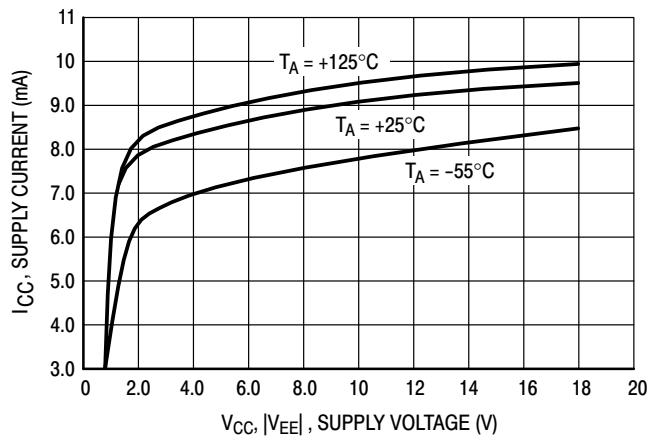**Figure 16. Output Short Circuit Current versus Temperature**

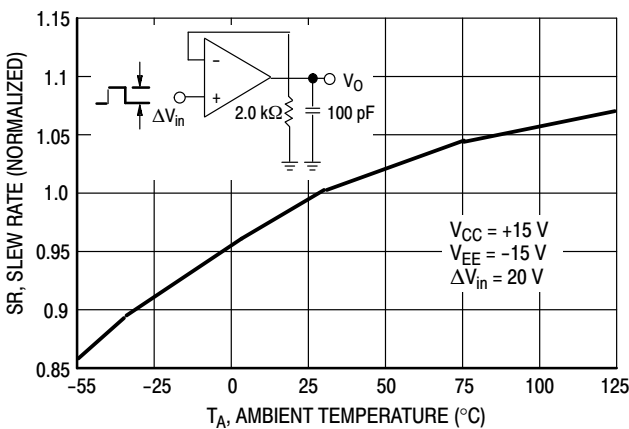**Figure 17. Supply Current versus Supply Voltage**

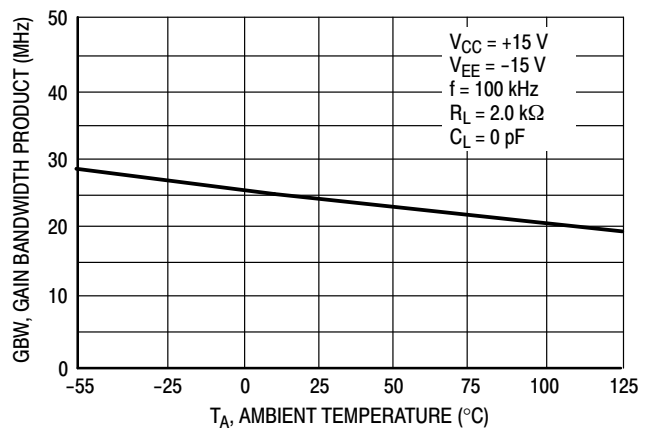**Figure 18. Normalized Slew Rate versus Temperature**

Figure 19. Gain Bandwidth Product versus Temperature
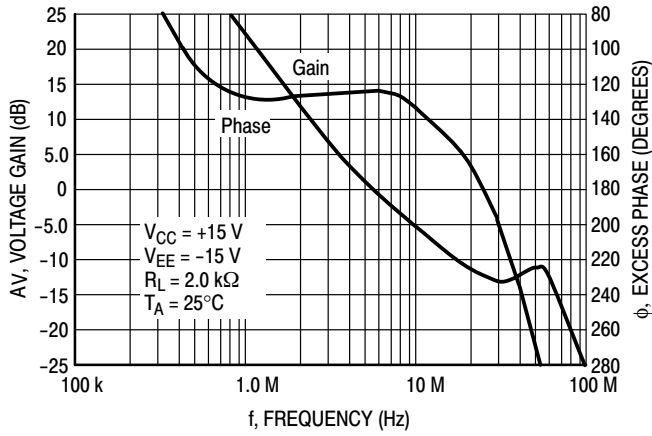
**Figure 20. Voltage Gain and Phase
versus Frequency**

V_{CC} = +15 V
V_{EE} = −15 V
R_L = 2.0 kΩ
T_A = 25°C
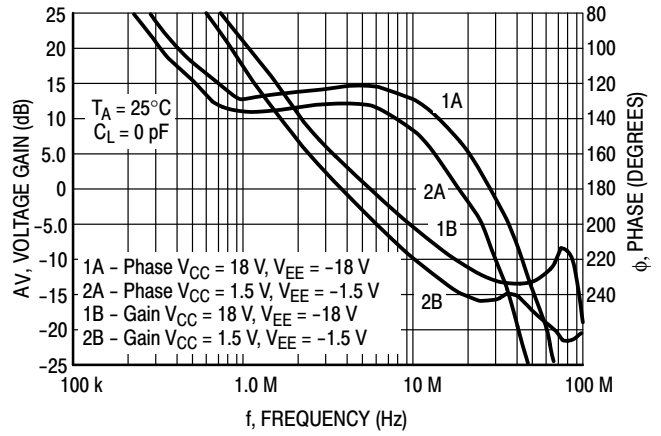
**Figure 21. Gain and Phase
versus Frequency**

T_A = 25°C
C_L = 0 pF

1A – Phase V_{CC} = 18 V, V_{EE} = −18 V
2A – Phase V_{CC} = 1.5 V, V_{EE} = −1.5 V
1B – Gain V_{CC} = 18 V, V_{EE} = −18 V
2B – Gain V_{CC} = 1.5 V, V_{EE} = −1.5 V
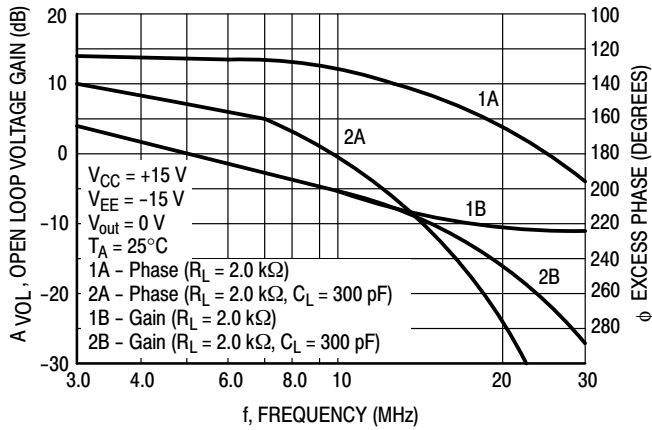
**Figure 22. Open Loop Voltage Gain and
Phase versus Frequency**

V_{CC} = +15 V
V_{EE} = −15 V
V_{out} = 0 V
T_A = 25°C
1A – Phase (R_L = 2.0 kΩ)
2A – Phase (R_L = 2.0 kΩ, C_L = 300 pF)
1B – Gain (R_L = 2.0 kΩ)
2B – Gain (R_L = 2.0 kΩ, C_L = 300 pF)
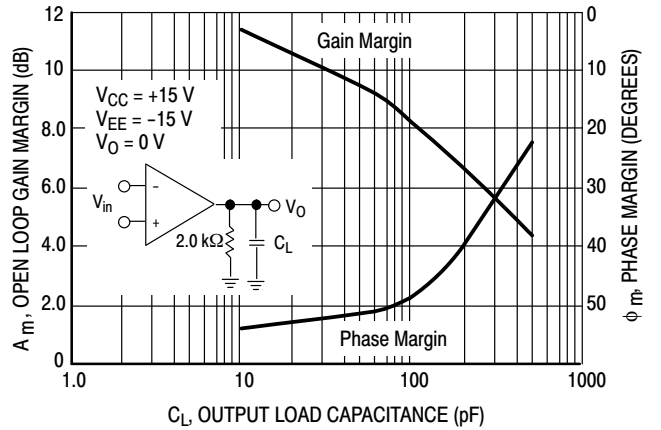
**Figure 23. Open Loop Gain Margin and Phase
Margin versus Output Load Capacitance**

V_{CC} = +15 V
V_{EE} = −15 V
V_O = 0 V

Gain Margin

Phase Margin

V_{in} — + V_O
2.0 kΩ C_L
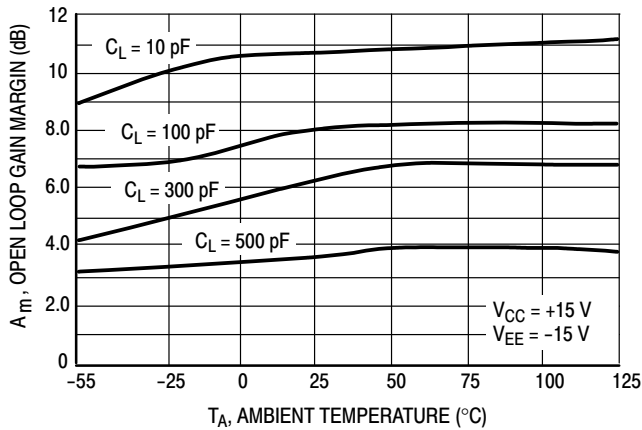
**Figure 24. Open Loop Gain Margin
versus Temperature**

C_L = 10 pF
C_L = 100 pF
C_L = 300 pF
C_L = 500 pF
V_{CC} = +15 V
V_{EE} = −15 V
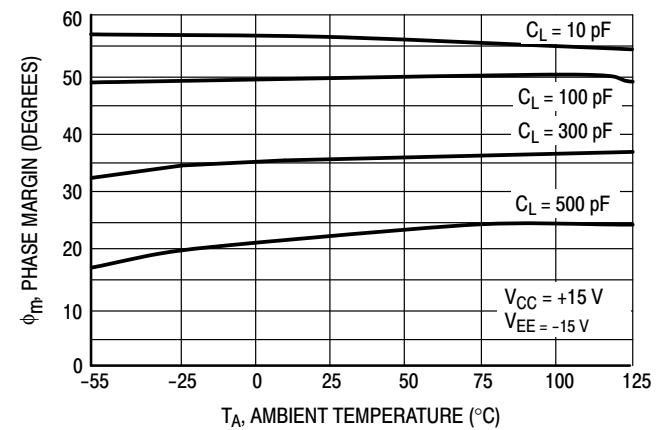
Figure 25. Phase Margin versus Temperature

C_L = 10 pF
C_L = 100 pF
C_L = 300 pF
C_L = 500 pF
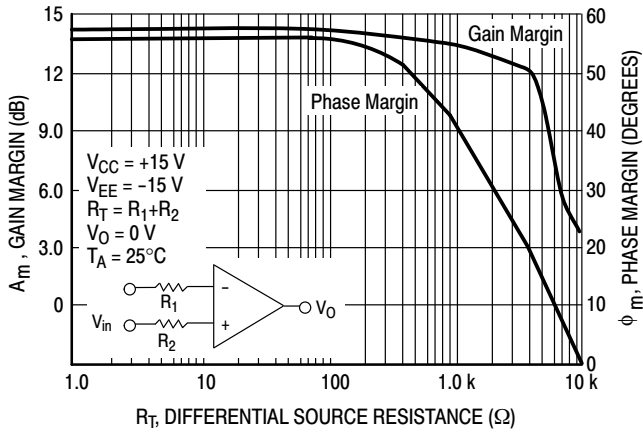V_{CC} = +15 V
V_{EE} = −15 V

**Figure 26. Phase Margin and Gain Margin
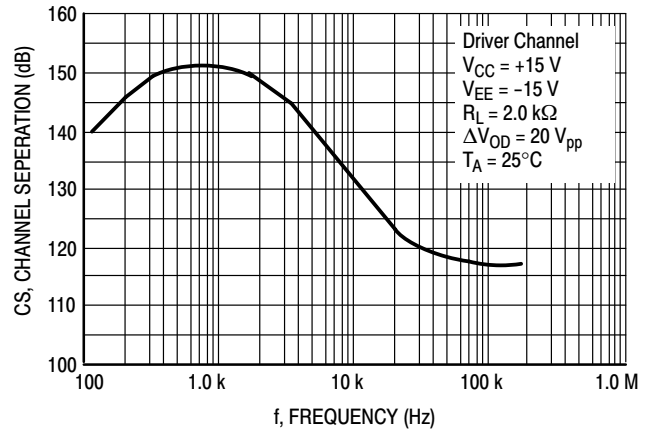versus Differential Source Resistance**
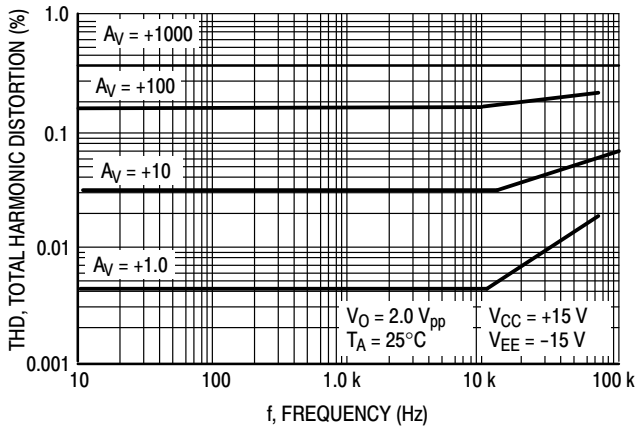
**Figure 27. Channel Separation
versus Frequency**

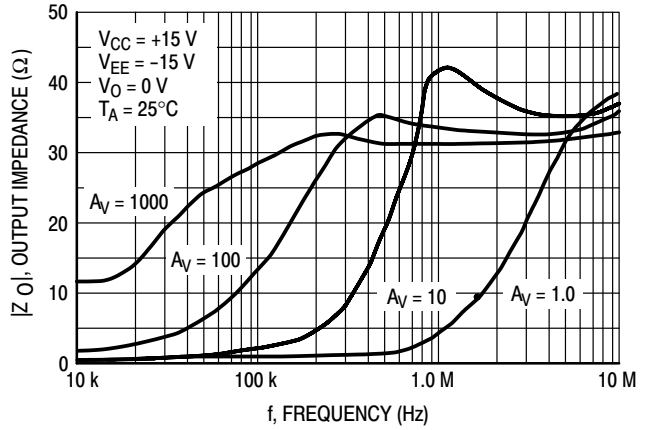**Figure 28. Total Harmonic Distortion
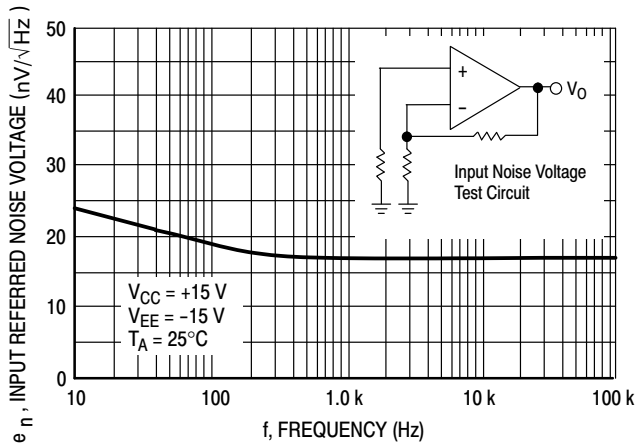versus Frequency**

Figure 29. Output Impedance versus Frequency

**Figure 30. Input Referred Noise Voltage
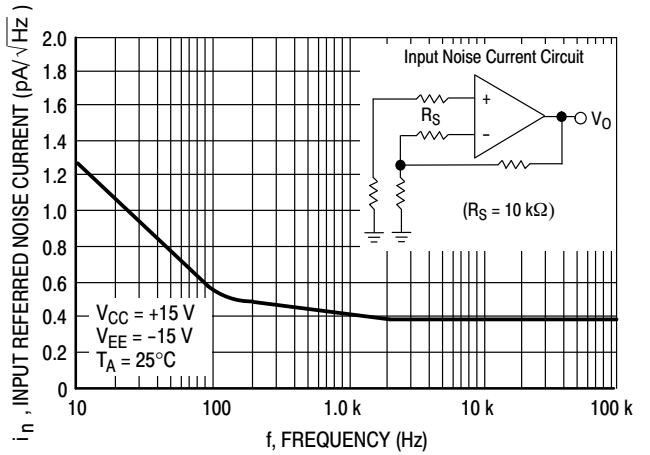versus Frequency**

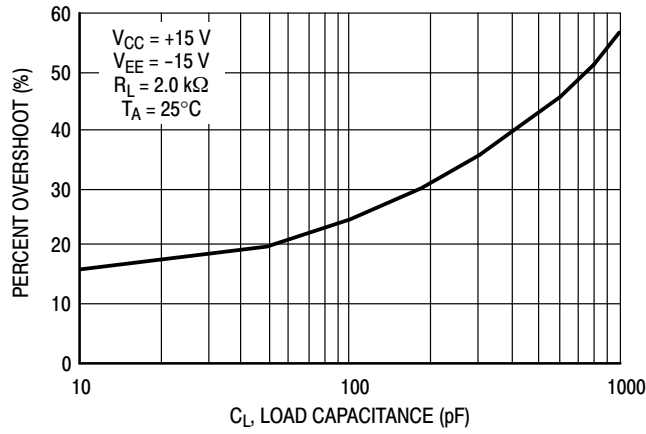**Figure 31. Input Referred Noise Current
versus Frequency**

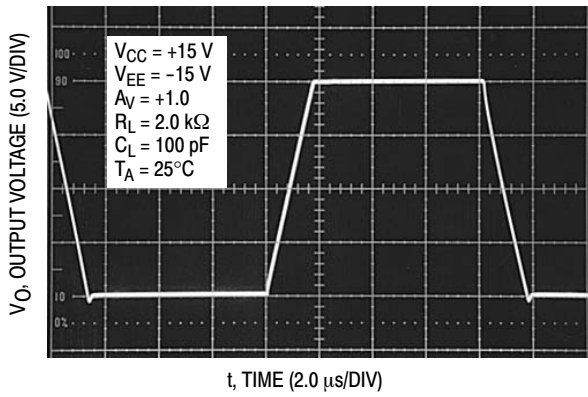**Figure 32. Percent Overshoot versus
Load Capacitance**

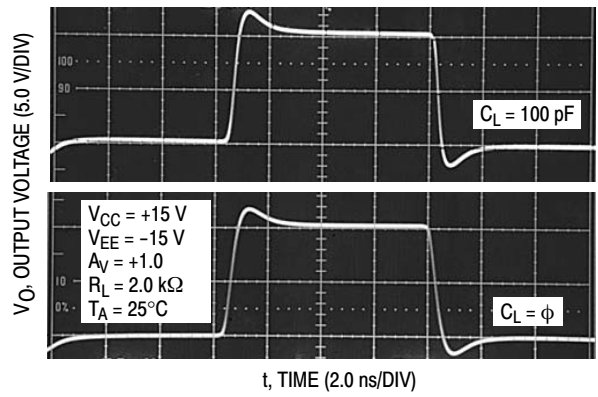**Figure 33. Non−inverting Amplifier Slew Rate
for the MC33274**

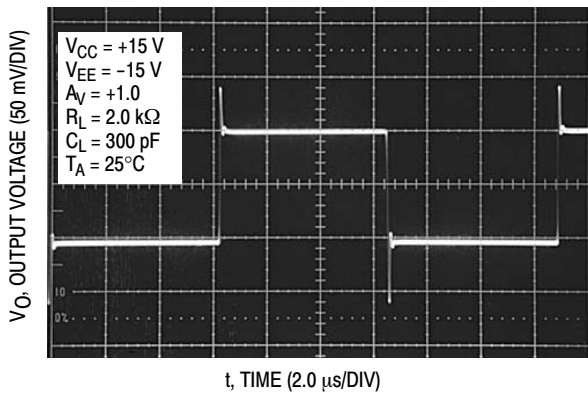**Figure 34. Non−inverting Amplifier Overshoot
for the MC33274**
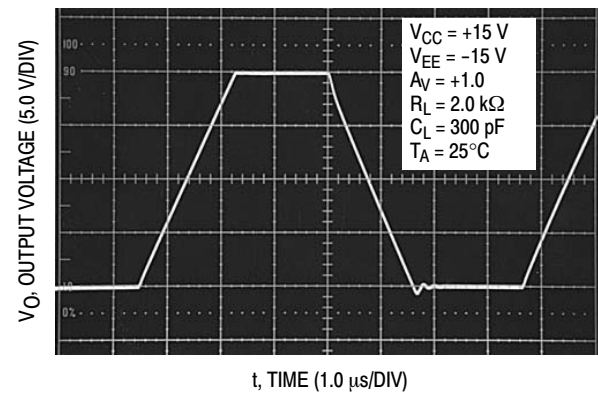

**Figure 35. Small Signal Transient Response
for MC33274**

**Figure 36. Large Signal Transient Response
for MC33274**

ORDERING INFORMATION

Device	Package	Shipping†
MC33272AD	SOIC−8	98 Units / Rail
MC33272ADG	SOIC−8 (Pb−Free)	
MC33272ADR2	SOIC−8	2500 / Tape & Reel
MC33272ADR2G	SOIC−8 (Pb−Free)	
MC33272AP	PDIP−8	50 Units / Rail
MC33272APG	PDIP−8 (Pb−Free)	
NCV33272ADR2*	SOIC−8	2500 / Tape & Reel
NCV33272ADR2G*	SOIC−8 (Pb−Free)	
MC33274AD	SOIC−14	55 Units / Rail
MC33274ADG	SOIC−14 (Pb−Free)	
MC33274ADR2	SOIC−14	2500 / Tape & Reel
MC33274ADR2G	SOIC−14 (Pb−Free)	
MC33274ADTBR2G	TSSOP−14 (Pb−Free)	
MC33274AP	PDIP−14	25 Units / Rail
MC33274APG	PDIP−14 (Pb−Free)	
NCV33274AD*	SOIC−14	55 Units / Rail
NCV33274ADG*	SOIC−14 (Pb−Free)	
NCV33274ADR2*	SOIC−14	2500 / Tape & Reel
NCV33274ADR2G*	SOIC−14 (Pb−Free)	
NCV33274ADTBR2G*	TSSOP−14 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

PDIP−8
P SUFFIX
CASE 626−05
ISSUE N

TOP VIEW

END VIEW
WITH LEADS CONSTRAINED
NOTE 5

SIDE VIEW

END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-AGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION E3 IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE R

TOP VIEW

END VIEW
WITH LEADS CONSTRAINED
NOTE 5

SIDE VIEW

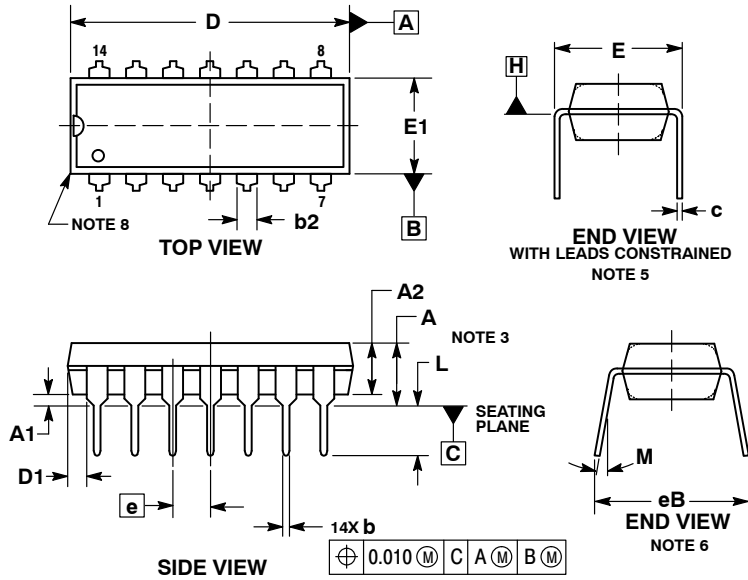⊕ | 0.010 Ⓜ | C | A Ⓜ | B Ⓜ

END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-AGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION E3 IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

| DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AK
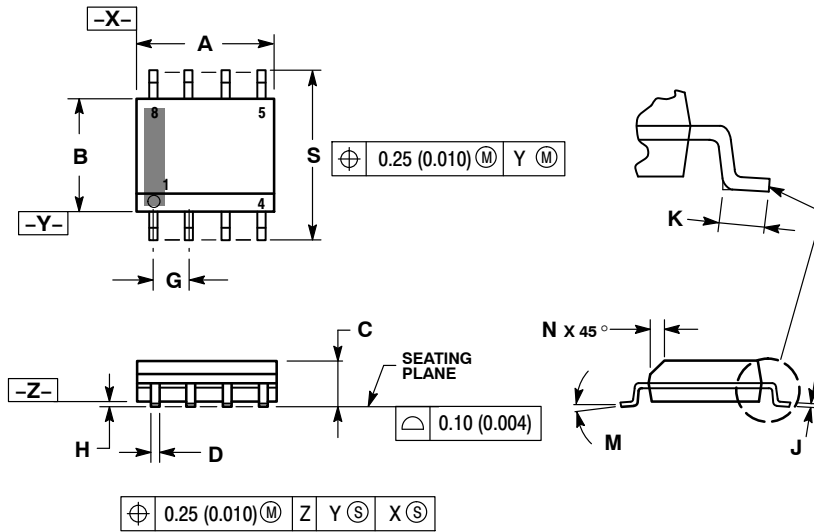
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*
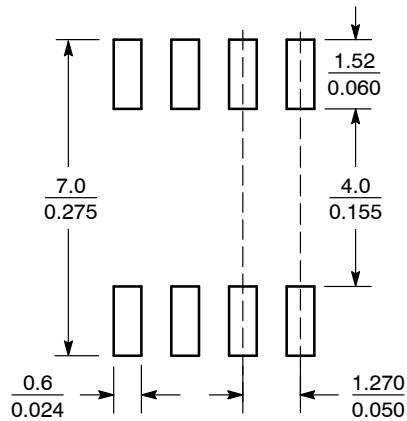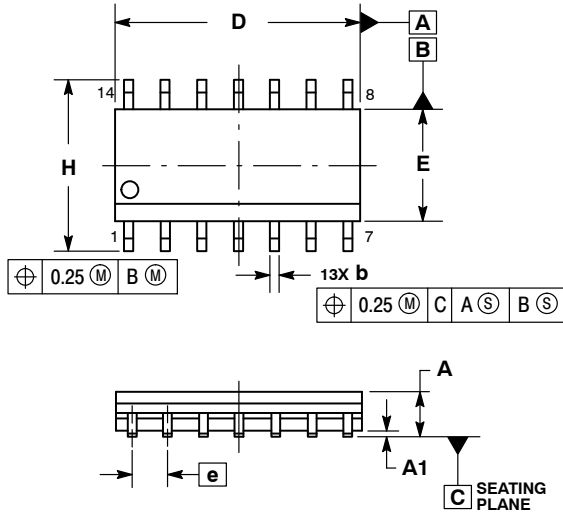

SCALE 6:1 $\left(\dfrac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
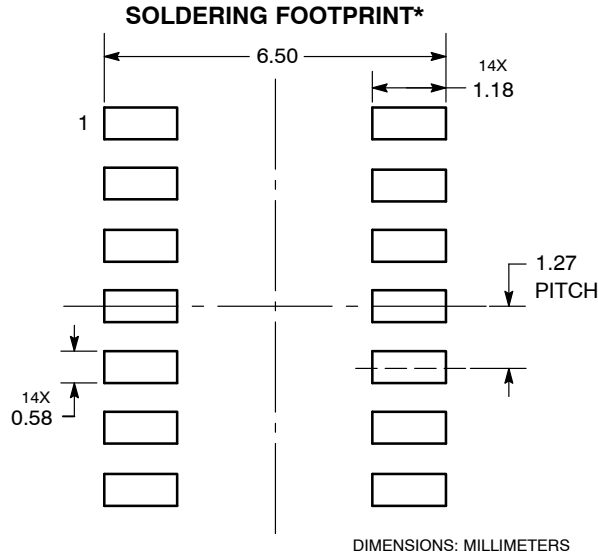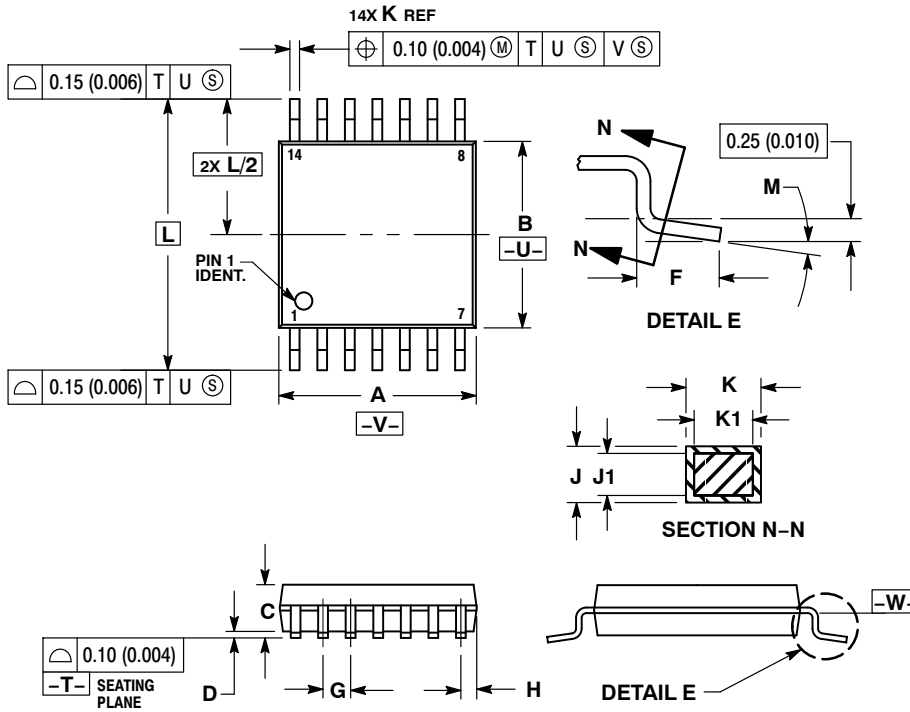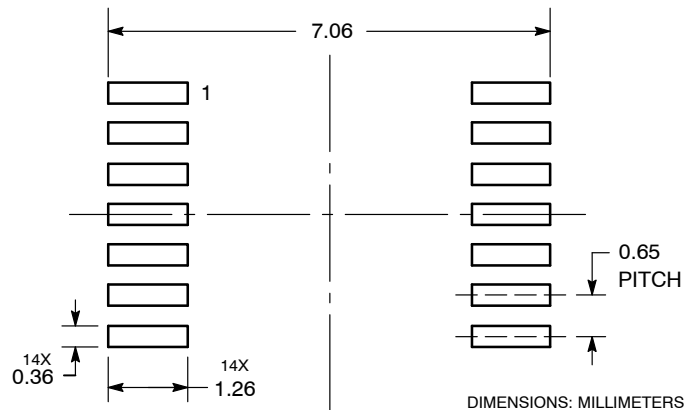
PACKAGE DIMENSIONS

SOIC−14
CASE 751A−03
ISSUE K

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DETAIL A

SEATING PLANE

DIM	MILLIMETERS		INCHES	
	MIN	**MAX**	**MIN**	**MAX**
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*

6.50

14X
1.18

1
1.27
PITCH

14X
0.58

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP−14
CASE 948G
ISSUE B

14X K REF

⊕ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

◁ | 0.15 (0.006) | T U Ⓢ

2X L/2

L

14 **8**

B

−U−

PIN 1
IDENT.

1 **7**

◁ | 0.15 (0.006) | T U Ⓢ

A

−V−

N

0.25 (0.010)

M

N

F

DETAIL E

K
K1

J J1

SECTION N−N

C

◁ | 0.10 (0.004)

−T− SEATING
PLANE

D **G** **H**

−W−

DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

14X
0.36

14X
1.26

DIMENSIONS: MILLIMETERS

MC33272A/D

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Amplifier IC Development Tools *category:*

Click to view products by ON Semiconductor *manufacturer:*

Other Similar products are found below :

EVAL-ADCMP562BRQZ EVAL-ADCMP565BPZ EVAL-ADCMP566BCPZ EVAL-ADCMP607BCPZ EVAL-ADM1191EBZ EVAL-HSOPAMP-1CPZ 125932-HMC874LC3C AD8003ACP-EBZ AD8013AR-14-EBZ AD8033AKS-EBZ AD8040AR-EBZ AD8044AR-EBZ AD8129AR-EBZ AD8225-EVALZ ADA4853-3YRU-EBZ ADA4859-3ACP-EBZ ADA4861-3YR-EBZ ADA4862-3YR-EBZ ADA4891-3AR-EBZ ADA4950-2YCP-EBZ DEM-OPA-SOT-1B OPA653EVM LMH6553SDEVAL/NOPB EVAL-ADCMP561BRQZ AD744JR-EBZ AD8004AR-EBZ AD8023AR-EBZ AD8030ARJ-EBZ AD8039ART-EBZ AD8040ARU-EBZ AD8054AR-EBZ AD8073JR-EBZ AD813AR-14-EBZ AD8232-EVALZ AD8304-EVALZ AD8335-EVALZ AD8336-EVALZ AD848JR-EBZ ADA4850-2YCP-EBZ ADA4853-2YCP-EBZ ADA4858-3ACP-EBZ ADA4922-1ACP-EBZ ADCMP380-EVALZ ADL5390-EVALZ THS4513EVM THS7347EVM 551600075-001/NOPB 551600083-001/NOPB BUF12840EVM DEM-OPA-SO-2E