# Freescale Semiconductor, Inc.

**Addendum**

*HC908LJ12AD/D*
*Rev. 0, 6/2003*

*Addendum to*
*MC68HC908LJ12*
*Technical Data*

**Freescale Semiconductor, Inc.**

This addendum provides information to the following MCU devices:

- **MC68HLC908LJ12** (*see page 1*)
- **MC68HC08LJ12** (*see page 9*)

The entire *MC68HC908LJ12 Technical Data*, Rev. 2 (Motorola document number MC68HC908LJ12/D) applies to the these two devices, with exceptions outlined in this addendum.

Amendments to *MC68HC908LJ12/D*, Rev. 2, are documented on *page 13*.

## MC68HLC908LJ12

The MC68HLC908LJ12 is a low-voltage version of the MC68HC908LJ12, with an operating voltage range of 2.4 to 3.3V.

**FLASH Memory**
The FLASH memory can be read at operating voltages from 2.4 to 3.3V. Program or erase operations require a minimum operating voltage of 2.7V.

**Low-Voltage Inhibit (LVI)**
The LVI module is not designed for the MC68HLC908LJ12. After an MCU reset, the LVI module is disabled (LVIPWRD = 1 in CONFIG1). The LVIPWRD bit should be left as logic 1 (the default setting).

**Electrical Specifications**
Electrical specifications for the MC68HLC908LJ12 device are given in the following tables.

*Functional Operating
Range*

**Table 1. Operating Range**

| Characteristic | Symbol | Value | | Unit |
|---|---|---|---|---|
| Operating temperature range | $T_A$ | −40 to +85 | | °C |
| Operating voltage range | $V_{DD}$ | 2.4 to 2.7 | 2.7 to 3.3 | V |
| Maximum internal operating frequency | $f_{OP}$ | 2 | 4 | MHz |
| Operating voltage for FLASH memory program and erase operations | $V_{DD}$ | 2.7 to 3.3 | | V |

*DC Electrical
Characteristics*

**Table 2. DC Electrical Characteristics (2.4 to 2.7V)**

| Characteristic[1] | Symbol | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage ($I_{LOAD}$ = −1.0 mA) All ports | $V_{OH}$ | $V_{DD}$−0.4 | — | — | V |
| Output low voltage ($I_{LOAD}$ = 0.8mA) All ports ($I_{LOAD}$ = 4.0 mA) PTB2–PTB5 ($I_{LOAD}$ = 10.0 mA) PTB0/TxD–PTB1 | $V_{OL}$ | — | — | 0.4 | V |
| Input high voltage All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1 | $V_{IH}$ | $0.7 \times V_{DD}$ | — | $V_{DD}$ | V |
| Input low voltage All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1 | $V_{IL}$ | $V_{SS}$ | — | $0.3 \times V_{DD}$ | V |
| $V_{DD}$ supply current Run[3], $f_{OP}$ = 2 MHz   with all modules on   with ADC on   with ADC off Wait[4], $f_{OP}$ = 2 MHz (all modules off) Stop, $f_{OP}$ = 8 kHz[5]   25°C (with OSC, RTC, LCD[6], LVI on)   25°C (with OSC, RTC, LCD[6] on)   25°C (with OSC, RTC on)   25°C (all modules off) | $I_{DD}$ | — — — — — — — — | — — — — — — — — | 5.2 3.8 2.8 2.3 200 27 15 1 | mA mA mA mA μA μA μA μA |
| Digital I/O ports Hi-Z leakage current All ports, $\overline{RST}$ | $I_{IL}$ | — | — | ± 10 | μA |

**Table 2. DC Electrical Characteristics (2.4 to 2.7 V) (Continued)**

| Characteristic[1] | Symbol | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|
| Input current $\overline{IRQ}$ | $I_{IN}$ | — | — | $\pm 1$ | μA |
| Capacitance   Ports (as input or output) | $C_{OUT}$ $C_{IN}$ | — — | — — | 12 8 | pF |
| POR re-arm voltage[7] | $V_{POR}$ | 0 | — | 100 | mV |
| POR rise-time ramp rate[8] | $R_{POR}$ | 0.02 | — | — | V/ms |
| Monitor mode entry voltage (at $\overline{IRQ}$ pin) | $V_{HI}$ | $1.5 \times V_{DD}$ | — | $2 \times V_{DD}$ | V |
| Pullup resistors[9]   PTA0–PTA3, PTD4–PTD7 configured as KBI0–KBI7   $\overline{RST}$, $\overline{IRQ}$ | $R_{PU1}$ $R_{PU2}$ | — — | 25 27 | — — | kΩ kΩ |

1. $V_{DD}$ = 2.4 to 2.7 Vdc, $V_{SS}$ = 0 Vdc, $T_A$ = $T_L$ to $T_H$, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. Run (operating) $I_{DD}$ measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. $C_L$ = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run $I_{DD}$.
4. Wait $I_{DD}$ measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. $C_L$ = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects wait $I_{DD}$.
5. The 8kHz clock is from a 32kHz clock input at OSC1, for the driving the RTC.
6. LCD driver configured for low current mode.
7. Maximum is highest voltage that POR is guaranteed.
8. If minimum $V_{DD}$ is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum $V_{DD}$ is reached.
9. $R_{PU1}$ and $R_{PU2}$ are measured at $V_{DD}$ = 2.6 V.

**Table 3. DC Electrical Characteristics (2.7 to 3.3 V)**

| Characteristic[1] | Symbol | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage ($I_{LOAD}$ = −1.0 mA)   All ports | $V_{OH}$ | $V_{DD}-0.4$ | — | — | V |
| Output low voltage   ($I_{LOAD}$ = 0.8mA) All ports   ($I_{LOAD}$ = 4.0 mA) PTB2–PTB5   ($I_{LOAD}$ = 10.0 mA) PTB0/TxD–PTB1 | $V_{OL}$ | — | — | 0.4 | V |
| Input high voltage   All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1 | $V_{IH}$ | $0.7 \times V_{DD}$ | — | $V_{DD}$ | V |
| Input low voltage   All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1 | $V_{IL}$ | $V_{SS}$ | — | $0.3 \times V_{DD}$ | V |

**Table 3. DC Electrical Characteristics (2.7 to 3.3 V) (Continued)**

| Characteristic[1] | Symbol | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ supply current | | | | | |
| Run[3], $f_{OP}$ = 4 MHz | | | | | |
|   with all modules on | | — | — | 8 | mA |
|   with ADC on | | — | — | 6 | mA |
|   with ADC off | | — | — | 5 | mA |
| Wait[4], $f_{OP}$ = 4 MHz (all modules off) | $I_{DD}$ | — | — | 3.5 | mA |
| Stop, $f_{OP}$ = 8 kHz[5] | | | | | |
|   25°C (with OSC, RTC, LCD[6], LVI on) | | — | — | 280 | μA |
|   25°C (with OSC, RTC, LCD[6] on) | | — | — | 38 | μA |
|   25°C (with OSC, RTC on) | | — | — | 15 | μA |
|   25°C (all modules off) | | — | — | 1 | μA |
| Digital I/O ports Hi-Z leakage current<br>  All ports, $\overline{RST}$ | $I_{IL}$ | — | — | ± 10 | μA |
| Input current<br>  $\overline{IRQ}$ | $I_{IN}$ | — | — | ± 1 | μA |
| Capacitance<br>  Ports (as input or output) | $C_{OUT}$<br>$C_{IN}$ | —<br>— | —<br>— | 12<br>8 | pF |
| POR re-arm voltage[7] | $V_{POR}$ | 0 | — | 100 | mV |
| POR rise-time ramp rate[8] | $R_{POR}$ | 0.02 | — | — | V/ms |
| Monitor mode entry voltage (at $\overline{IRQ}$ pin) | $V_{HI}$ | $1.5 \times V_{DD}$ | — | $2 \times V_{DD}$ | V |
| Pullup resistors[9]<br>  PTA0–PTA3, PTD4–PTD7 configured as KBI0–KBI7<br>  $\overline{RST}$, $\overline{IRQ}$ | $R_{PU1}$<br>$R_{PU2}$ | —<br>— | 25<br>27 | —<br>— | kΩ<br>kΩ |

1. $V_{DD}$ = 2.7 to 3.3 Vdc, $V_{SS}$ = 0 Vdc, $T_A = T_L$ to $T_H$, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. Run (operating) $I_{DD}$ measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. $C_L$ = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run $I_{DD}$.
4. Wait $I_{DD}$ measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. $C_L$ = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects wait $I_{DD}$.
5. The 8kHz clock is from a 32kHz clock input at OSC1, for the driving the RTC.
6. LCD driver configured for low current mode.
7. Maximum is highest voltage that POR is guaranteed.
8. If minimum $V_{DD}$ is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum $V_{DD}$ is reached.
9. $R_{PU1}$ and $R_{PU2}$ are measured at $V_{DD}$ = 3V.

*Oscillator*
*Characteristics*

### Table 4. Oscillator Specifications (2.4 to 2.7 V)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Internal oscillator clock frequency | $f_{ICLK}$ | — | See **Figure 1**. | — | Hz |
| External reference clock to OSC1[1] | $f_{OSC}$ | dc | — | 8M | Hz |
| Crystal reference frequency[2] | $f_{XCLK}$ | | 32.768k | 4.9152M | Hz |
| Crystal load capacitance[3] | $C_L$ | — | — | — | |
| Crystal fixed capacitance | $C_1$ | — | $2 \times C_L$ (25p) | — | F |
| Crystal tuning capacitance | $C_2$ | — | $2 \times C_L$ (25p) | — | F |
| Feedback bias resistor | $R_B$ | — | 10M | — | Ω |
| Series resistor[4] | $R_S$ | — | 100k | — | Ω |

1. No more than 10% duty cycle deviation from 50%.
2. Fundamental mode crystals only.
3. Consult crystal manufacturer's data.
4. Not Required for high frequency crystals.

### Table 5. Oscillator Specifications (2.7 to 3.3 V)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Internal oscillator clock frequency | $f_{ICLK}$ | — | See **Figure 1**. | — | Hz |
| External reference clock to OSC1[1] | $f_{OSC}$ | dc | — | 16M | Hz |
| Crystal reference frequency[2] | $f_{XCLK}$ | | 32.768k | 4.9152M | Hz |
| Crystal load capacitance[3] | $C_L$ | — | — | — | |
| Crystal fixed capacitance | $C_1$ | — | $2 \times C_L$ (25p) | — | F |
| Crystal tuning capacitance | $C_2$ | — | $2 \times C_L$ (25p) | — | F |
| Feedback bias resistor | $R_B$ | — | 10M | — | Ω |
| Series resistor[4] | $R_S$ | — | 100k | — | Ω |

1. No more than 10% duty cycle deviation from 50%.
2. Fundamental mode crystals only.
3. Consult crystal manufacturer's data.
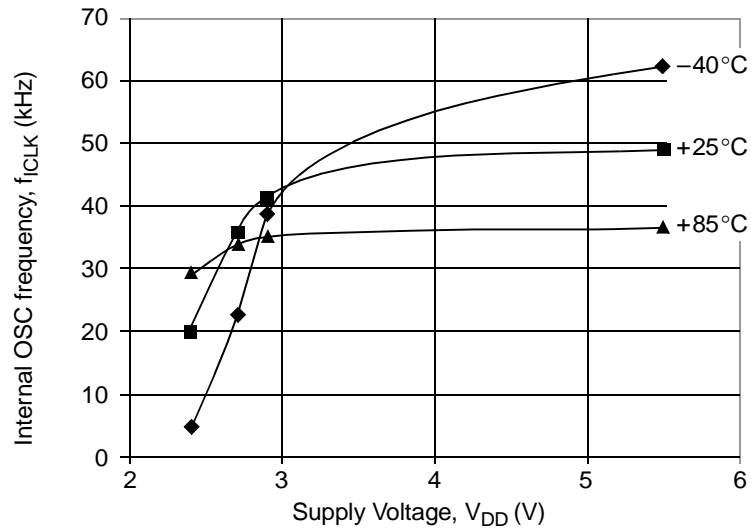4. Not Required for high frequency crystals.

**Figure 1. Typical Internal Oscillator Frequency**

*ADC Electrical Characteristics*
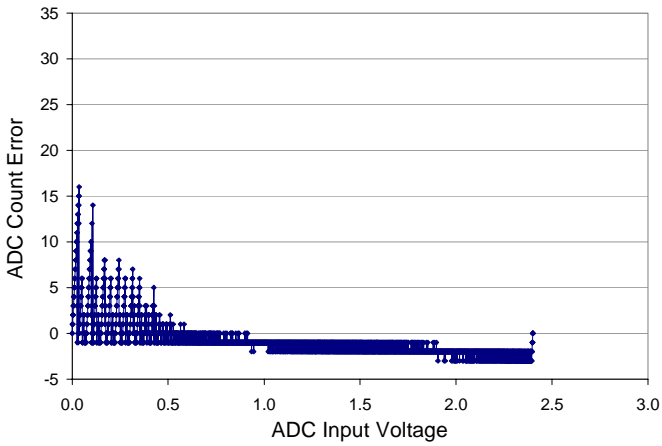
**Table 6. ADC Electrical Characteristics (2.4 to 3.3 V)**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDA}$ | 2.4 | 3.3 | V | |
| Input range | $V_{ADIN}$ | 0 | $V_{DDA}$ | V | $V_{ADIN} \leq V_{DDA}$ |
| Resolution | $B_{AD}$ | 10 | 10 | bits | 1,024 counts |
| Absolute accuracy | $A_{AD}$ | See **Figure 2** and **Figure 3**. | | | Includes quantization. $\pm 1$ ADC count = $\pm 0.5$ LSB |
| ADC internal clock | $f_{ADIC}$ | 32 k | 2 M | Hz | $t_{ADIC} = 1/f_{ADIC}$ |
| Conversion range | $R_{AD}$ | $V_{REFL}$ | $V_{REFH}$ | V | |
| ADC voltage reference high | $V_{REFH}$ | — | $V_{DDA} + 0.1$ | V | |
| ADC voltage reference low | $V_{REFL}$ | $V_{SSA} - 0.1$ | — | V | $V_{SSA}$ is tied to $V_{SS}$ internally. |
| Conversion time | $t_{ADC}$ | 16 | 17 | $t_{ADIC}$ cycles | |
| Sample time | $t_{ADS}$ | 5 | — | $t_{ADIC}$ cycles | |
| Monotonically | $M_{AD}$ | Guaranteed | | | |
| Zero input reading | $Z_{ADI}$ | 000 | 001 | HEX | $V_{ADIN} = V_{REFL}$ |
| Full-scale reading | $F_{ADI}$ | 3FC | 3FF | HEX | $V_{ADIN} = V_{REFH}$ |
| Input capacitance | $C_{ADI}$ | — | 20 | pF | Not tested. |
| Input impedance | $R_{ADI}$ | 20M | — | $\Omega$ | Measured at 5V |
| $V_{REFH}/V_{REFL}$ | $I_{VREF}$ | — | 1.6 | mA | Not tested. |

*Addendum to MC68HC908LJ12 Technical Data*
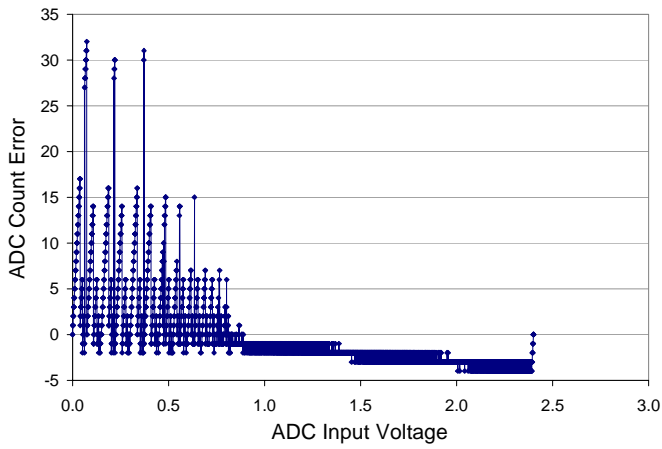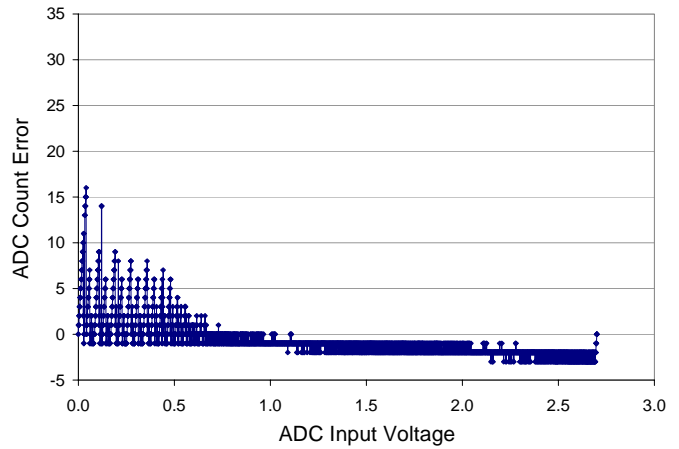
**(a) V$_{DD}$ = 2.4V at −40°C**

**(b) V$_{DD}$ = 2.4V at 25°C**

**(c) V$_{DD}$ = 2.4V at 85°C**

**(d) V$_{DD}$ = 2.7V at −40°C**
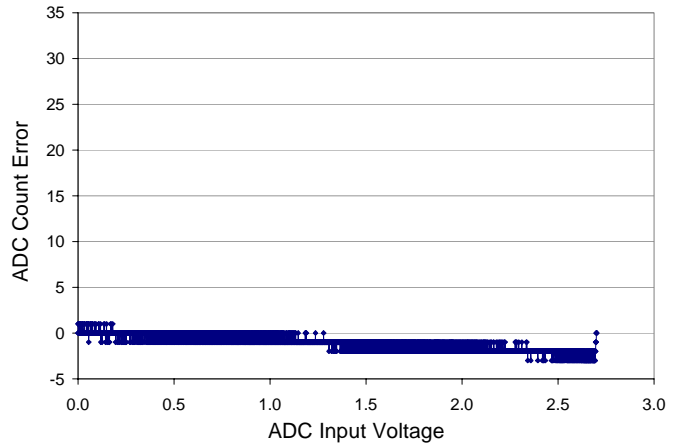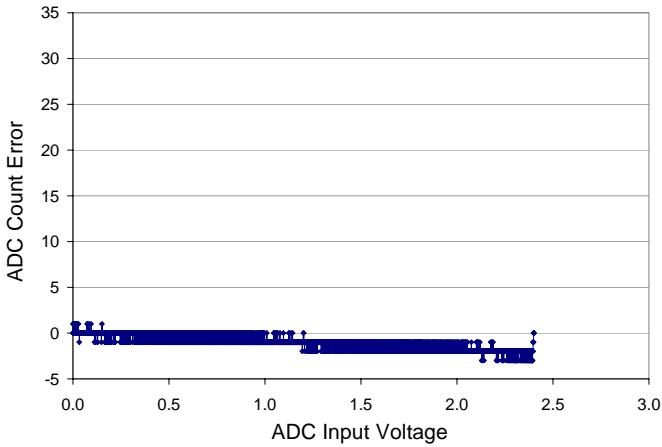
**(e) V$_{DD}$ = 2.7V at 25°C**
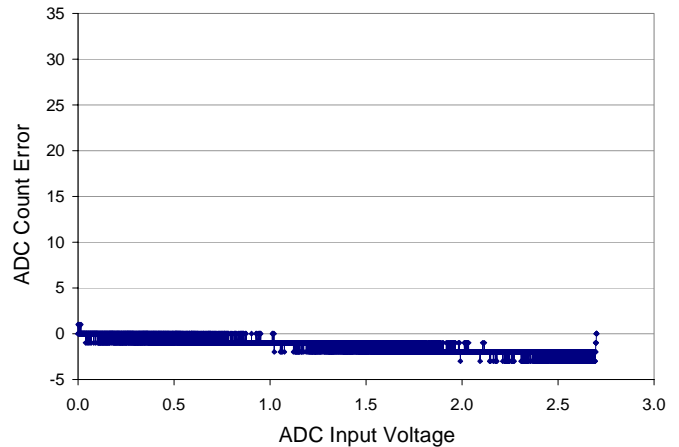
**(f) V$_{DD}$ = 2.7V at 85°C**

**Note: ADC performance increases with increase in operating voltage and temperature.**

**Figure 2. Typical ADC Accuracy (2.4V and 2.7V)**

*Addendum to MC68HC908LJ12 Technical Data*

$V_{DD}$ = 3.0 to 3.3V, at −40 to 85°C
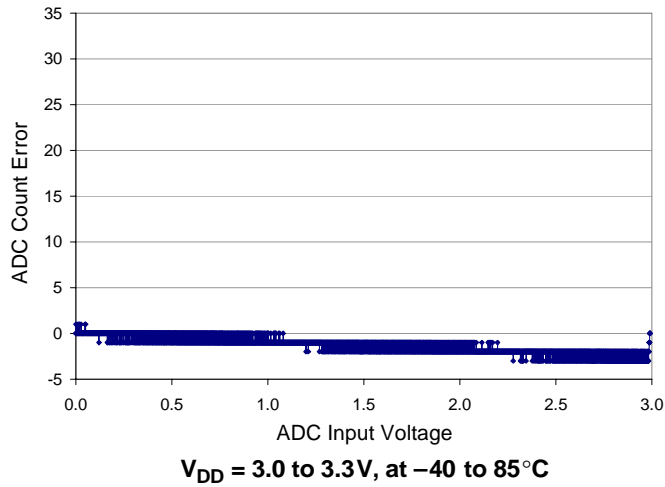
**Figure 3. Typical ADC Accuracy (3V and 3.3V)**

*Memory Characteristics*

At an operating voltage of less than 2.7 V, the FLASH memory can only be read. Program and erase are achieved at an operating voltage of 2.7 to 3.3V. The program and erase parameters in the *MC68HC908LJ12 Technical Data* are for $V_{DD}$ = 2.7 to 3.3V only.

**MC68HLC908LJ12 Order Numbers**

**Table 7** shows the ordering numbers for the MC68HLC908LJ12.

**Table 7. MC68HLC908LJ12 Order Numbers**

| MC Order Number [1] | Package | Operating Temperature Range |
|---|---|---|
| MC68HLC98LJ12CFB | 52-pin LQFP | −40 °C to +85 °C |
| MC68HLC98LJ12CPB | 64-pin LQFP | −40 °C to +85 °C |
| MC68HLC98LJ12CFU | 64-pin QFP | −40 °C to +85 °C |

1. The missing "0" in "908" is intentional.

## MC68HC08LJ12

The MC68HC08LJ12 is the ROM part equivalent to the MC68HC908LJ12.

**Table 8. Summary of MC68HC08LJ12 and MC68HC908LJ12 Differences**

|  | MC68HC08LJ12 | MC68HC908LJ12 |
|---|---|---|
| **Operating voltages** | —<br>5.0V ± 10% | 3.3V ± 10%<br>5.0V ± 10% |
| **Memory ($C000–$EFFF)** | 12,288 bytes ROM | 12,288 bytes FLASH |
| **User vectors ($FFD0–$FFFF)** | 48 bytes ROM | 48 bytes FLASH |
| **Registers at $FE08 and $FF09** | Not used;<br>   locations are reserved. | FLASH related registers.<br>$FE08 — FLCR<br>$FF09 — FLBPR |
| **Monitor ROM<br>($FC00–$FDFF and $FE10–$FFCF)** | Used for testing purposes only. | Used for testing and FLASH<br>   programming/erasing. |
| **Available packages** | 52-pin LQFP<br>64-pin LQFP<br>64-pin QFP | 52-pin LQFP<br>64-pin LQFP<br>64-pin QFP |

**MCU Block Diagram**     **Figure 4** shows the block diagram of the MC68HC08LJ12.

**Memory Map**     The MC68HC08LJ128 has 12,288 bytes of user ROM from $C000 to $EFFF, and 48 bytes of user ROM vectors from $FFD0 to $FFFF. On the MC68HC908LJ12 these memory locations are FLASH memory.

**Figure 5** shows the memory map of the MC68HC08LJ12.

**Reserved Registers**     The two registers at $FE08 and $FE09 are reserved locations on the MC68HC08LJ12.

On the MC68HC908LJ12, these two locations are the FLASH control register and the FLASH block protect register respectively.

**Monitor ROM**     The monitor program (monitor ROM: $FE10–$FFCF and $FC00–$FDFF) on the MC68HC08LJ12 is for device testing only.
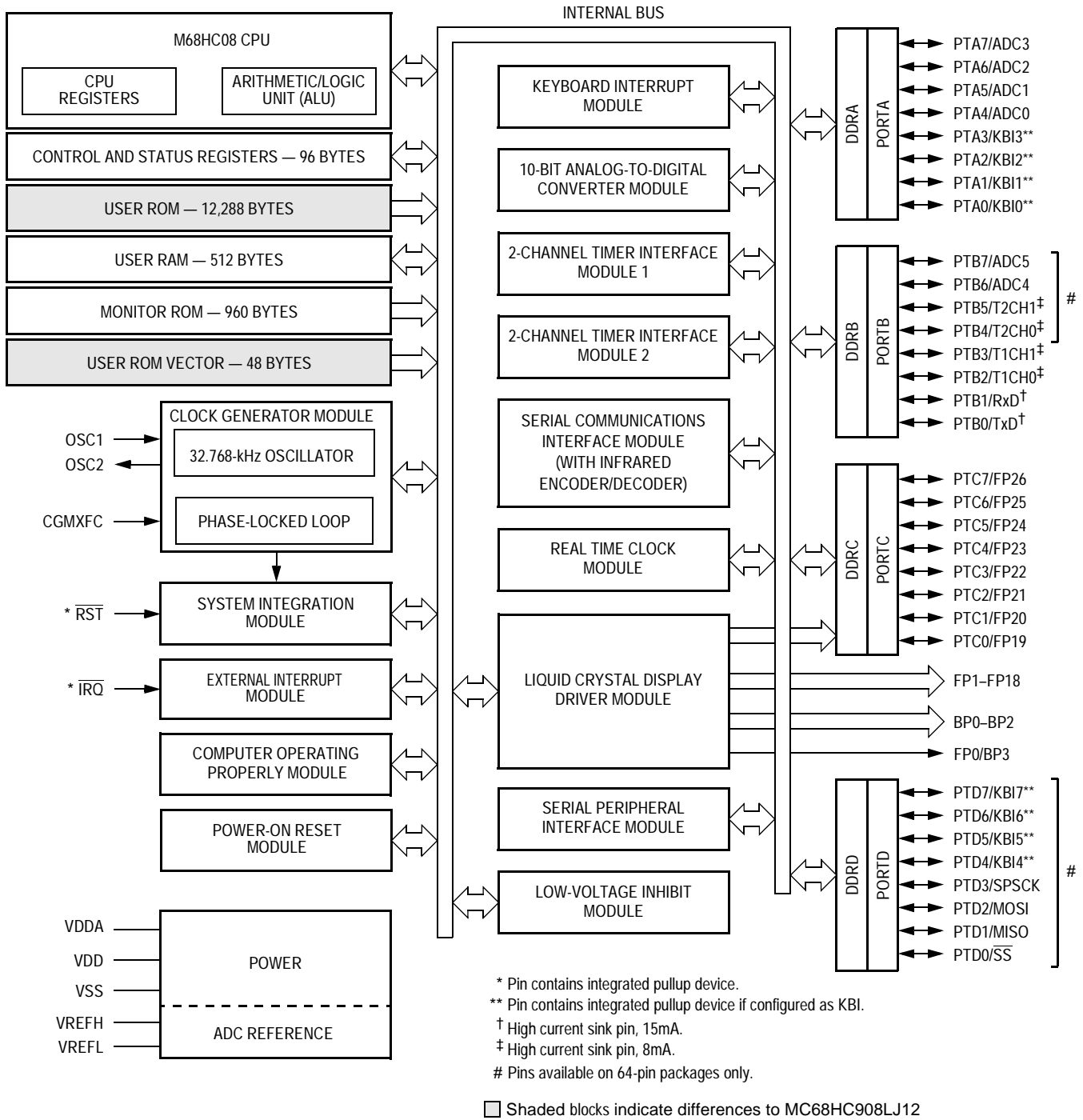
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INTERNAL BUS

**M68HC08 CPU**

CPU REGISTERS

ARITHMETIC/LOGIC UNIT (ALU)

CONTROL AND STATUS REGISTERS — 96 BYTES

USER ROM — 12,288 BYTES

USER RAM — 512 BYTES

MONITOR ROM — 960 BYTES

USER ROM VECTOR — 48 BYTES

**CLOCK GENERATOR MODULE**

OSC1

OSC2

32.768-kHz OSCILLATOR

CGMXFC

PHASE-LOCKED LOOP

* RST

SYSTEM INTEGRATION MODULE

* IRQ

EXTERNAL INTERRUPT MODULE

COMPUTER OPERATING PROPERLY MODULE

POWER-ON RESET MODULE

VDDA

VDD

VSS

POWER

VREFH

VREFL

ADC REFERENCE

KEYBOARD INTERRUPT MODULE

10-BIT ANALOG-TO-DIGITAL CONVERTER MODULE

2-CHANNEL TIMER INTERFACE MODULE 1

2-CHANNEL TIMER INTERFACE MODULE 2

SERIAL COMMUNICATIONS INTERFACE MODULE (WITH INFRARED ENCODER/DECODER)

REAL TIME CLOCK MODULE

LIQUID CRYSTAL DISPLAY DRIVER MODULE

SERIAL PERIPHERAL INTERFACE MODULE

LOW-VOLTAGE INHIBIT MODULE

DDRA / PORTA

PTA7/ADC3
PTA6/ADC2
PTA5/ADC1
PTA4/ADC0
PTA3/KBI3**
PTA2/KBI2**
PTA1/KBI1**
PTA0/KBI0**

DDRB / PORTB

PTB7/ADC5
PTB6/ADC4
PTB5/T2CH1‡
PTB4/T2CH0‡
PTB3/T1CH1‡
PTB2/T1CH0‡
PTB1/RxD†
PTB0/TxD†

#

DDRC / PORTC

PTC7/FP26
PTC6/FP25
PTC5/FP24
PTC4/FP23
PTC3/FP22
PTC2/FP21
PTC1/FP20
PTC0/FP19

FP1–FP18

BP0–BP2

FP0/BP3

DDRD / PORTD

PTD7/KBI7**
PTD6/KBI6**
PTD5/KBI5**
PTD4/KBI4**
PTD3/SPSCK
PTD2/MOSI
PTD1/MISO
PTD0/SS

#

\* Pin contains integrated pullup device.
\*\* Pin contains integrated pullup device if configured as KBI.
† High current sink pin, 15mA.
‡ High current sink pin, 8mA.
# Pins available on 64-pin packages only.

☐ Shaded blocks indicate differences to MC68HC908LJ12

**Figure 4. MC68HC08LJ12 Block Diagram**

For More Information On This Product,
Go to: www.freescale.com

| Address | Section |
|---|---|
| $0000 ↓ $005F | I/O Registers<br>96 Bytes |
| $0060 ↓ $025F | RAM<br>512 Bytes |
| $0260 ↓ $BFFF | Unimplemented<br>48,544 Bytes |
| $C000 ↓ $EFFF | ROM<br>12,288 Bytes |
| $F000 ↓ $FBFF | Unimplemented<br>3,072 Bytes |
| $FC00 ↓ $FDFF | Monitor ROM 1<br>512 Bytes |
| $FE00 | SIM Break Status Register (SBSR) |
| $FE01 | SIM Reset Status Register (SRSR) |
| $FE02 | Reserved |
| $FE03 | SIM Break Flag Control Register (SBFCR) |
| $FE04 | Interrupt Status Register 1 (INT1) |
| $FE05 | Interrupt Status Register 2 (INT2) |
| $FE06 | Interrupt Status Register 3 (INT3) |
| $FE07 | Reserved |
| $FE08 | Reserved |
| $FE09 | Reserved |
| $FE0A | Reserved |
| $FE0B | Reserved |
| $FE0C | Break Address Register High (BRKH) |
| $FE0D | Break Address Register Low (BRKL) |
| $FE0E | Break Status and Control Register (BRKSCR) |
| $FE0F | LVI Status Register (LVISR) |
| $FE10 ↓ $FFCF | Monitor ROM 2<br>448 Bytes |
| $FFD0 ↓ $FFFF | ROM Vectors<br>48 Bytes |

**Figure 5. MC68HC08LJ12 Memory Map**

**Electrical Specifications**

Electrical specifications for the MC68HC908LJ12 apply to the MC68HC08LJ12 except for the parameters indicated below.

*Functional Operating Range*

**Table 9. Operating Range**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Operating temperature range | $T_A$ | $-40$ to $+85$ | $^\circ$C |
| Operating voltage range | $V_{DD}$ | $5.0V \pm 10\%$ | V |

*RAM Memory Characteristics*

**Table 10. Memory Characteristics**

| Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| RAM data retention voltage | $V_{RDR}$ | 1.3 | — | V |

Notes:
  Since MC68HC08LJ12 is a ROM device, FLASH memory electrical characteristics do not apply.

**MC68HC08LJ12 Order Numbers**

These part numbers are generic numbers only. To place an order, ROM code must be submitted to the ROM Processing Center (RPC).

**Table 11. MC68HC08LJ12 Order Numbers**

| MC Order Number | Package | Operating Temperature Range |
|---|---|---|
| MC68HC08LJ12CFB | 52-pin LQFP | $-40\ ^\circ$C to $+85\ ^\circ$C |
| MC68HC08LJ12CPB | 64-pin LQFP | $-40\ ^\circ$C to $+85\ ^\circ$C |
| MC68HC08LJ12CFU | 64-pin QFP | $-40\ ^\circ$C to $+85\ ^\circ$C |

## AMENDMENTS TO MC68HC908LJ12/D, REV. 2

**5.0V DC Electrical Characteristics**  Pages 394 and 395, *Table 23-4 5.0V DC Electrical Characteristics* — Delete LVI typical values and correct note 6.

*From:*

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Low-voltage inhibit, trip falling voltage | $V_{TRIPF}$ | 4.00 | 4.32 | 4.70 | V |
| Low-voltage inhibit, trip rising voltage | $V_{TRIPR}$ | 4.00 | 4.32 | 4.70 | V |

**Notes**:
  6. LCD driver configured for high current mode.

*To:*

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Low-voltage inhibit, trip falling voltage | $V_{TRIPF}$ | 4.00 | — | 4.70 | V |
| Low-voltage inhibit, trip rising voltage | $V_{TRIPR}$ | 4.00 | — | 4.70 | V |

**Notes**:
  6. LCD driver configured for low current mode.

**3.3V DC Electrical Characteristics**  Pages 396 and 397, *Table 23-5 3.3V DC Electrical Characteristics* — Delete LVI typical values and correct note 6.

*From:*

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Low-voltage inhibit, trip falling voltage | $V_{TRIPF}$ | 2.40 | 2.57 | 2.88 | V |
| Low-voltage inhibit, trip rising voltage | $V_{TRIPR}$ | 2.46 | 2.63 | 2.97 | V |

**Notes**:
  6. LCD driver configured for high current mode.

*To:*

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Low-voltage inhibit, trip falling voltage | $V_{TRIPF}$ | 2.40 | — | 2.88 | V |
| Low-voltage inhibit, trip rising voltage | $V_{TRIPR}$ | 2.46 | — | 2.97 | V |

**Notes**:
  6. LCD driver configured for low current mode.

*Addendum to MC68HC908LJ12 Technical Data*

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**Oscillator Characteristics**    Page 398, ***Table 23-8 5.0V Oscillator Specifications*** and ***Table 23-9 3.3V Oscillator Specifications*** — Replace *Internal oscillator clock frequency* values.

*From:*

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Internal oscillator clock frequency | $f_{ICLK}$ | 46k | 47k | 48k | Hz |

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Internal oscillator clock frequency | $f_{ICLK}$ | 42.8k | 43.4k | 44k | Hz |

*To:*    See **Figure 1 . Typical Internal Oscillator Frequency** on page 6 of this document.

**— END —**

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HC908LJ12AD/D
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