MTP3N50E

Designer's™ Data Sheet

TMOS E-FET ™
High Energy Power FET
N−Channel Enhancement−Mode Silicon Gate

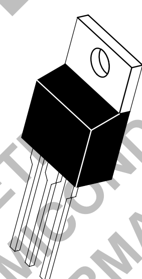
ON Semiconductor®

http://onsemi.com

TMOS POWER FET
3.0 AMPERES, 500 VOLTS
$R_{DS(on)}$ = 3.0 Ω

This advanced high voltage TMOS E−FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain−to−source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source−to−Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source−to−Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



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CASE 221A−06
Style 5

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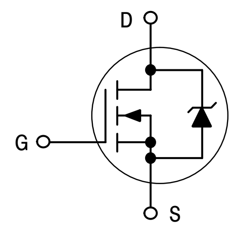


MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	500	Vdc
Drain−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate−Source Voltage — Continuous — Non−repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	3.0 10	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

UNCLAMPED DRAIN−TO−SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain−to−Source Avalanche Energy — T_J = 25°C — T_J = 100°C Repetitive Pulse Drain−to−Source Avalanche Energy	W_{DSR} (1) W_{DSR} (2)	210 33 5.0	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) V_{DD} = 50 V, I_D = 3.0 A
(2) Pulse Width and frequency is limited by T_J(max) and thermal response

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	500	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 500 V, V_{GS} = 0) (V_{DS} = 400 V, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	— —	0.25 1.0	mAdc
Gate−Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate−Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mAdc) (T_J = 125°C)		$V_{GS(th)}$	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	—	2.4	3.0	Ohm
Drain−Source On−Voltage (V_{GS} = 10 Vdc) (I_D = 3.0 A) (I_D = 1.5 A, T_J = 100°C)		$V_{DS(on)}$	— —	— —	10 8.0	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.5 Adc)		g_{FS}	1.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	435	—	pF
Output Capacitance		C_{oss}	—	56	—	
Transfer Capacitance		C_{rss}	—	9.2	—	
SWITCHING CHARACTERISTICS*						
Turn−On Delay Time	(V_{DD} = 250 V, I_D ≈ 3.0 A, R_G = 18 Ω, R_L = 83 Ω, $V_{GS(on)}$ = 10 V)	$t_{d(on)}$	—	14	—	ns
Rise Time		t_r	—	14	—	
Turn−Off Delay Time		$t_{d(off)}$	—	30	—	
Fall Time		t_f	—	20	—	
Total Gate Charge	(V_{DS} = 400 V, I_D = 3.0 A, V_{GS} = 10 V)	Q_g	—	15	21	nC
Gate−Source Charge		Q_{gs}	—	2.5	—	
Gate−Drain Charge		Q_{gd}	—	10	—	
SOURCE−DRAIN DIODE CHARACTERISTICS*						
Forward On−Voltage	(I_S = 3.0 A)	V_{SD}	—	—	1.5	Vdc
Forward Turn−On Time	(I_S = 3.0 A, di/dt = 100 A/μs)	t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	200	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	—	7.5	—	

* Indicates Pulse Test: Pulse Width = 300 μs Max, Duty Cycle ≤ 2.0%.
** Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

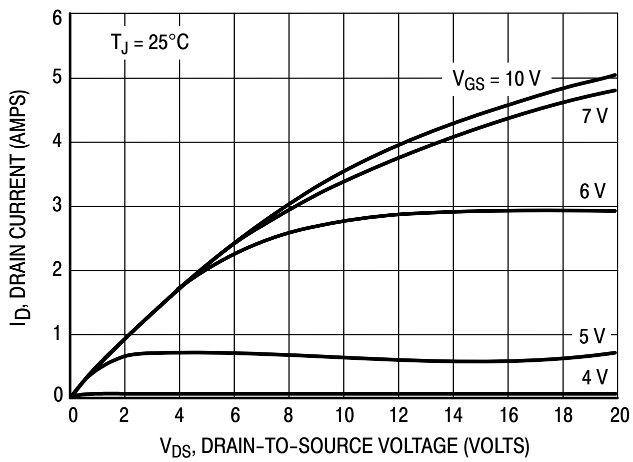


Figure 1. On−Region Characteristics

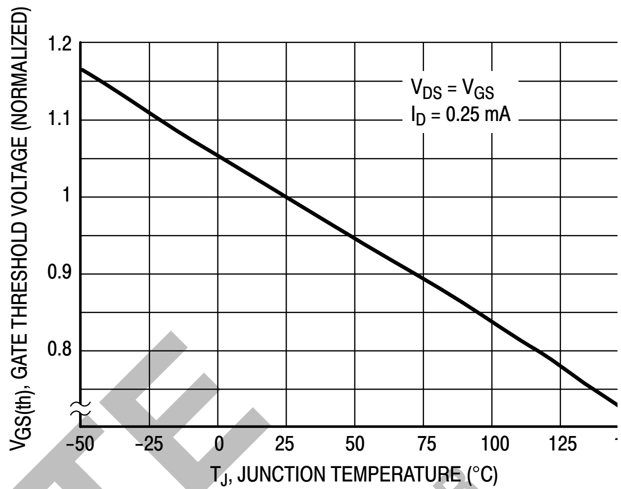


Figure 2. Gate−Threshold Voltage Variation With Temperature

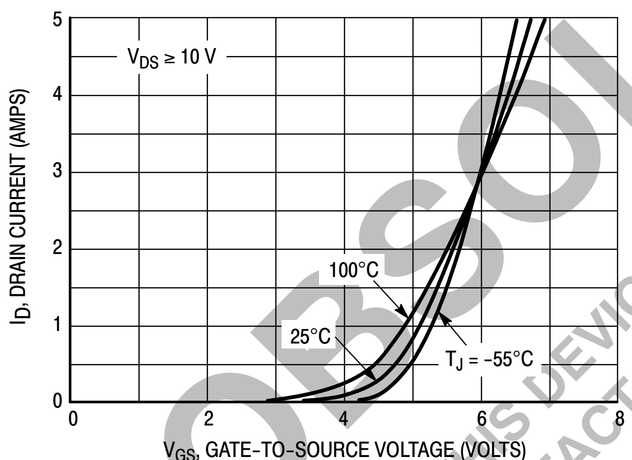


Figure 3. Transfer Characteristics

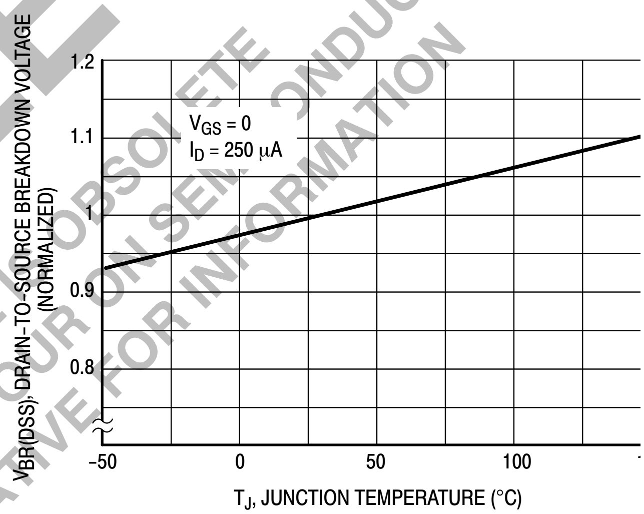


Figure 4. Breakdown Voltage Variation With Temperature

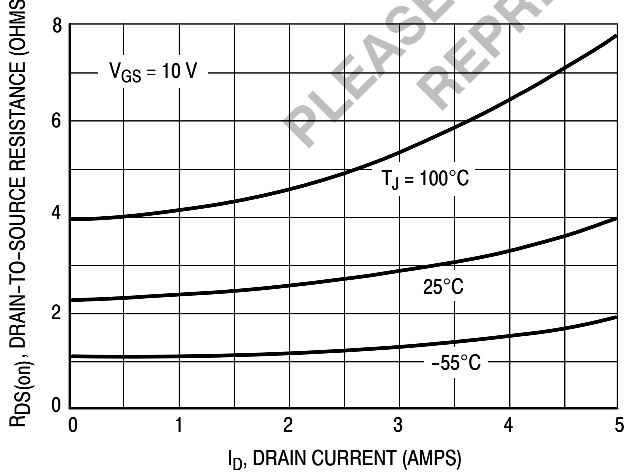


Figure 5. On−Resistance versus Drain Current

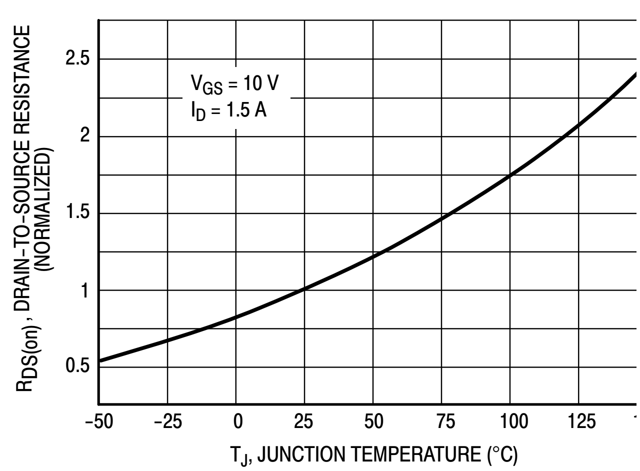


Figure 6. On−Resistance versus Temperature

SAFE OPERATING AREA INFORMATION

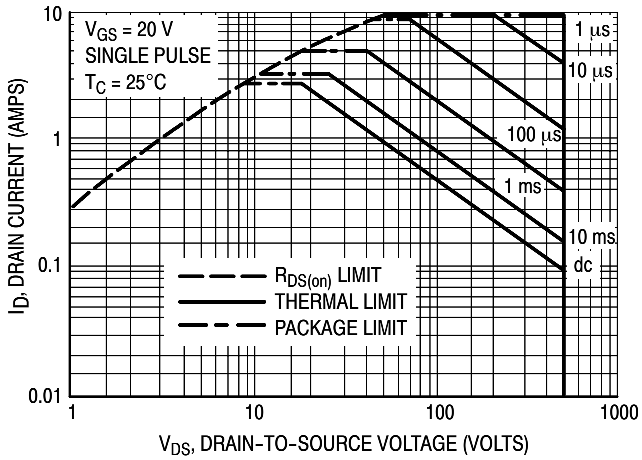


Figure 7. Maximum Rated Forward Biased Safe Operating Area

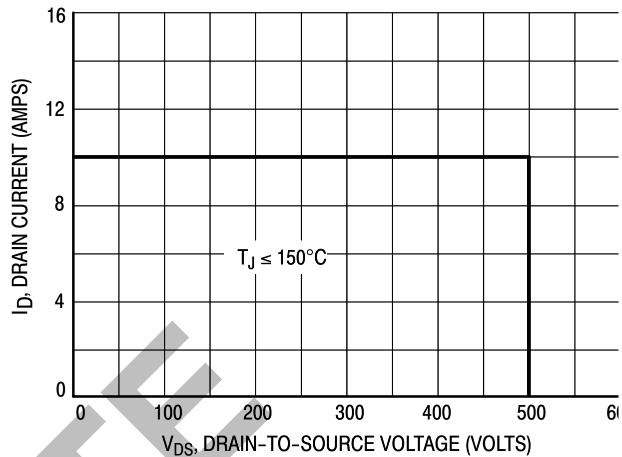


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain−to−source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance−General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn−on and turn−off of the devices for switching times less than one microsecond.

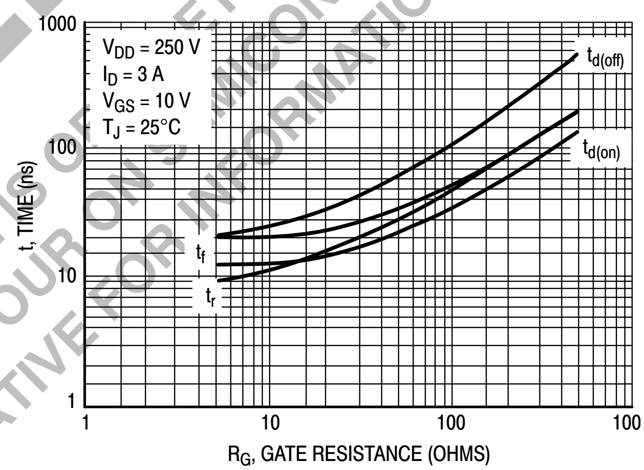
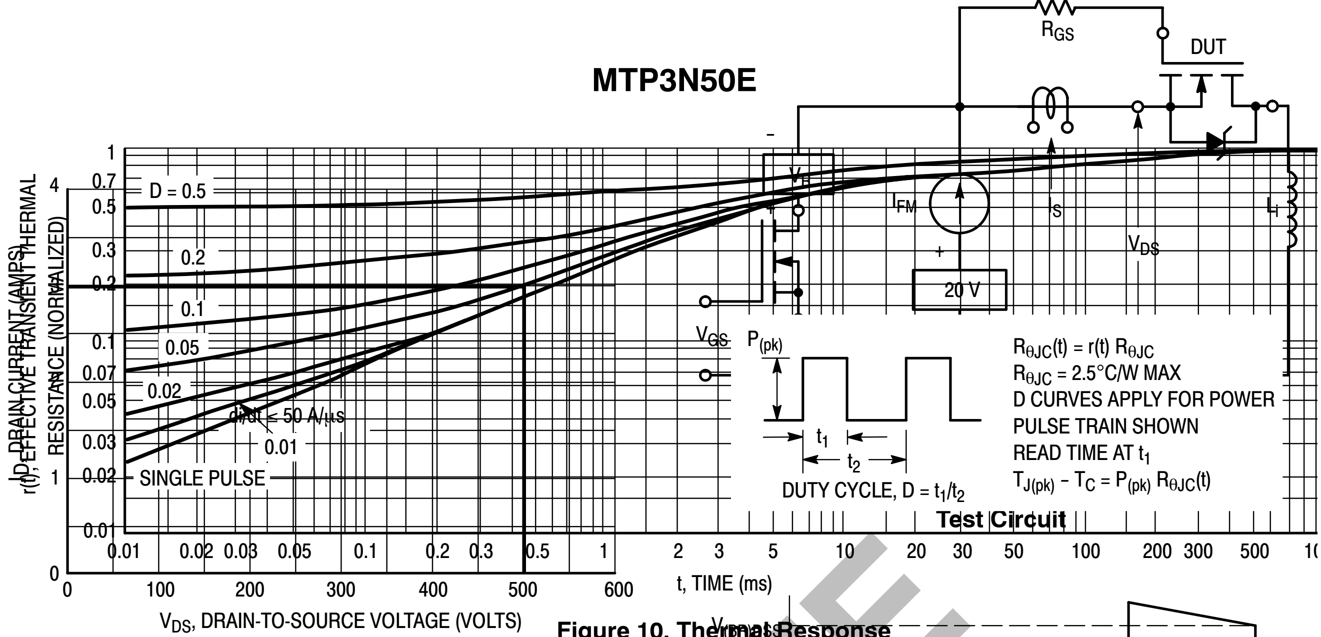


Figure 9. Resistive Switching Time Variation versus Gate Resistance



Test Circuit

Figure 10. Thermal Response

Figure 12. Commutating Safe Operating Area (CSOA)

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

Figure 14. Unclamped Inductive Switching Test Circuit

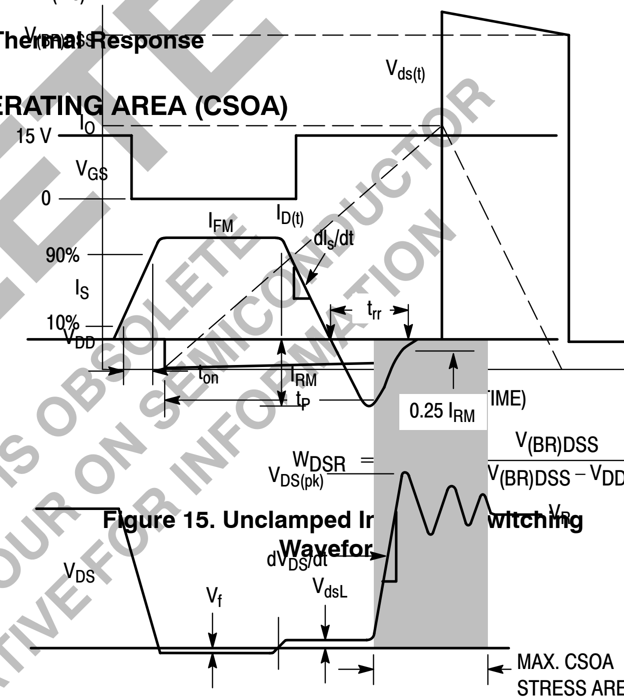


Figure 15. Unclamped Inductive Switching Waveforms

Figure 11. Commutating Waveforms

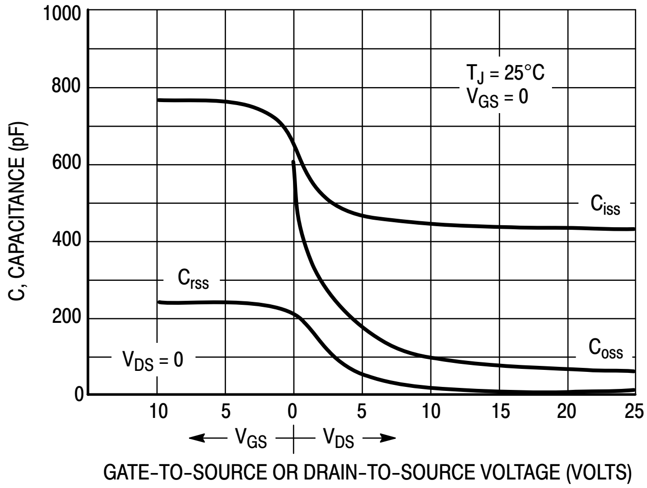


Figure 16. Capacitance Variation

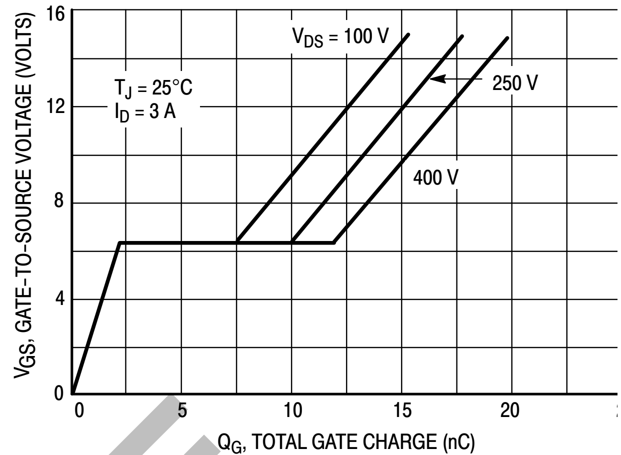
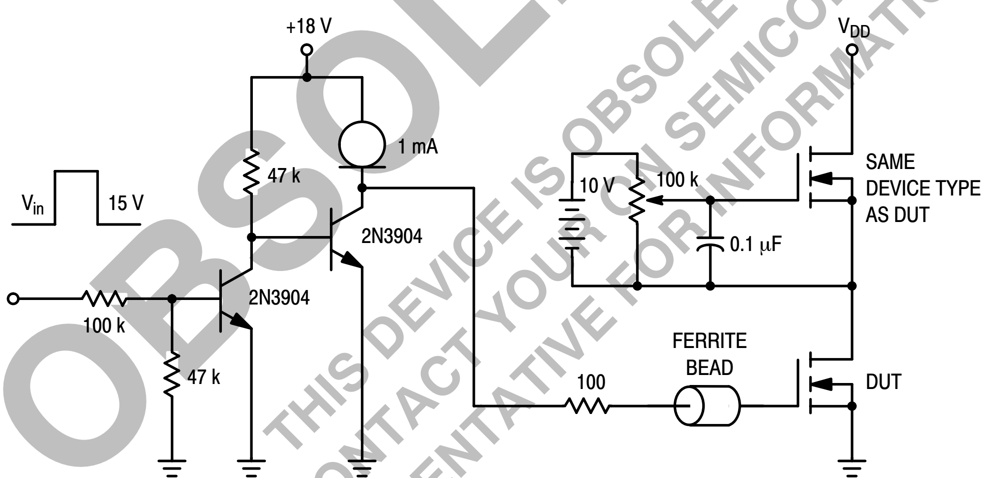


Figure 17. Gate Charge versus Gate-To-Source Voltage

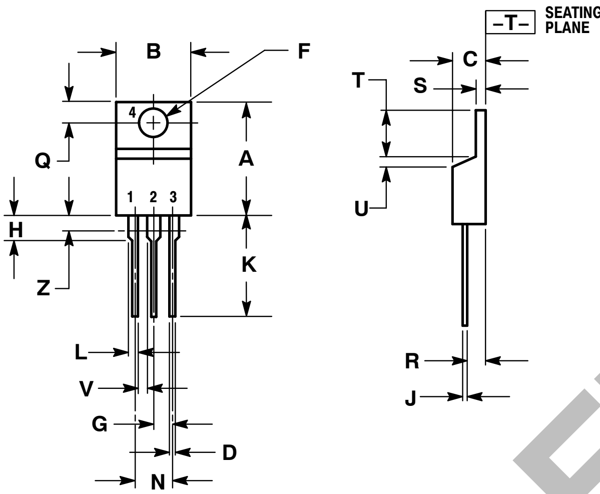


V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

PACKAGE DIMENSIONS

CASE 221A−06 ISSUE Y



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

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