

Vishay Semiconductors

Schottky Rectifier, 2 x 3 A



PRODUCT SUMMARY							
Package	D-PAK (TO-252AA)						
I _{F(AV)}	2 x 3 A						
V _R	50 V, 60 V						
V_F at I_F	0.65 V						
I _{RM}	15 mA at 125 °C						
T _J max.	150 °C						
Diode variation	Common cathode						
E _{AS}	6 mJ						

FEATURES

- Popular D-PAK outline
- Center tap configuration
- Small foot print, surface mountable
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Compliant to RoHS Directive 2002/95/EC
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C

DESCRIPTION

The VS-MBRD650CTPbF, VS-MBRD660CTPbF surface mount, center tap, Schottky rectifier series has been designed for applications requiring low forward drop and small foot prints on PC boards. Typical applications are in disk drives, switching power supplies, converters, freewheeling diodes, battery charging, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS									
SYMBOL	CHARACTERISTICS	VALUES	UNITS A V A V						
I _{F(AV)}	Rectangular waveform	6	А						
V _{RRM}		50/60	V						
I _{FSM}	t _p = 5 μs sine	490	А						
V _F	3 Apk, T _J = 125 °C (per leg)	0.65	V						
TJ	Range	- 40 to 150	۵°						

VOLTAGE RATINGS									
PARAMETER	SYMBOL	VS-MBRD650CTPbF	VS-MBRD660CTPbF	UNITS					
Maximum DC reverse voltage	V _R	50	60	V					
Maximum working peak reverse voltage	V _{RWM}	50	00	v					

ABSOLUTE MAXIMUM RATINGS									
PARAMETER		SYMBOL	TEST CONDIT	VALUES	UNITS				
Maximum average per leg		Iran	50% duty cycle at T ₂ = 128 °C, rectangular waveform		3.0				
See fig. 5	per device	IF(AV)	30% duty cycle at $10^{\circ} = 120\%$ 0, re	6	A				
Maximum peak one cycle non-repetitive surge current See fig. 7		less s	5 µs sine or 3 µs rect. pulse	Following any rated load		490			
		IFSM	10 ms sine or 6 ms rect. pulse	V_{RRM} applied		75			
Non-repetitive avalanche energy per leg		E _{AS}	T _J = 25 °C, I _{AS} = 1 A, L = 12 mH		6	mJ			
Repetitive avalanche current per leg		I _{AR}	Current decaying linearly to zero in 1 μ s Frequency limited by T _J maximum V _A = 1.5 x V _R typical		0.6	А			

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ELECTRICAL SPECIFICATIONS									
PARAMETER	SYMBOL	TEST CO	TEST CONDITIONS						
		3 A	T 25 °C	0.7					
Maximum forward voltage drop per leg	V (1)	6 A	1j=23 0	0.9	v				
See fig. 1	VFM (1)	3 A	T - 125 °C	0.65					
		6 A	1j = 125 C	0.85					
Maximum reverse leakage current per leg	I _{RM} ⁽¹⁾	$T_J = 25 \ ^\circ C$	V Patod V-	0.1	mA				
See fig. 2		T _J = 125 °C	VR - naleu VR	15					
Typical junction capacitance per leg	CT	$V_R = 5 V_{DC}$ (test signal range	ge 100 kHz to 1 MHz), 25 °C	145	pF				
Typical series inductance per leg	L _S	Measured lead to lead 5 r	5.0	nH					
Maximum voltage rate of change	dV/dt	Rated V _R	10 000	V/µs					

Note

 $^{(1)}\,$ Pulse width < 300 $\mu s,$ duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS								
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS			
Maximum junction and storage temperature range		T _J ⁽¹⁾ , T _{Stg}		- 40 to 150	°C			
Maximum thermal resistance,	per leg	P	DC operation	6				
junction to case	per device	H _{thJC}	See fig. 4	3	°C/W			
Maximum thermal resistance, junction to ambient		R _{thJA}		80	0,11			
Approximate weight				0.3	g			
				0.01	oz.			
Marking device			Case style D PAK (similar to TO 252AA)	MBRD650CT				
			Case style D-FAR (Similar 10 TO-232AA)	MBRD660CT				

Note

(1) $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$ thermal runaway condition for a diode on its own heatsink



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Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)



Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics (Per Leg)

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Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)

Note

- Formula used: $T_C = T_J (Pd + Pd_{REV}) \times R_{thJC}$; (1)
 - $\begin{array}{l} \mathsf{Pd} = \mathsf{Forward} \ \mathsf{power} \ \mathsf{loss} = \mathsf{I}_{\mathsf{F}(\mathsf{AV})} \times \mathsf{V}_{\mathsf{FM}} \ \mathsf{at} \ (\mathsf{I}_{\mathsf{F}(\mathsf{AV})}/\mathsf{D}) \ (\mathsf{see fig. 6}); \\ \mathsf{Pd}_{\mathsf{REV}} = \mathsf{Inverse} \ \mathsf{power} \ \mathsf{loss} = \mathsf{V}_{\mathsf{R1}} \times \mathsf{I}_{\mathsf{R}} \ (\mathsf{1} \mathsf{D}); \ \mathsf{I}_{\mathsf{R}} \ \mathsf{at} \ \mathsf{V}_{\mathsf{R1}} = \mathsf{80} \ \% \ \mathsf{rated} \ \mathsf{V}_{\mathsf{R}} \end{array}$



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ORDERING INFORMATION TABLE



LINKS TO RELATED DOCUMENTS							
Dimensions	www.vishay.com/doc?95016						
Part marking information	www.vishay.com/doc?95059						
Packaging information	www.vishay.com/doc?95033						





D-PAK (TO-252AA)

DIMENSIONS in millimeters and inches



SYMBOL	MILLIN	IETERS	INC	HES	NOTES		SYMPOL	MILLIN	IETERS	INC	HES	NOTES
	MIN. MAX. MIN. MAX.		STMDUL	MIN.	MAX.	MIN.	MAX.	NULES				
А	2.18	2.39	0.086	0.094			е	2.29	BSC	0.090) BSC	
A1	-	0.13	-	0.005			Н	9.40	10.41	0.370	0.410	
b	0.64	0.89	0.025	0.035			L	1.40	1.78	0.055	0.070	
b2	0.76	1.14	0.030	0.045			L1	2.74	BSC	0.108	BREF.	
b3	4.95	5.46	0.195	0.215	3		L2	0.51	BSC	0.020	BSC	
С	0.46	0.61	0.018	0.024			L3	0.89	1.27	0.035	0.050	3
c2	0.46	0.89	0.018	0.035			L4	-	1.02	-	0.040	
D	5.97	6.22	0.235	0.245	5		L5	1.14	1.52	0.045	0.060	2
D1	5.21	-	0.205	-	3		Ø	0°	10°	0°	10°	
E	6.35	6.73	0.250	0.265	5]	Ø1	0°	15°	0°	15°	
E1	4.32	-	0.170	-	3		Ø2	25°	35°	25°	35°	

Notes

⁽¹⁾ Dimensioning and tolerancing as per ASME Y14.5M-1994

(2) Lead dimension uncontrolled in L5

⁽³⁾ Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad

(4) Section C - C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip

(5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

⁽⁶⁾ Dimension b1 and c1 applied to base metal only

⁽⁷⁾ Datum A and B to be determined at datum plane H

⁽⁸⁾ Outline conforms to JEDEC outline TO-252AA

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