FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13731-3E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90895 Series

MB90F897/F897S/MB90V495G

■ DESCRIPTION

MB90895 series devices are 16-bit micro general-purpose controllers designed for applications which need high-speed real-time processing. The devices of this series are high-performance 16-bit CPU micro controllers employing of the dual operation flash memory and CAN controller on LQFP-48 small package.

The system, inheriting the architecture of F²MC* family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).

The peripheral resources of MB90895 series include the following:

8/10-bit A/D converter, UART0/UART1 (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

*: "F²MC", an abbreviation for FUJITSU Flexible Microcontroller, is a registered trademark of FUJITSU Ltd.

■ FEATURES

- **Models that support +125°C**
- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).
  - Operation by sub-clock (8.192 kHz) is allowed. (MB90F897)
  - Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).
- **16 Mbyte CPU memory space**
  - 24-bit internal addressing

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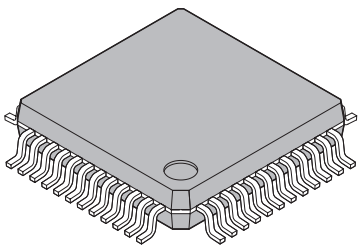
■ PACKAGE

48-pin plastic, LQFP



(FPT-48P-M26)

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- **Instruction system best suited to controller**
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced multiply-divide instructions and RETI instructions
  - Enhanced high-precision computing with 32-bit accumulator
- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Enhanced various pointer indirect instructions
  - Barrel shift instructions
- **Increased processing speed**
  - 4-byte instruction queue
- **Powerful interrupt function with 8 levels and 34 factors**
- **Automatic data transfer function independent of CPU**
  - Expanded intelligent I/O service function (EI^2 OS): Maximum of 16 channels
- **Low power consumption (standby) mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and clock timer only)
  - Clock mode (a mode that operates sub clock and clock timer only)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU blocking operation mode
- **Process**
  - CMOS technology
- **I/O port**
  - General-purpose input/output port (CMOS output) :
    MB90F897 : 34 ports (including 4 high-current output ports)
    MB90F897S : 36 ports (including 4 high-current output ports)
- **Timer**
  - Time-base timer, clock timer, watchdog timer: 1 channel
  - 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels
  - 16-bit reload timer: 2 channels
  - 16-bit input/output timer
    - 16-bit free run timer: 1 channel
    - 16-bit input capture: (ICU): 4 channels

    Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.
- **CAN controller: 1 channel**
  - Compliant with Ver 2.0A and Ver 2.0B CAN specifications
  - 8 built-in message buffers
  - Transmission rate of 10 Kbps to 1 Mbps (by 16 MHz machine clock)
  - CAN wake-up
- **UART0 (SCI), UART1(SCI): 2 channel**
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available.
- **DTP/External interrupt: 4 channels, CAN wake-up: 1channel**
  - Module for activation of expanded intelligent I/O service (EI^2OS), and generation of external interrupt.
- **Delay interrupt generator module**
  - Generates interrupt request for task switching.
- **8/10-bit A/D converter: 8 channels**
  - Resolution is selectable between 8-bit and 10-bit.
  - Activation by external trigger input is allowed.
  - Conversion time: 6.125 µs (at 16-MHz machine clock, including sampling time)
- **Program patch function**
  - Address matching detection for 2 address pointers.

■ PRODUCT LINEUP

Parameter \ Part Number		MB90F897/S	MB90V495G
Classification		Flash ROM	Evaluation product
ROM capacity		64 Kbytes	—
RAM capacity		2 Kbytes	6 Kbytes
Process		CMOS	
Package		LQFP-48 (0.50 mm width)	PGA256
Operating power supply voltage		3.5 V to 5.5 V	4.5 V to 5.5 V
Special power supply for emulator*1		—	None
CPU functions		Number of basic instructions : 351 instructions Instruction bit length : 8 bits and 16 bits Instruction length : 1 byte to 7 bytes Data bit length : 1 bit, 8 bits, 16 bits	
		Minimum instruction execution time : 62.5 ns (at 16-MHz machine clock)	
		Interrupt processing time : 1.5 µs at minimum (at 16-MHz machine clock)	
Low power consumption (standby) mode		Sleep mode/Clock mode/Time-base timer mode/ Stop mode/CPU intermittent	
I/O port		General-purpose input/output ports (CMOS output) : 34 ports (36 ports*2) including 4 high-current output ports (P14 to P17)	
Time-base timer		18-bit free-run counter Interrupt cycle : 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms (with oscillation clock frequency at 4 MHz)	
Watchdog timer		Reset generation cycle: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (with oscillation clock frequency at 4 MHz)	
16-bit input/output timer	16-bit free-run timer	Number of channels: 1 Interrupt upon occurrence of overflow	
	Input capture	Number of channels: 4 Retaining free-run timer value set by pin input (rising edge, falling edge, and both edges)	
16-bit reload timer		Number of channels: 2 16-bit reload timer operation Count clock cycle: 0.25 µs, 0.5 µs, 2.0 µs (at 16-MHz machine clock frequency) External event count is allowed.	
Clock timer		15-bit free-run counter Interrupt cycle: 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s (with 8.192 kHz sub clock)	
8/16-bit PPG timer		Number of channels: 2 (four 8-bit channels are available also.) PPG operation is allowed with four 8-bit channels or one 16-bit channel. Outputting pulse wave of arbitrary cycle or arbitrary duty is allowed. Count clock: 62.5 ns to 1 µs (with 16 MHz machine clock)	
Delay interrupt generator module		Interrupt generator module for task switching. Used for real-time OS.	
DTP/External interrupt		Number of inputs: 4 Activated by rising edge, falling edge, "H" level or "L" level input. External interrupt or expanded intelligent I/O service (EI^{2}OS) is available.	

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Parameter \ Part Number	MB90F897/S	MB90V495G
8/10-bit A/D converter	Number of channels: 8 Resolution: Selectable 10-bit or 8-bit. Conversion time: 6.125 µs (at 16-MHz machine clock, including sampling time) Sequential conversion of two or more successive channels is allowed. (Setting a maximum of 8 channels is allowed.) Single conversion mode : Selected channel is converted only once. Sequential conversion mode: Selected channel is converted repetitively. Halt conversion mode : Conversion of selected channel is stopped and activated alternately.	
UART0 (SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 Kbps to 2 Mbps Clock-asynchronous transfer: 1,202 bps to 62,500 bps Communication is allowed by bi-directional serial communication function and master/slave type connection.	
UART1 (SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 Kbps to 2 Mbps Clock-asynchronous transfer: 9,615 bps to 500 Kbps Communication is allowed by bi-directional serial communication function and master/slave type connection.	
CAN	Compliant with Ver 2.0A and Ver 2.0B CAN specifications. 8 built-in message buffers. Transmission rate of 10 Kbps to 1 Mbps (by 16 MHz machine clock) CAN wake-up	

*1 : Settings of DIP switch S2 for using emulation pod MB2145-507. For details, see MB2145-507 Hardware Manual (2.7 Power Pin solely for Emulator).

*2 : MB90F897S

■ PACKAGES AND PRODUCT MODELS

Package	MB90F897/S
FPT-48P-M26	○

○ : Yes, × : No

Note : Refer to "■ PACKAGE DIMENSION" for details of the package.

■ PRODUCT COMPARISON

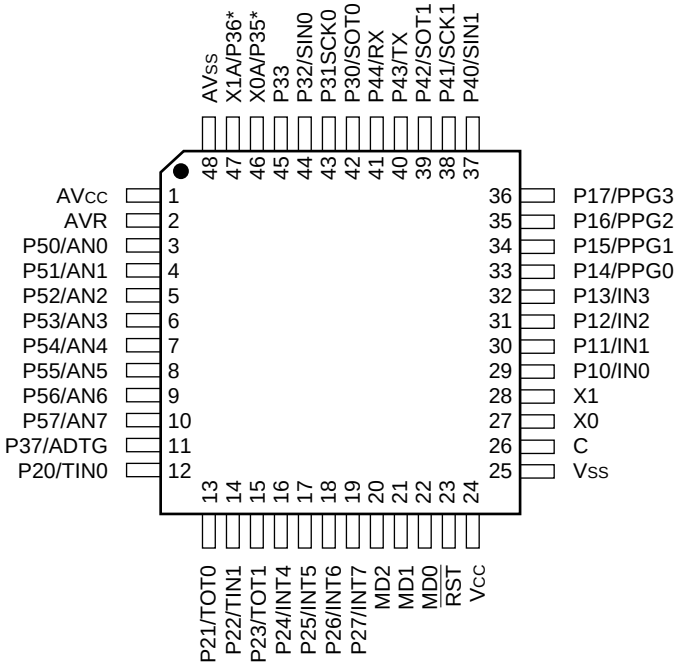
Memory space

When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

- The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.
- On MB90V495G, an image from FF4000$_H$ to FFFFFF$_H$ is viewed on 00 bank and an image of FE0000$_H$ to FF3FFF$_H$ is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)
- On MB90F897/S, an image from FF4000$_H$ to FFFFFF$_H$ is viewed on 00 bank and an image of FF0000$_H$ to FF3FFF$_H$ is viewed only on FF bank.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-48P-M26)

* : MB90F897 : X1A, X0A
MB90F897S : P36, P35

■ PIN DESCRIPTION

Pin No.	Pin name	Circuit type	Function
1	AVcc	—	Vcc power input pin for A/D converter.
2	AVR	—	Power (Vref+) input pin for A/D converter. Use as input for Vcc or lower.
3 to 10	P50 to P57	E	General-purpose input/output ports.
	AN0 to AN7		Functions as analog input pin for A/D converter. Valid when analog input setting is “enabled.”
11	P37	D	General-purpose input/output ports.
	ADTG		Function as an external trigger input pin for A/D converter. Use the pin by setting as input port.
12	P20	D	General-purpose input/output ports.
	TIN0		Function as an event input pin for reload timer 0. Use the pin by setting as input port.
13	P21	D	General-purpose input/output ports.
	TOT0		Function as an event output pin for reload timer 0. Valid only when output setting is “enabled.”
14	P22	D	General-purpose input/output ports.
	TIN1		Function as an event input pin for reload timer 1. Use the pin by setting as input port.
15	P23	D	General-purpose input/output ports.
	TOT1		Function as an event output pin for reload timer 1. Valid only when output setting is “enabled.”
16 to 19	P24 to P27	D	General-purpose input/output ports.
	INT4 to INT7		Functions as external interrupt input pin. Use the pin by setting as input port.
20	MD2	F	Input pin for specifying operation mode. Connect directly to Vss.
21	MD1	C	Input pin for specifying operation mode. Connect directly to Vcc.
22	MD0	C	Input pin for specifying operation mode. Connect directly to Vcc.
23	$\overline{\text{RST}}$	B	External reset input pin.
24	Vcc	—	Power source (5 V) input pin.
25	Vss	—	Power source (0 V) input pin.
26	C	—	Capacitor pin for stabilizing power source. Connect a ceramic capacitor of approximately 0.1 μF.
27	X0	A	Pin for high-rate oscillation.
28	X1	A	Pin for high-rate oscillation.
29 to 32	P10 to P13	D	General-purpose input/output ports.
	IN0 to IN3		Functions as trigger input pins of input capture channels 0 to 3. Use the pins by setting as input ports.

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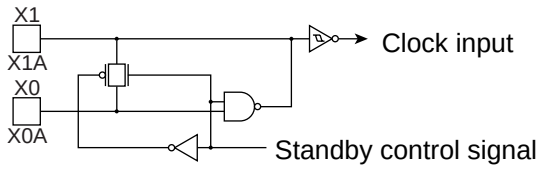
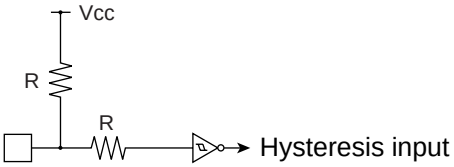
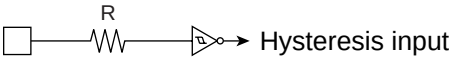
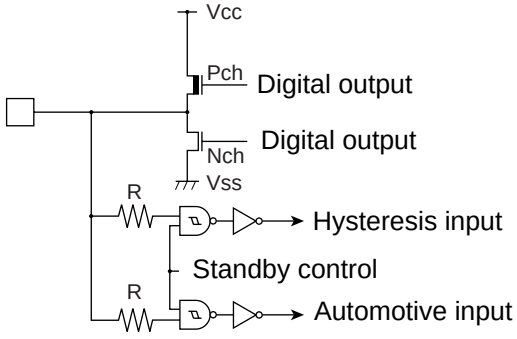
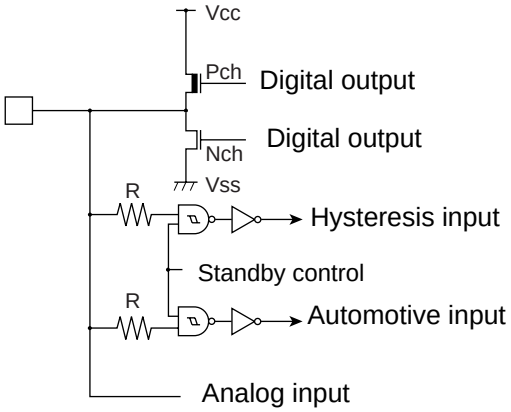
Pin No.	Pin name	Circuit type	Function
33 to 36	P14 to P17	G	General-purpose input/output ports. High-current output ports.
	PPG0 to PPG3		Functions as output pin of PPG timers 01 and 23. Valid when output setting is “enabled.”
37	P40	D	General-purpose input/output port.
	SIN1		Serial data input pin for UART1. Use the pin by setting as input port.
38	P41	D	General-purpose input/output port.
	SCK1		Serial clock input pin for UART1. Valid only when serial clock input/output setting on UART1 is “enabled.”
39	P42	D	General-purpose input/output port.
	SOT1		Serial data input pin for UART1. Valid only when serial data input/output setting on UART1 is “enabled.”
40	P43	D	General-purpose input/output port.
	TX		Transmission output pin for CAN. Valid only when output setting is “enabled.”
41	P44	D	General-purpose input/output port.
	RX		Transmission output pin for CAN. Valid only when output setting is “enabled.”
42	P30	D	General-purpose input/output port.
	SOT0		Serial data output pin for UART0. Valid only when serial data output setting on UART0 is “enabled.”
43	P31	D	General-purpose input/output port.
	SCK0		Serial clock input pin for UART0. Valid only when serial clock input/output setting on UART0 is “enabled.”
44	P32	H	General-purpose input/output port.
	SIN0		Serial data input pin for UART0. Valid only when output setting is “enabled.”
45	P33	D	General-purpose input/output port.
46	X0A*	A	Pin for low-rate oscillation.
	P35*		General-purpose input/output port.
47	X1A*	A	Pin for low-rate oscillation.
	P36*		General-purpose input/output port.
48	AVss	—	Vss power source input pin for A/D converter.

* : MB90F897 : X1A, X0A
MB90F897S : P36, P35

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• High-rate oscillation feedback resistor, approx. 1 MΩ • Low-rate oscillation feedback resistor, approx. 10 MΩ
B		• Hysteresis input with pull-up resistor. • Pull-up resistor, approx. 50 kΩ
C		• Hysteresis input
D		• CMOS hysteresis input • CMOS level output • Standby control provided • Automotive input
E		• CMOS hysteresis input • CMOS level output • Shared for analog input pin • Standby control provided • Automotive input

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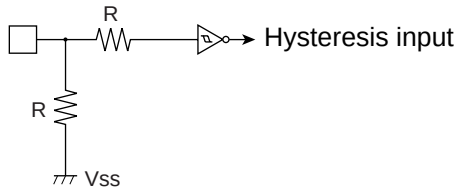
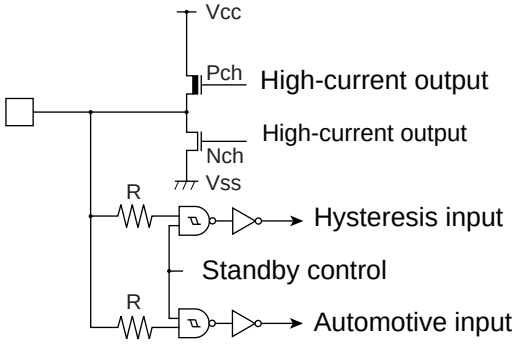
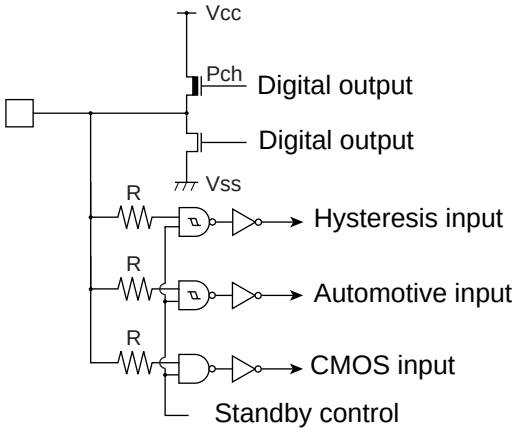
Type	Circuit	Remarks
F		• Hysteresis input with pull-down resistor • Pull-down resistor, approx. 50 kΩ • FLASH product is not provided with pull-down resistor.
G		• CMOS hysteresis input • CMOS level output (high-current output) • Standby control provided • Automotive input
H		• CMOS hysteresis input • CMOS level output • Standby control provided • CMOS input • Automotive input

■ HANDLING DEVICES

• Do Not Exceed Maximum Rating (preventing “latch up”)

- On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc and Vss.
- Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.
- When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

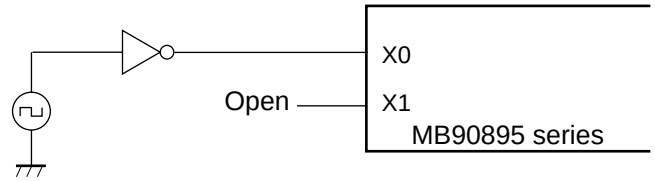
• Handling Unused Pins

- Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused input pins open under output status, or process as input pins if they are under input status.

• Using External Clock

- When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

• Using external clock



• Notes When Using No Sub Clock on MB90F897

- If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

• About Power Supply Pins

- If two or more Vcc and Vss exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.
- Pay attention to connect a power supply to Vcc and Vss of MB90895 series device in a lowest-possible impedance.
- Near pins of MB90895 series device, connecting a bypass capacitor is recommended at 0.1 µF across Vcc and Vss.

• Crystal Oscillator Circuit

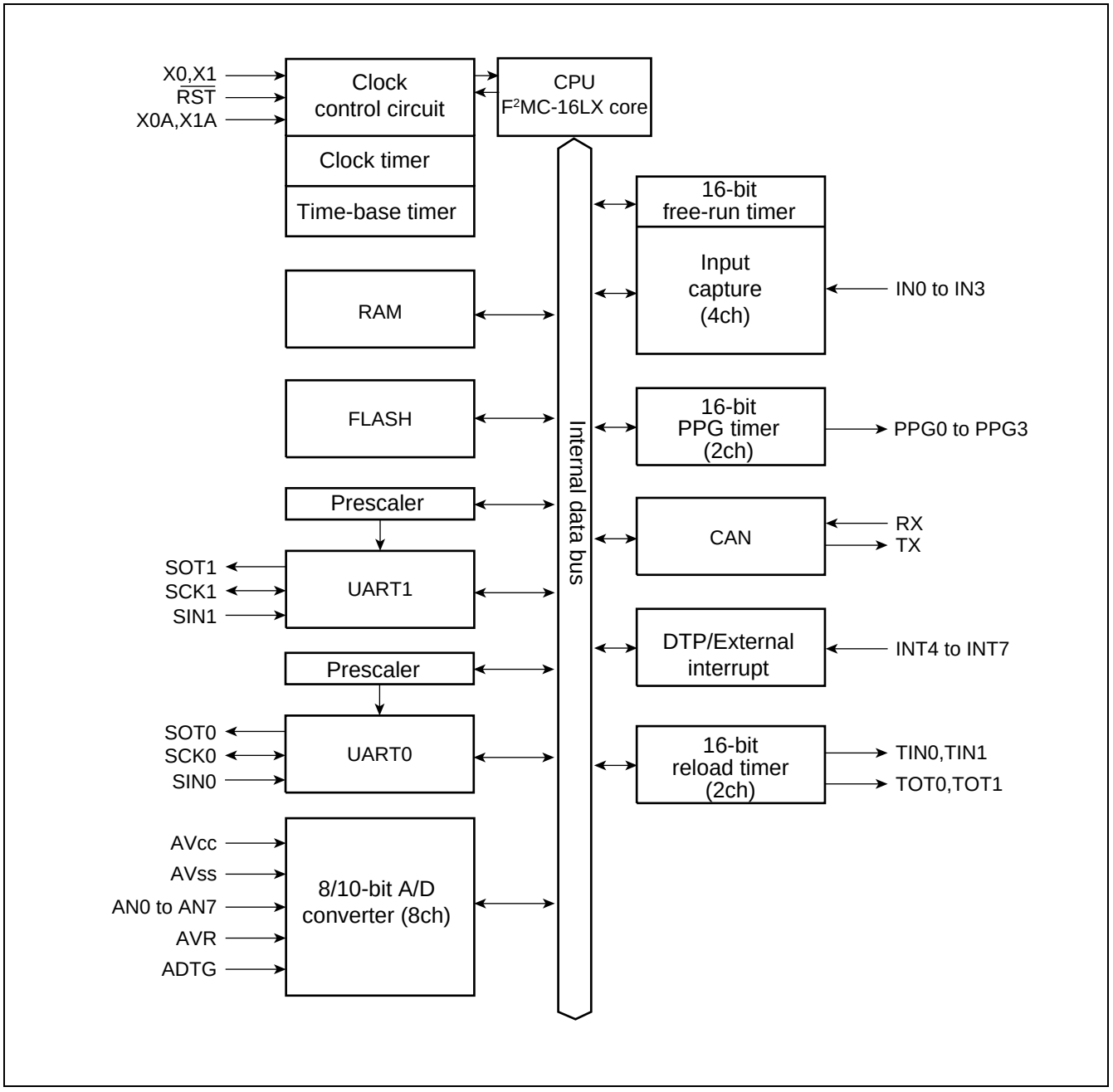
- Noises around X0 and X1 pins cause malfunctions on a MB90895 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.
- Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

• Caution on Operations during PLL Clock Mode

- If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

- **Sequence of Turning on Power of A/D Converter and Applying Analog Input**
  - Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).
  - Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.
  - Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)
- **Handling Pins When A/D Converter is Not Used**
  - If the A/D converter is not used, connect the pins under the following conditions: “AVcc=AVR=Vcc,” and “AVss=Vss”
- **Note on Turning on Power**
  - For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μs of voltage rising time (between 0.2 V and 2.7 V) when turning on the power.
- **Stabilization of supply voltage**
  - A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.
    For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.
- **Support for +125°C**
  - Users considering application exceeding T_A = +105°C are advised to contact their FUJITSU representatives beforehand for reliability limitations for reliability limitations.

■ BLOCK DIAGRAM



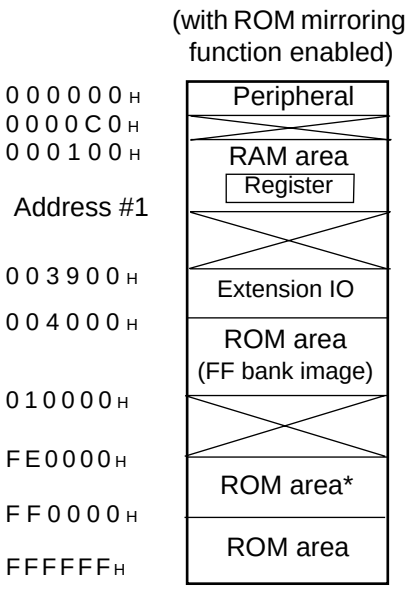
■ MEMORY MAP

MB90895 series allows specifying a memory access mode “single chip mode.”

1. Memory allocation of MB90895

MB90895 series model has 24-bit wide internal address bus and up to 24-bit bus of external address bus. A maximum of 16 Mbyte memory space of external access memory is accessible.

2. Memory map



Model	Address #1
MB90V495G	001900H
MB90F897/S	000900H

: Internal access memory

: Access disallowed

* : On MB90F897/S, to read “FE0000H” to “FEFFFFH” is to read out “FF0000H” to “FFFFFFH”.

Note : When internal ROM is operating, F²MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called “mirroring ROM,” which allows effective use of C compiler small model. F²MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying “far” using pointer.
For example, when accessing to “00C000H”, ROM data at “FFC000H” is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of “FF4000H” to “FFFFFFH” is viewed on “004000H” to “00FFFFH” image, store a ROM data table in area “FF4000H” to “FFFFFFH.”

■ I/O MAP

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
000000H	(Reserved area) *				
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H to 000010H	(Reserved area) *				
000011H	DDR1	Port 1 direction data register	R/W	Port 1	00000000B
000012H	DDR2	Port 2 direction data register	R/W	Port 2	00000000B
000013H	DDR3	Port 3 direction data register	R/W	Port 3	000X0000B
000014H	DDR4	Port 4 direction data register	R/W	Port 4	XXX00000B
000015H	DDR5	Port 5 direction data register	R/W	Port 5	00000000B
000016H to 00001AH	(Reserved area) *				
00001BH	ADER	Analog input permission register	R/W	8/10-bit A/D converter	11111111B
00001CH to 00001FH	(Reserved area) *				
000020H	SMR0	Serial mode register 0	R/W	UART0	00000000B
000021H	SCR0	Serial control register 0	R/W, W		00000100B
000022H	SIDR0/ SODR0	Serial input data register 0/ Serial output data register 0	R, W		XXXXXXXXB
000023H	SSR0	Serial status register 0	R, R/W		00001X00B
000024H	CDCR0	Communication prescaler control register 0	R/W		0XXX1111B
000025H	SES0	Serial edge selection register 0	R/W		XXXXXXX0B
000026H	SMR1	Serial mode register 1	R/W	UART1	00000000B
000027H	SCR1	Serial control register 1	R/W, W		00000100B
000028H	SIDR1/ SODR1	Serial input data register 1/ Serial output data register 1	R, W		XXXXXXXXB
000029H	SSR1	Serial status data register 1	R, R/W		00001000B
00002AH	(Reserved area) *				
00002BH	CDCR1	Communication prescaler control register 1	R/W	UART1	0XXX0000B

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Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
00002C$_H$ to 00002F$_H$	(Reserved area) *				
000030$_H$	ENIR	DTP/External interrupt permission register	R/W	DTP/External interrupt	00000000$_B$
000031$_H$	EIRR	DTP/External interrupt permission register	R/W		XXXXXXXX$_B$
000032$_H$	ELVR	Detection level setting register	R/W		00000000$_B$
000033$_H$			R/W		00000000$_B$
000034$_H$	ADCS	A/D control status register	R/W	8/10-bit A/D converter	00000000$_B$
000035$_H$			R/W, W		00000000$_B$
000036$_H$	ADCR	A/D data register	W, R		XXXXXXXX$_B$
000037$_H$			R		00101XXX$_B$
000038$_H$ to 00003E$_H$	(Reserved area) *				
00003F$_H$	PSCCR	PLL/Subclock control register	R/W, W	Clock	XXXX0000$_B$
000040$_H$	PPGC0	PPG0 operation mode control register	R/W, W	8/16-bit PPG timer 0/1	0X000XX1$_B$
000041$_H$	PPGC1	PPG1 operation mode control register	R/W, W		0X000001$_B$
000042$_H$	PPG01	PPG0/1 count clock selection register	R/W		000000XX$_B$
000043$_H$	(Reserved area) *				
000044$_H$	PPGC2	PPG2 operation mode control register	R/W, W	8/16-bit PPG timer 2/3	0X000XX1$_B$
000045$_H$	PPGC3	PPG3 operation mode control register	R/W, W		0X000001$_B$
000046$_H$	PPG23	PPG2/3 count clock selection register	R/W		000000XX$_B$
000047$_H$ to 00004F$_H$	(Reserved area) *				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
000050H	IPCP0	Input capture data register 0	R	16-bit input/output timer	XXXXXXXXB
000051H					XXXXXXXXB
000052H	IPCP1	Input capture data register 1	R		XXXXXXXXB
000053H					XXXXXXXXB
000054H	ICS01	Input capture control status register	R/W		00000000B
000055H	ICS23				00000000B
000056H	TCDT	Timer counter data register	R/W		00000000B
000057H					00000000B
000058H	TCCS	Timer counter control status register	R/W		00000000B
000059H	(Reserved area) *				
00005AH	IPCP2	Input capture data register 2	R	16-bit input/output timer	XXXXXXXXB
00005BH					XXXXXXXXB
00005CH	IPCP3	Input capture data register 3	R		XXXXXXXXB
00005DH					XXXXXXXXB
00005EH to 000065H	(Reserved area) *				
000066H	TMCSR0	Timer control status register	R/W	16-bit reload timer 0	00000000B
000067H			R/W		XXXX0000B
000068H	TMCSR1		R/W	16-bit reload timer 1	00000000B
000069H			R/W		XXXX0000B
00006AH to 00006EH	(Reserved area) *				
00006FH	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	XXXXXXX1B
000070H to 00007FH	(Reserved area) *				
000080H	BVALR	Message buffer enabling register	R/W	CAN controller	00000000B
000081H	(Reserved area) *				
000082H	TREQR	Send request register	R/W	CAN controller	00000000B
000083H	(Reserved area) *				
000084H	TCANR	Send cancel register	W	CAN controller	00000000B
000085H	(Reserved area) *				
000086H	TCR	Send completion register	R/W	CAN controller	00000000B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
000087H	(Reserved area) *				
000088H	RCR	Receive completion register	R/W	CAN controller	00000000B
000089H	(Reserved area) *				
00008AH	RRTRR	Receive RTR register	R/W	CAN controller	00000000B
00008BH	(Reserved area) *				
00008CH	ROVRR	Receive overrun register	R/W	CAN controller	00000000B
00008DH	(Reserved area) *				
00008EH	RIER	Receive completion interrupt permission register	R/W	CAN controller	00000000B
00008FH to 00009DH	(Reserved area) *				
00009EH	PACSR	Address detection control register	R/W	Address matching detection function	00000000B
00009FH	DIRR	Delay interrupt request generation/ release register	R/W	Delay interrupt generation module	XXXXXXX0B
0000A0H	LPMCR	Lower power consumption mode control register	W,R/W	Lower power consumption mode	00011000B
0000A1H	CKSCR	Clock selection register	R,R/W	Clock	11111100B
0000A2H	PILR	Port input level selection register	R/W	I/O	0000000XB
0000A3H to 0000A7H	(Reserved area) *				
0000A8H	WDTC	Watchdog timer control register	R,W	Watchdog timer	XXXXX111B
0000A9H	TBTC	Time-base timer control register	R/W,W	Time-base timer	1XX00100B
0000AAH	WTC	Clock timer control register	R,R/W	Clock timer	1X001000B
0000ABH to 0000ADH	(Reserved area) *				
0000AEH	FMCS	Flash memory control status register	R,W,R/W	512K-bit flash memory	000X0000B
0000AFH	(Reserved area) *				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
0000B0H	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111B
0000B1H	ICR01	Interrupt control register 01			00000111B
0000B2H	ICR02	Interrupt control register 02			00000111B
0000B3H	ICR03	Interrupt control register 03			00000111B
0000B4H	ICR04	Interrupt control register 04			00000111B
0000B5H	ICR05	Interrupt control register 05			00000111B
0000B6H	ICR06	Interrupt control register 06			00000111B
0000B7H	ICR07	Interrupt control register 07			00000111B
0000B8H	ICR08	Interrupt control register 08			00000111B
0000B9H	ICR09	Interrupt control register 09			00000111B
0000BAH	ICR10	Interrupt control register 10			00000111B
0000BBH	ICR11	Interrupt control register 11			00000111B
0000BCH	ICR12	Interrupt control register 12			00000111B
0000BDH	ICR13	Interrupt control register 13			00000111B
0000BEH	ICR14	Interrupt control register 14			00000111B
0000BFH	ICR15	Interrupt control register 15			00000111B
0000C0H to 0000FFH	(Reserved area) *				
001FF0H	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	XXXXXXXXB
001FF1H		Detection address setting register 0 (middle-order)			XXXXXXXXB
001FF2H		Detection address setting register 0 (high-order)			XXXXXXXXB
001FF3H	PADR1	Detection address setting register 1 (low-order)	R/W		XXXXXXXXB
001FF4H		Detection address setting register 1 (middle-order)			XXXXXXXXB
001FF5H		Detection address setting register 1 (high-order)			XXXXXXXXB
003900H	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register	R,W	16-bit reload timer 0	XXXXXXXXB
003901H					XXXXXXXXB
003902H	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register	R,W	16-bit reload timer 1	XXXXXXXXB
003903H					XXXXXXXXB
003904H to 003909H	(Reserved area) *				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
00390A$_H$	FWR0	FLASH programing control register 0	R/W	Dual operation FLASH	00000000$_B$
00390B$_H$	FWR1	FLASH programing control register 1	R/W		00000000$_B$
00390C$_H$	SSR0	Sector conversion set register	R/W		00XXXXX0$_B$
00390D$_H$ to 00390F$_H$	(Reserved area) *				
003910$_H$	PRLL0	PPG0 reload register L	R/W	8/16-bit PPG timer	XXXXXXXX$_B$
003911$_H$	PRLH0	PPG0 reload register H	R/W		XXXXXXXX$_B$
003912$_H$	PRLL1	PPG1 reload register L	R/W		XXXXXXXX$_B$
003913$_H$	PRLH1	PPG1 reload register H	R/W		XXXXXXXX$_B$
003914$_H$	PRLL2	PPG2 reload register L	R/W		XXXXXXXX$_B$
003915$_H$	PRLH2	PPG2 reload register H	R/W		XXXXXXXX$_B$
003916$_H$	PRLL3	PPG3 reload register L	R/W		XXXXXXXX$_B$
003917$_H$	PRLH3	PPG3 reload register H	R/W		XXXXXXXX$_B$
003918$_H$ to 00392F$_H$	(Reserved area) *				
003930$_H$ to 003BFF$_H$	(Reserved area) *				
003C00$_H$ to 003C0F$_H$	RAM (General-purpose RAM)				
003C10$_H$ to 003C13$_H$	IDR0	ID register 0	R/W	CAN controller	XXXXXXXX$_B$ to XXXXXXXX$_B$
003C14$_H$ to 003C17$_H$	IDR1	ID register 1	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C18$_H$ to 003C1B$_H$	IDR2	ID register 2	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C1C$_H$ to 003C1F$_H$	IDR3	ID register 3	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C20$_H$ to 003C23$_H$	IDR4	ID register 4	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C24$_H$ to 003C27$_H$	IDR5	ID register 5	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C28$_H$ to 003C2B$_H$	IDR6	ID register 6	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
003C2C$_H$ to 003C2F$_H$	IDR7	ID register 7	R/W	CAN controller	XXXXXXXX$_B$ to XXXXXXXX$_B$
003C30$_H$ 003C31$_H$	DLCR0	DLC register 0	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C32$_H$ 003C33$_H$	DLCR1	DLC register 1	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C34$_H$ 003C35$_H$	DLCR2	DLC register 2	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C36$_H$ 003C37$_H$	DLCR3	DLC register 3	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C38$_H$ 003C39$_H$	DLCR4	DLC register 4	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C3A$_H$ 003C3B$_H$	DLCR5	DLC register 5	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C3C$_H$ 003C3D$_H$	DLCR6	DLC register 6	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C3E$_H$ 003C3F$_H$	DLCR7	DLC register 7	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C40$_H$ to 003C47$_H$	DTR0	Data register 0	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C48$_H$ to 003C4F$_H$	DTR1	Data register 1	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C50$_H$ to 003C57$_H$	DTR2	Data register 2	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C58$_H$ to 003C5F$_H$	DTR3	Data register 3	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C60$_H$ to 003C67$_H$	DTR4	Data register 4	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C68$_H$ to 003C6F$_H$	DTR5	Data register 5	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C70$_H$ to 003C77$_H$	DTR6	Data register 6	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C78$_H$ to 003C7F$_H$	DTR7	Data register 7	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$

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Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
003C80H to 003CFFH	(Reserved area) *				
003D00H 003D01H	CSR	Control status register	R/W, R	CAN controller	0XXXX001B 00XXX000B
003D02H	LEIR	Last event display register	R/W		000XX000B
003D03H	(Reserved area) *				
003D04H 003D05H	RTEC	Send/receive error counter	R	CAN controller	00000000B 00000000B
003D06H 003D07H	BTR	Bit timing register	R/W		11111111B X1111111B
003D08H	IDER	IDE register	R/W		XXXXXXXXB
003D09H	(Reserved area) *				
003D0AH	TRTRR	Send RTR register	R/W		00000000B
003D0BH	(Reserved area) *				
003D0CH	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXXB
003D0DH	(Reserved area) *				
003D0EH	TIER	Send completion interrupt permission register	R/W	CAN controller	00000000B
003D0FH	(Reserved area) *				
003D10H 003D11H	AMSR	Acceptance mask selection register	R/W	CAN controller	XXXXXXXXB XXXXXXXXB
003D12H 003D13H	(Reserved area) *				
003D14H to 003D17H	AMR0	Acceptance mask register 0	R/W	CAN controller	XXXXXXXXB to XXXXXXXXB
003D18H to 003D1BH	AMR1	Acceptance mask register 1	R/W		XXXXXXXXB to XXXXXXXXB
003D1CH to 003DFFH	(Reserved area) *				
003E00H to 003EFFH	(Reserved area) *				
003FF0H to 003FFFH	(Reserved area) *				

Initial values :

0 : Initial value of this bit is “0.”

1 : Initial value of this bit is “1.”

X : Initial value of this bit is undefined.

* : “Reserved area” should not be written anything. Result of reading from “Reserved area” is undefined.

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS readiness	Interrupt vector			Interrupt control register		Priority*3
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT 9 instruction	×	#09	09H	FFFFD8H	—	—	↑
Exceptional treatment	×	#10	0AH	FFFFD4H	—	—	
CAN controller reception completed (RX)	×	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN controller transmission completed (TX) / Node status transition (NS)	×	#12	0CH	FFFFCCH			
Reserved	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
Reserved	×	#14	0EH	FFFFC4H			
CAN wakeup	Δ	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
Time-base timer	×	#16	10H	FFFFBCH			
16-bit reload timer 0	Δ	#17	11H	FFFFB8H	ICR03	0000B3H*1	
8/10-bit A/D converter	Δ	#18	12H	FFFFB4H			
16-bit free-run timer overflow	Δ	#19	13H	FFFFB0H	ICR04	0000B4H*1	
Reserved	×	#20	14H	FFFFACH			
Reserved	×	#21	15H	FFFFA8H	ICR05	0000B5H*2	
PPG timer ch0, ch1 underflow	×	#22	16H	FFFFA4H			
Input capture 0-input	Δ	#23	17H	FFFFA0H	ICR06	0000B6H*1	
External interrupt (INT4/INT5)	Δ	#24	18H	FFFF9CH			
Input capture 1-input	Δ	#25	19H	FFFF98H	ICR07	0000B7H*1	
PPG timer ch2, ch3 underflow	×	#26	1AH	FFFF94H			
External interrupt (INT6/INT7)	Δ	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Clock timer	Δ	#28	1CH	FFFF8CH			
Reserved	×	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Input capture 2-input Input capture 3-input	×	#30	1EH	FFFF84H			
Reserved	×	#31	1FH	FFFF80H	ICR10	0000BAH*1	
Reserved	×	#32	20H	FFFF7CH			
Reserved	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Reserved	×	#34	22H	FFFF74H			
Reserved	×	#35	23H	FFFF70H	ICR12	0000BCH*1	↓
16-bit reload timer 1	○	#36	24H	FFFF6CH			Low

(Continued)

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Interrupt source	EI²OS readiness	Interrupt vector			Interrupt control register		Priority*3
		Number		Address	ICR	Address	
UART1 reception completed	◎	#37	25H	FFFF68H	ICR13	0000BDH*1	High ↑
UART1 transmission completed	Δ	#38	26H	FFFF64H			
UART0 reception completed	◎	#39	27H	FFFF60H	ICR14	0000BEH*1	
UART0 transmission completed	Δ	#40	28H	FFFF5CH			
Flash memory	×	#41	29H	FFFF58H	ICR15	0000BFH*1	
Delay interrupt generation module	×	#42	2AH	FFFF54H			↓ Low

○ : Available

× : Unavailable

◎ : Available EI²OS function is provided.

Δ : Available when a cause of interrupt sharing a same ICR is not used.

*1 : • Peripheral functions sharing an ICR register have the same interrupt level.
• If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.
• If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

*2 : Only 16-bit reload timer is ready for EI²OS. Because PPG is not ready for EI²OS, disable PPG interrupt when using EI²OS with 16-bit reload timer.

*3 : Priority when two or more interrupts of a same level occur simultaneously.

■ PERIPHERAL RESOURCES

1. I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB90895 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

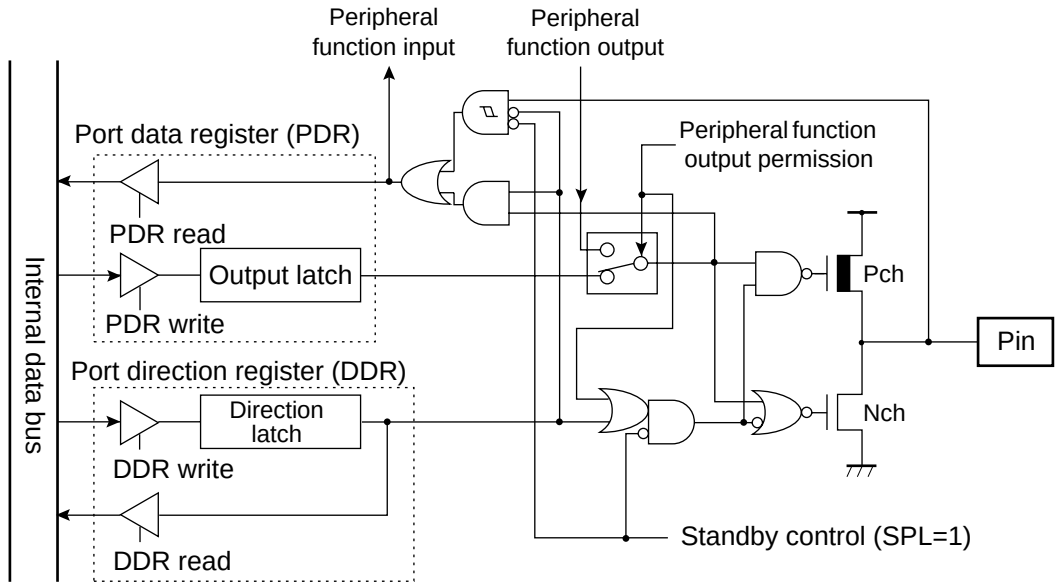
• I/O port functions

An I/O port, using port data resister (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions :

- Port 1 : General-purpose input/output port, used also for PPG timer output and input capture inputs.
- Port 2 : General-purpose input/output port, used also for reload timer input/output and external interrupt input.
- Port 3 : General-purpose input/output port, used also for A/D converter activation trigger pin.
- Port 4 : General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.
- Port 5 : General-purpose input/output port, used also analog input pin.

• Port 1 pins block diagram (single-chip mode)



Standby control : Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

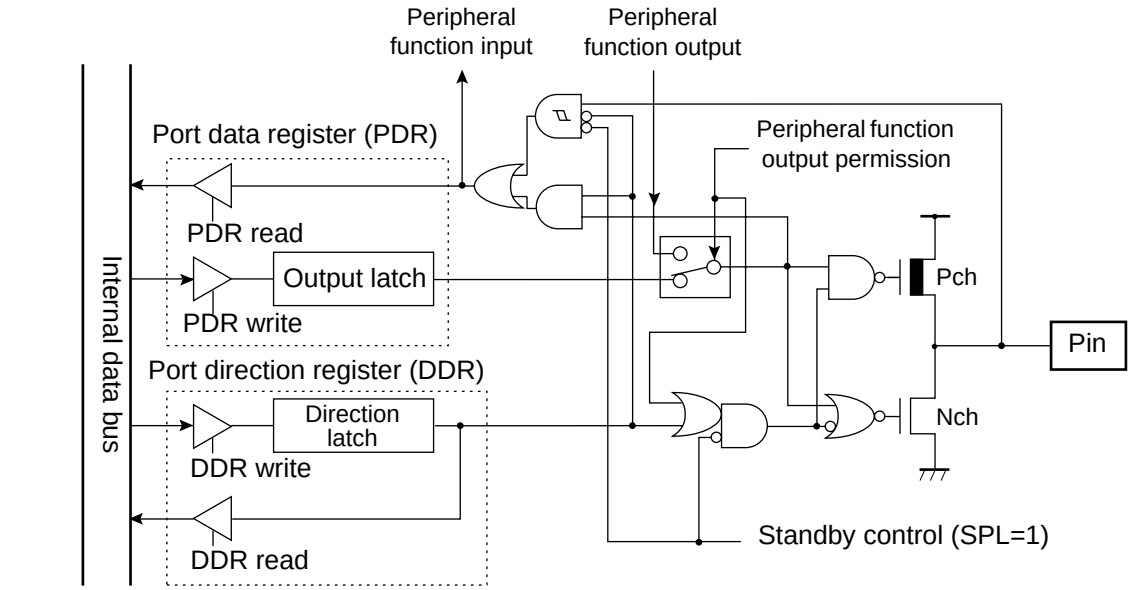
• Port 1 registers (single-chip mode)

- Port 1 registers include port 1 data register (PDR1) and port 1 direction register (DDR1).
- The bits configuring the register correspond to port 1 pins on a one-to-one basis.

Relation between port 1 registers and pins

Port name	Bits of register and corresponding pins								
Port 1	PDR1, DDR1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P17	P16	P15	P14	P13	P12	P11	P10

• **Port 2 pins block diagram (general-purpose input/output port)**



Standby control : Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

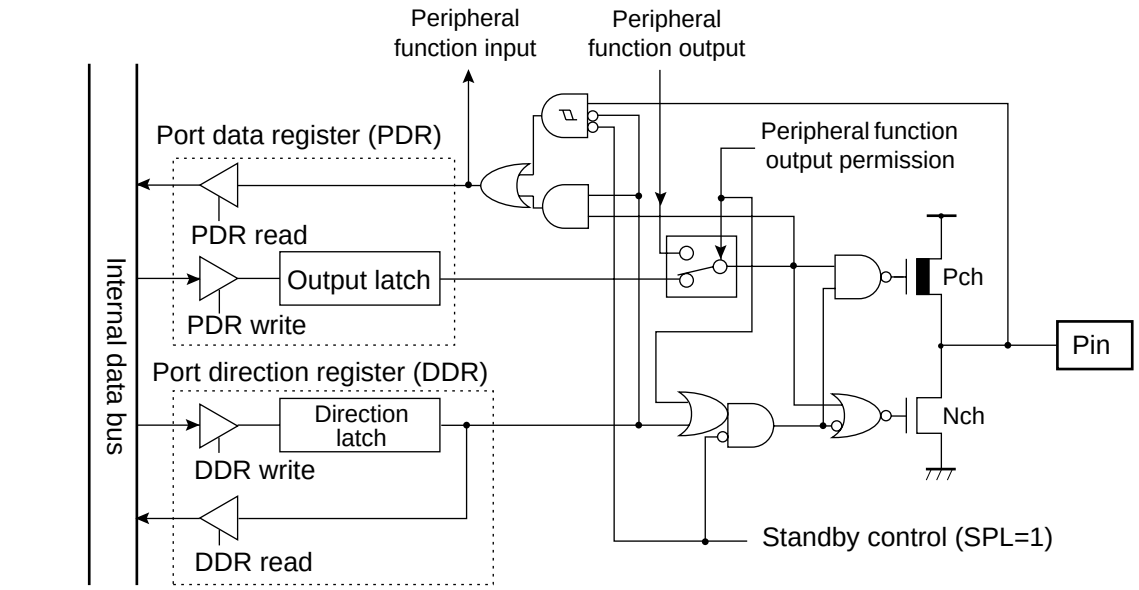
• **Port 2 registers**

- Port 2 registers include port 2 data register (PDR2) and port 2 direction register (DDR2).
- The bits configuring the register correspond to port 2 pins on a one-to-one basis.

Relation between port 2 registers and pins

Port name	Bits of register and corresponding pins								
Port 2	PDR2,DDR2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P27	P26	P25	P24	P23	P22	P21	P20

• Port 3 pins block diagram (general-purpose input/output port)



Standby control : Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

• Port 3 registers

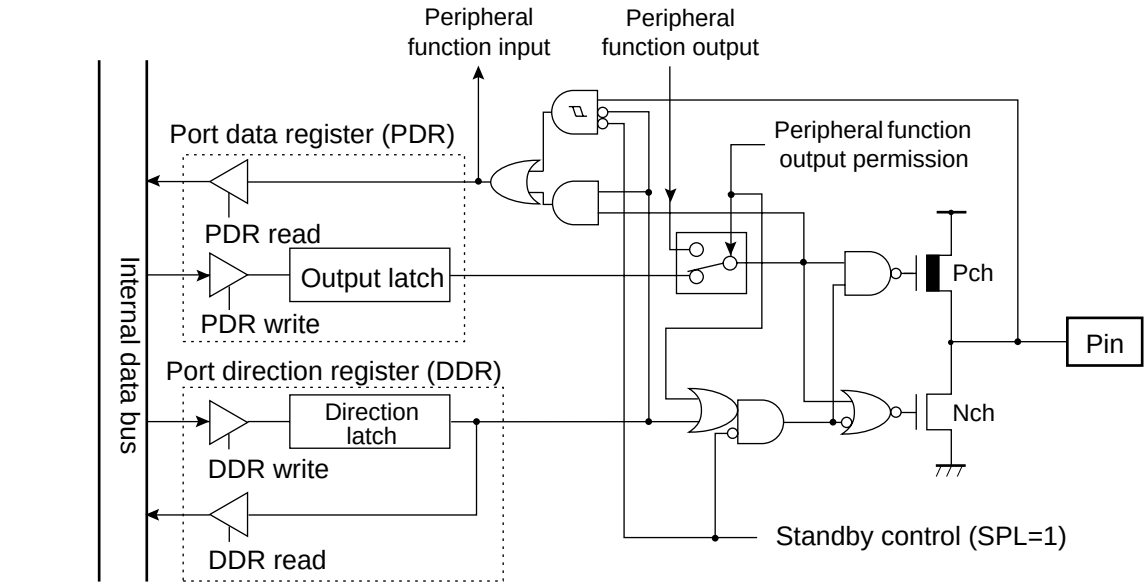
- Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).
- The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between port 3 registers and pins

Port name	Bits of register and corresponding pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	—	P33	P32	P31	P30

* : P35 and P36 do not exist on MB90F897.

• **Port 4 pins block diagram**



Standby control : Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

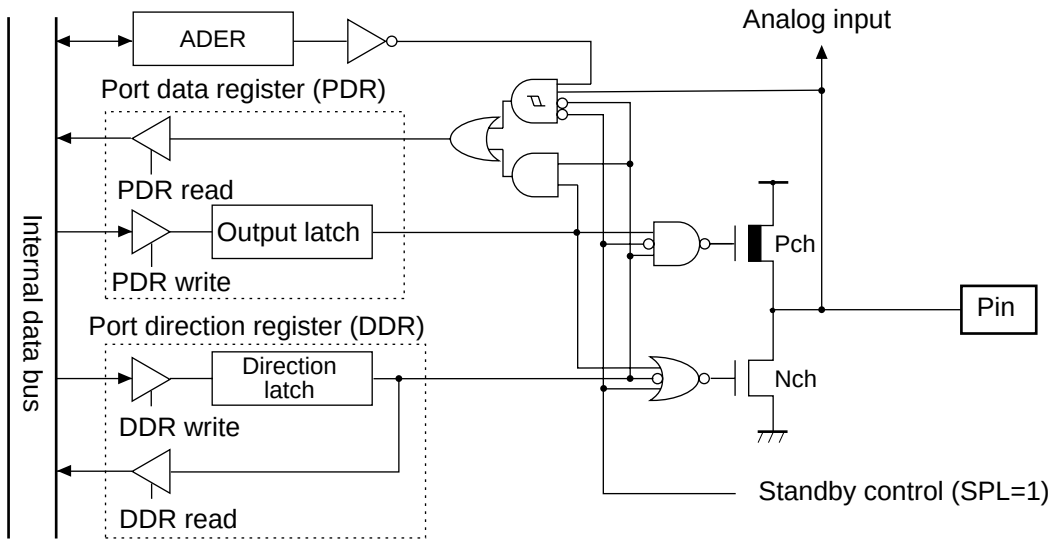
• **Port 4 registers**

- Port 4 registers include port 4 data register (PDR4) and port 4 direction register (DDR4).
- The bits configuring the register correspond to port 4 pins on a one-to-one basis.

Relation between port 4 registers and pins

Port name	Bits of register and corresponding pins								
Port 4	PDR4, DDR4	—	—	—	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	—	—	—	P44	P43	P42	P41	P40

• Port 5 pins block diagram



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and clock mode (SPL=1).

• Port 5 registers

- Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).
- Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.
- The bits configuring the register correspond to port 5 pins on a one-to-one basis.

Relation between port 5 registers and pins

Port name	Bits of register and corresponding pins								
Port 5	PDR5, DDR5	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	ADER	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
	Corresponding pins	P57	P56	P55	P54	P53	P52	P51	P50

2. Time-Base Timer

The time-base time is an 18-bit free-run counter (time-base timer counter) that counts up in synchronization with the main clock (dividing main oscillation clock by 2).

- Four choices of interval time are selectable, and generation of interrupt request is allowed for each interval time.
- Provides operation clock signal to oscillation stabilizing wait timer and peripheral functions.

• Interval timer function

- When the counter of time-base timer reaches an interval time specified by interval time selection bit (TBTC:TBC1, TBC0), an overflow (carrying-over) occurs (TBTC: TBOF=1) and interrupt request is generated.
- If an interrupt by overflow is permitted (TBTC: TBIE=1), an interrupt is generated when overflow occurs (TBTC: TBOF=1).
- The following four interval time settings are selectable :

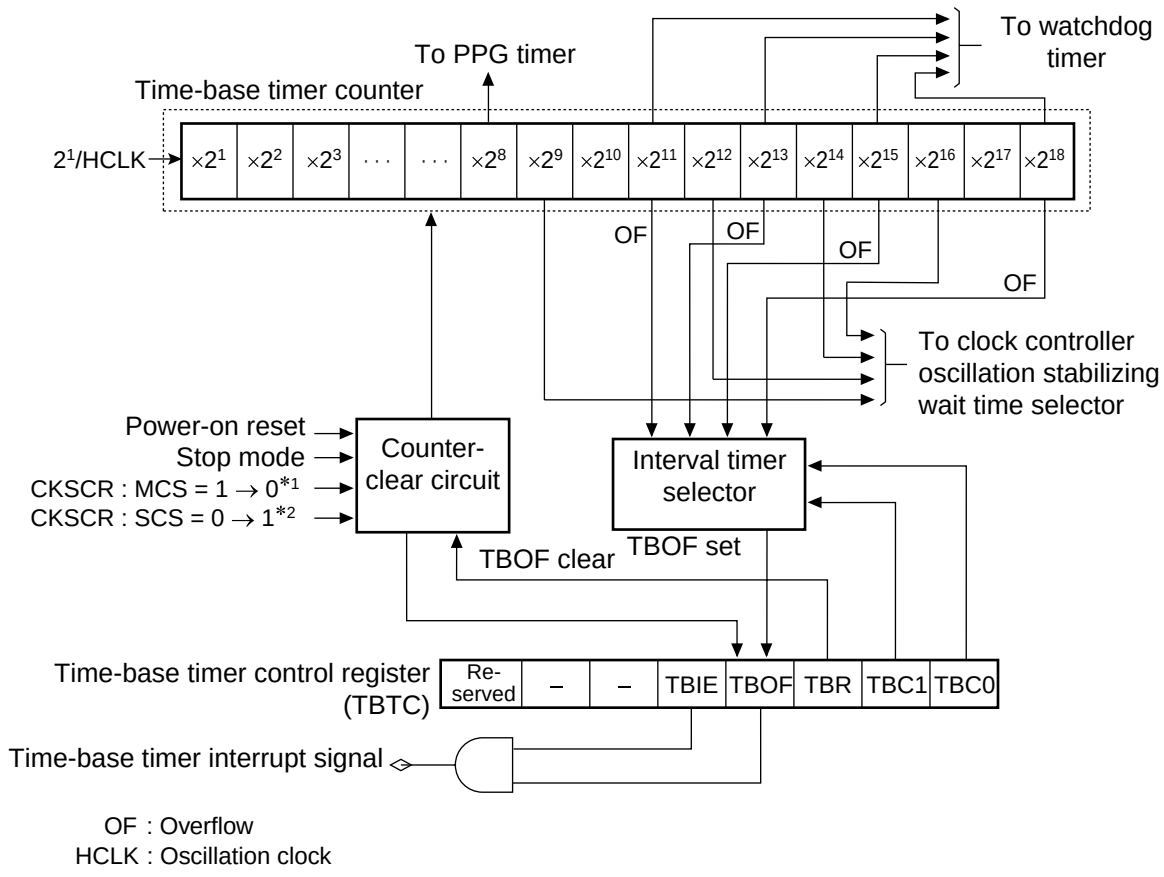
Interval time of time-base timer

Count clock	Interval time
2/HCLK (0.5 μs)	2^{12}/HCLK (Approx. 1.0 ms)
	2^{14}/HCLK (Approx. 4.1 ms)
	2^{16}/HCLK (Approx. 16.4 ms)
	2^{19}/HCLK (Approx. 131.1 ms)

HCLK: Oscillation clock

Values in parentheses “( )” are those under operation of 4-MHz oscillation clock.

• **Time-base timer block diagram**



OF : Overflow
HCLK : Oscillation clock

*1: Switch machine clock from main clock to PLL clock.

*2: Switch machine clock from sub clock to main clock.

Note : Actual interrupt request number of time-base timer is as follows:

Interrupt request number: #16 (10_H)

3. Watchdog Timer

The watchdog timer is a 2-bit counter that uses time-base timer or clock timer as count clock. If the counter is not cleared within an interval time, CPU is reset.

•Watchdog timer functions

- The watchdog timer is a timer counter that prevents runaway of a program. Once a watchdog timer is activated, the counter of watchdog timer must always be cleared within a specified time of interval. If specified interval time elapses without clearing the counter of a watchdog timer, CPU resetting occurs. This is the function of a watchdog timer.
- The interval time of a watchdog timer is determined by a clock cycle, which is input as a count clock. Watchdog resetting occurs between a minimum time and a maximum time specified.
- The output target of a clock source is specified by the watchdog clock selection bit (WTC: WDCS) in the clock timer control register.
- Interval time of a watchdog timer is specified by the time-base timer output selection bit/clock timer output selection bit (WDTC: WT1, WT0) in the watchdog timer control register.

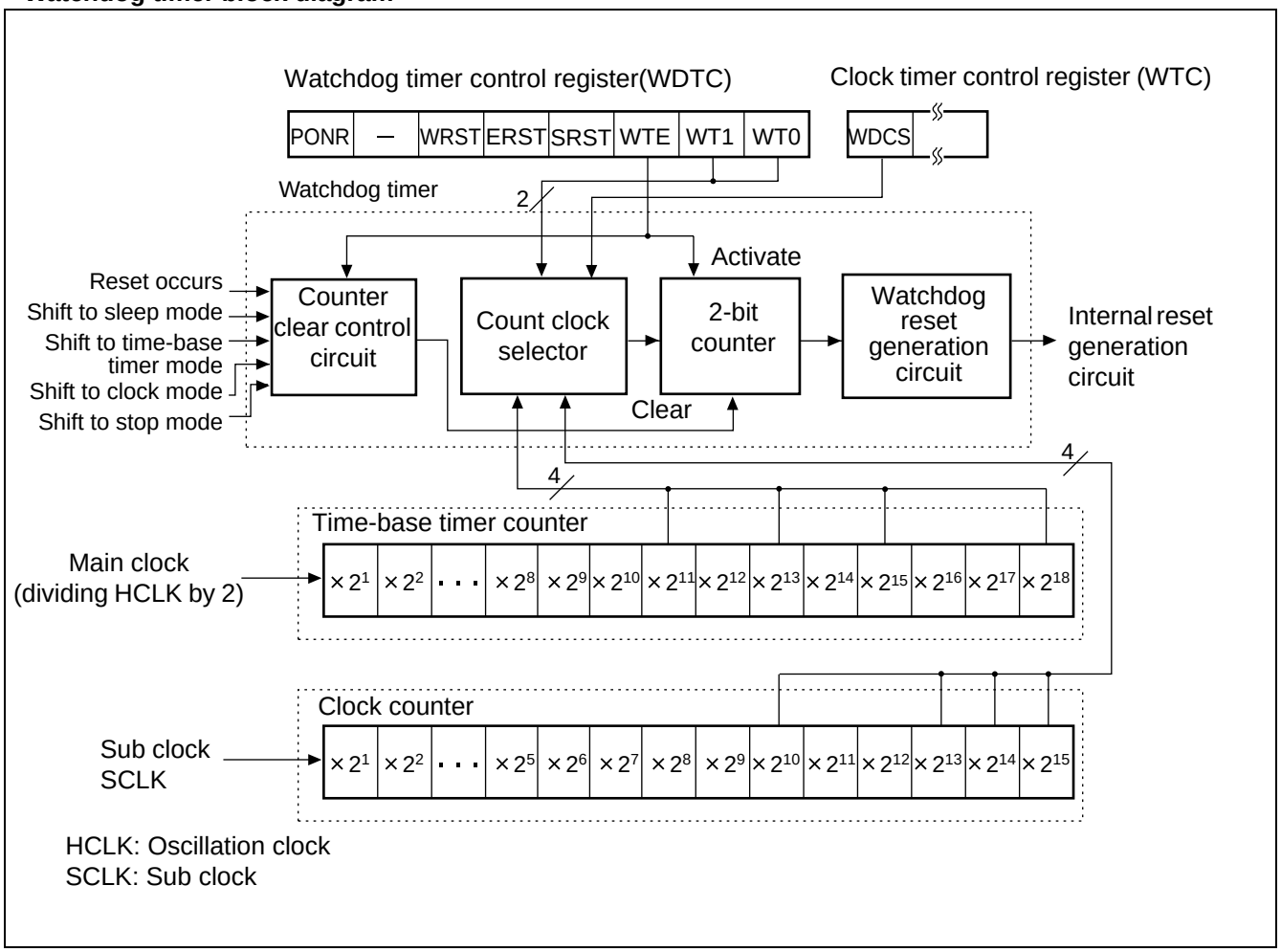
Interval timer of watchdog timer

Min	Max	Clock cycle	Min	Max	Clock cycle
Approx. 3.58 ms	Approx. 4.61 ms	2^{14}±2^{11} /HCLK	Approx. 0.457 s	Approx. 0.576 s	2^{12}±2^{9} /SCLK
Approx. 14.33 ms	Approx. 18.3 ms	2^{16}±2^{13} /HCLK	Approx. 3.584 s	Approx. 4.608 s	2^{15}±2^{12} /SCLK
Approx. 57.23 ms	Approx. 73.73 ms	2^{18}±2^{15} /HCLK	Approx. 7.168 s	Approx. 9.216 s	2^{16}±2^{13} /SCLK
Approx. 458.75 ms	Approx. 589.82 ms	2^{21}±2^{18} /HCLK	Approx. 14.336 s	Approx. 18.432 s	2^{17}±2^{14} /SCLK

HCLK: Oscillation clock (4 MHz) , CSCLK: Sub clock (8.192 kHz)

Notes: • If the time-base timer is cleared when watchdog timer count clock is used as time base timer output (carry-over signal), watchdog reset time may become longer.
• When using the sub clock as machine clock, be sure to specify watchdog timer clock source selection bit (WDCS) in clock timer control register (WTC) at “0,” selecting output of clock timer.

• **Watchdog timer block diagram**



4. 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

• Configuration of 16-bit input/output timer

The 16-bit input/output timer is composed of the following modules:

- 16-bit free-run timer (1 unit)
- Input capture (2 units, 2 input pins per unit)

• Functions of 16-bit input/output timer

(1) Functions of 16-bit free-run timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

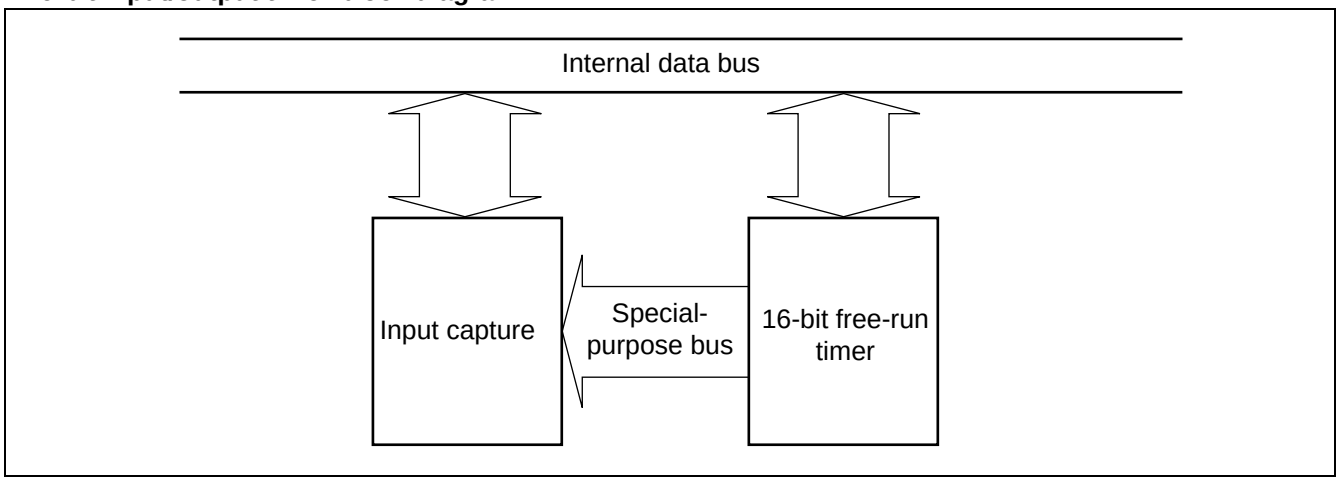
- Count clock is set among 8 types of machine clock dividing rates.
  Count clock : ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128
- Generation of interrupt is allowed by counter value overflow.
- Activation of expanded intelligent I/O service (EI^{2}OS) is allowed by interrupt generation.
- Counter value of 16-bit free-run timer is cleared to "0000$_H$" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).
- Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

(2) Functions of input capture

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

- Rising edge, falling edge, and both edges are selectable for detection.
- Generating interrupt on CPU is allowed by detecting an edge of input signal.
- Expanded intelligent I/O service (EI^{2}OS) is activated by interrupt generation.
- The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

• 16-bit input/output timer block diagram



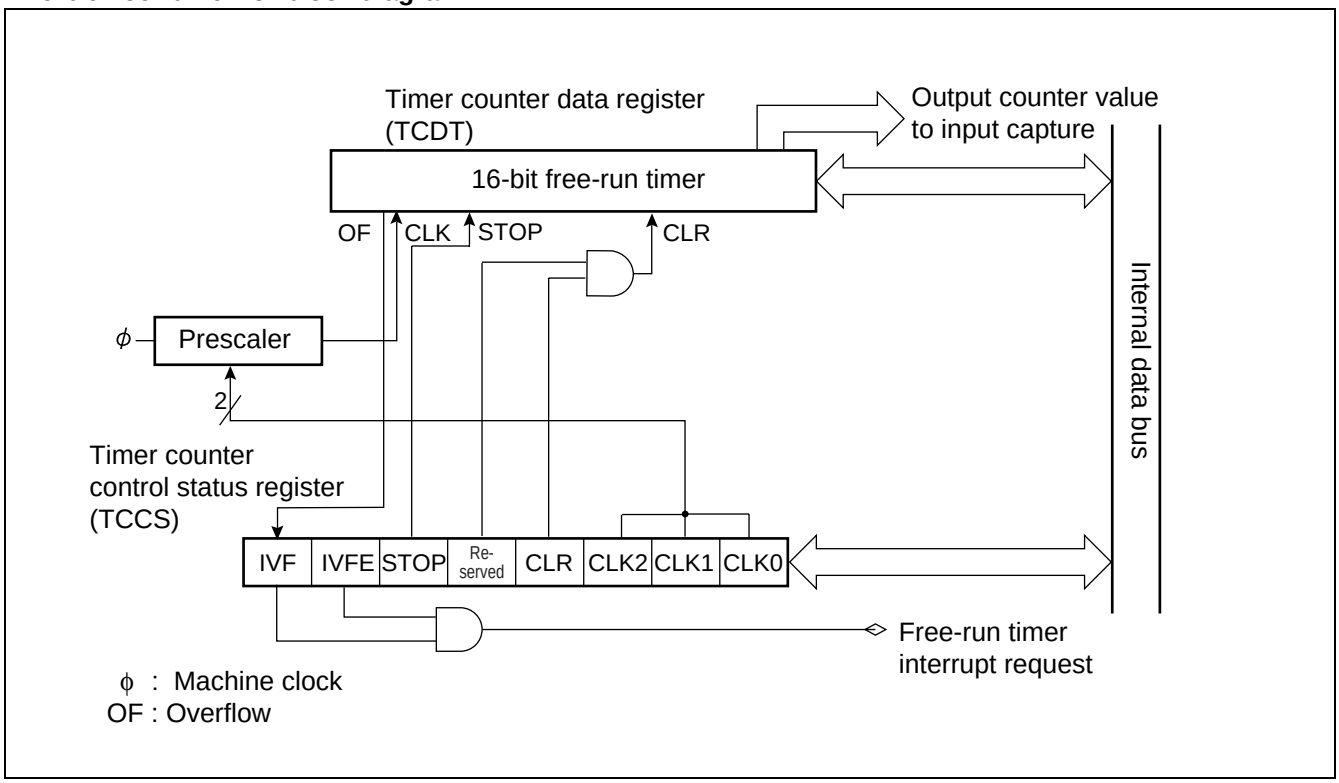
• 16-bit free-run timer

Counter value of 16-bit free-run timer is used as reference time (base time) of input capture.

• Input capture

Input capture detects rising edge, falling edge or both edges and retains a counter value of 16-bit free-run timer. Detection of edge on input signal is allowed to generate interrupt.

• 16-bit free-run timer block diagram



• Detailed pin assignment on block diagram

The 16-bit input/output timer includes a 16-bit free-run timer. Interrupt request number of the 16-bit free-run timer is as follows:
Interrupt request number: #19 (13_H)

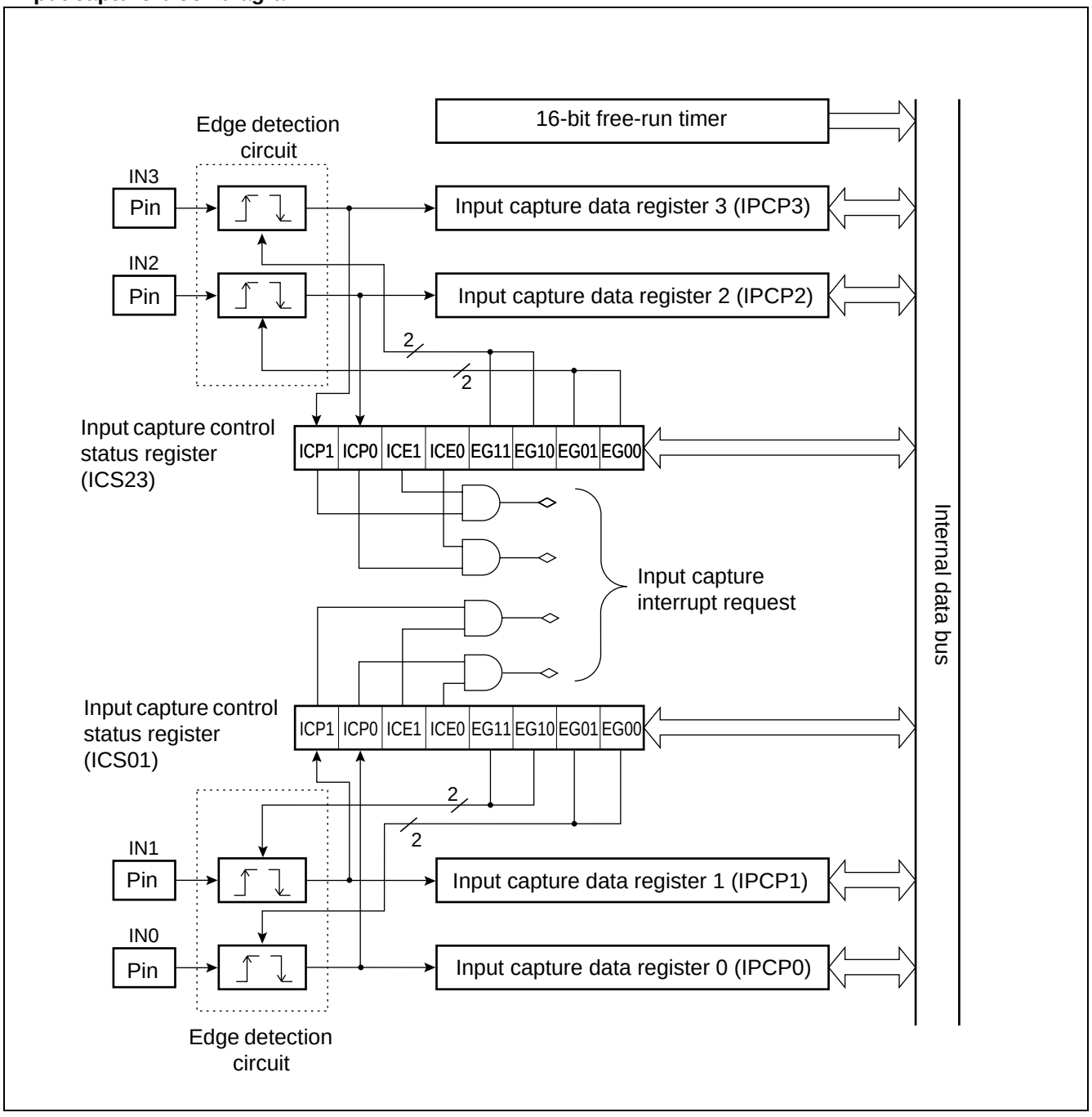
• Prescaler

The prescaler divides a machine clock and provides a counter clock to the 16-bit up counter. Dividing ratio of the machine clock is specified by timer counter control status register (TCCS) among four values.

• Timer counter data register (TCDT)

The timer counter data register is a 16-bit up counter. A current counter value of the 16-bit free-run timer is read. Writing a value during halt of the counter allows setting an arbitrary counter value.

•Input capture block diagram



5. 16-bit Reload Timer

The 16-bit reload timer has the following functions:

- Count clock is selectable among 3 internal clocks and external event clock.
- Activation trigger is selectable between software trigger and external trigger.
- Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.
- When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.
- The 16-bit reload timer is ready for expanded intelligent I/O service (EI^{2}OS).
- MB90895 series device has 2 channels of built-in 16-bit reload timer.

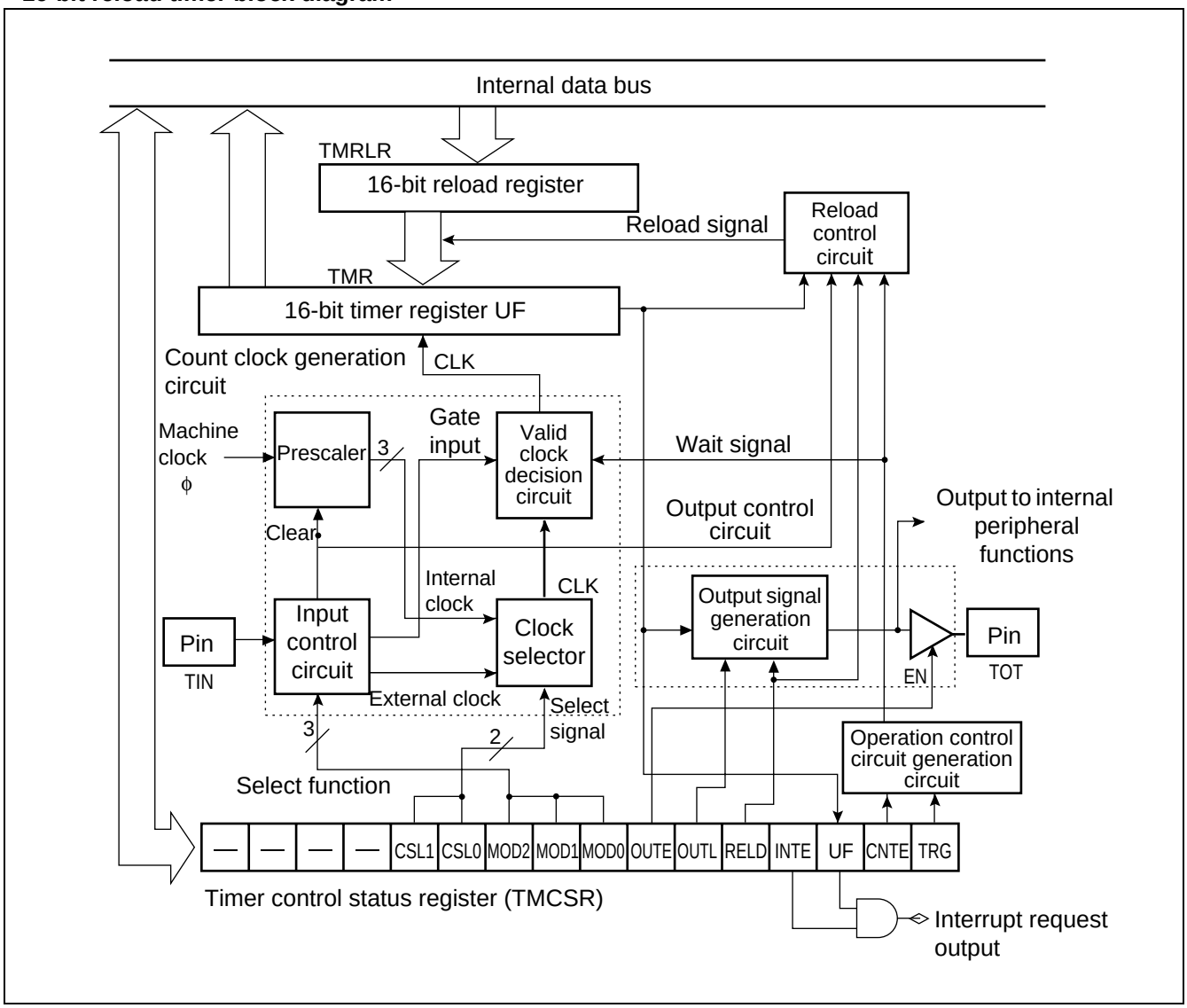
• Operation mode of 16-bit reload timer

Count clock	Activation trigger	Operation upon underflow
Internal clock mode	Software trigger, external trigger	One-shot mode, reload mode
Event count mode	Software trigger	One-shot mode, reload mode

• Internal clock mode

- The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to “00_B”, “01_B”, “10_B”.
- In the internal clock mode, the counter decrements in synchronization with the internal clock.
- Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.
- Edge detection of software trigger or external trigger is specified as an activation trigger.

• **16-bit reload timer block diagram**



6. Clock Timer Outline

The clock timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 8 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

• Interval timer function

- In the clock timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of clock timer is selectable among the following 8 choices :

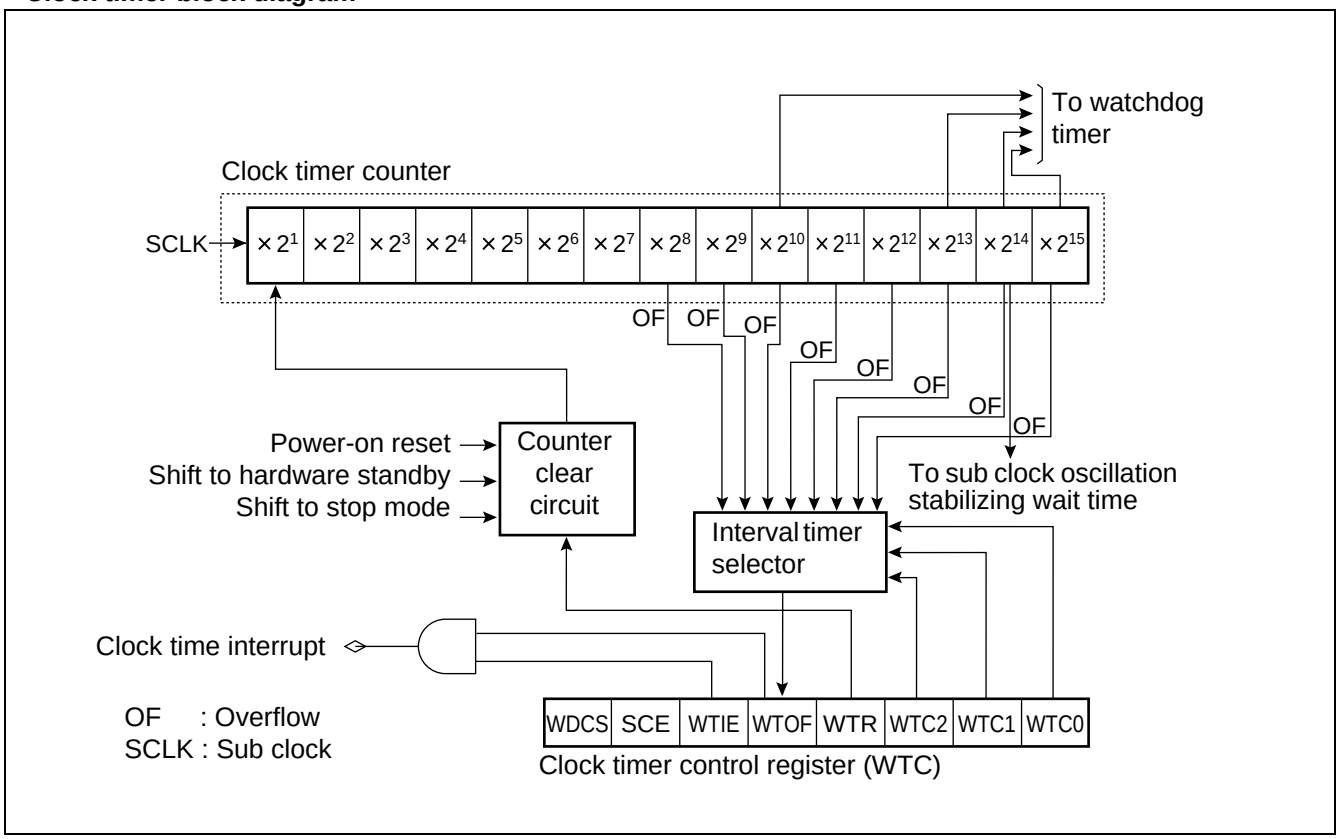
• Interval time of clock timer

Sub clock cycle	Interval time
SCLK (122 µs)	2^8/SCLK (31.25 ms)
	2^9/SCLK (62.5 ms)
	2^{10}/SCLK (125 ms)
	2^{11}/SCLK (250 ms)
	2^{12}/SCLK (500 ms)
	2^{13}/SCLK (1.0 s)
	2^{14}/SCLK (2.0 s)
	2^{15}/SCLK (4.0 s)

SCLK: Sub clock frequency

Values in parentheses “( )” are calculation when operating with 8.192 kHz clock.

• **Clock timer block diagram**



Actual interrupt request number of clock timer is as follows :

Interrupt request number : #28 ($1C_H$)

• **Clock timer counter**

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

• **Counter clear circuit**

A circuit that clears the clock timer counter.

7. 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

- 8-bit PPG output 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8-bit and 8-bit PPG output operation mode

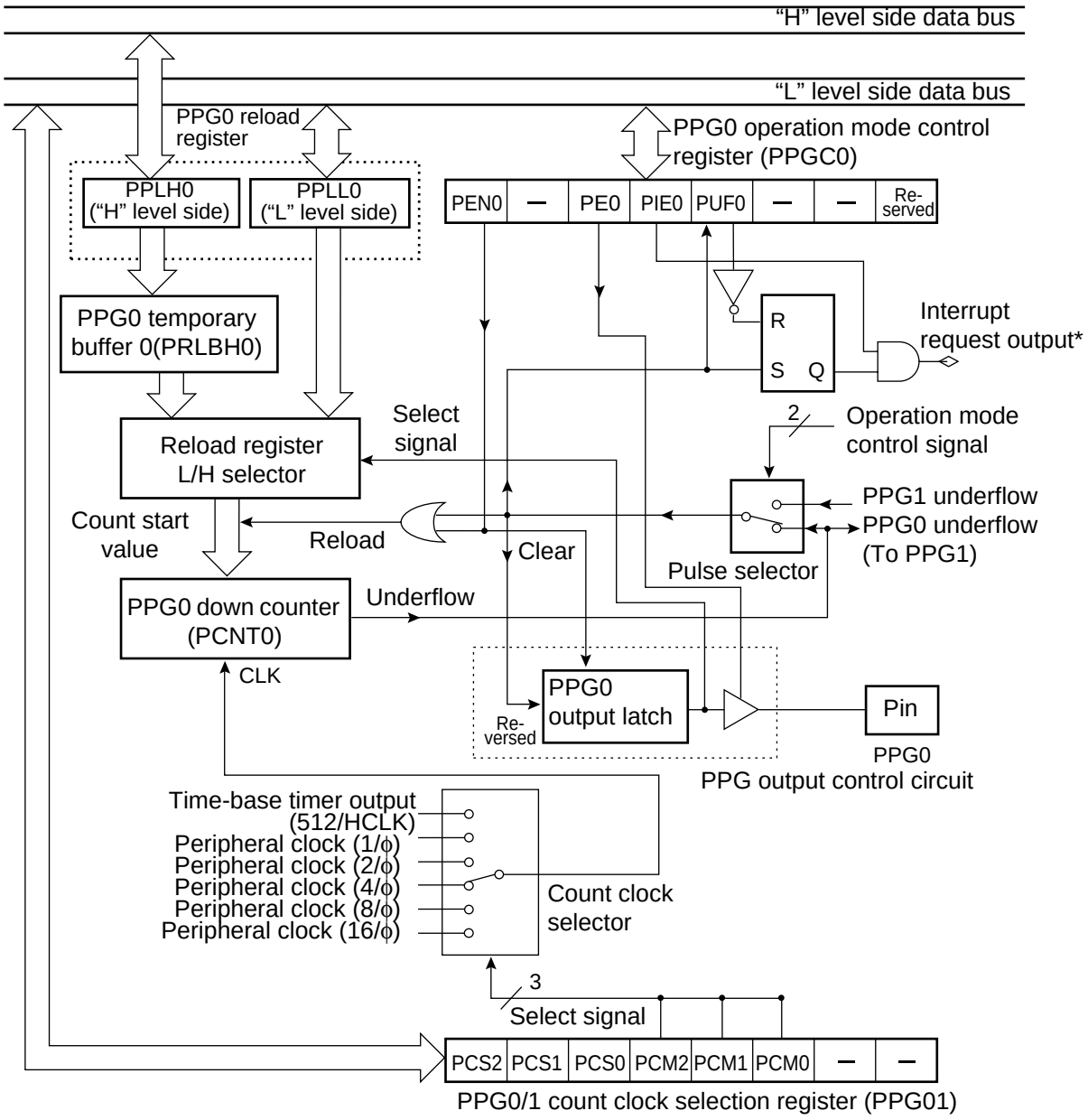
MB90895 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

• Functions of 8/-16-bit PPG timer

The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

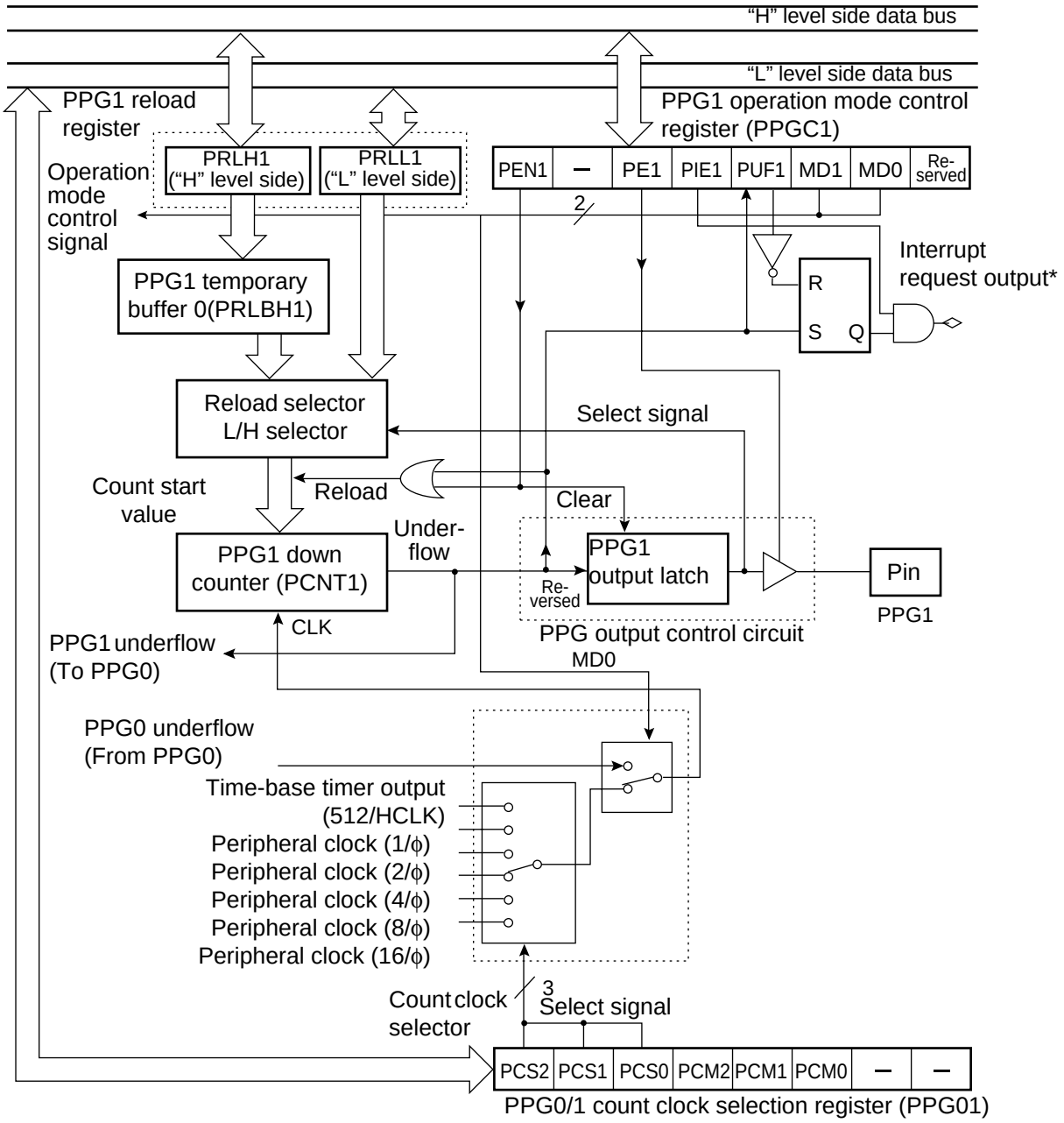
- Widths of “H” and “L” in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.
- Count clock is selectable among 6 internal clocks.
- The timer is usable as an interval timer, by generating interrupt requests for each interval.
- The time is usable as a D/A converter, with an external circuit.

• **8/16-bit PPG timer 0 block diagram**



– : Undefined
Reserved : Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

• **8/16-bit PPG timer 1 block diagram**



– : Undefined
Reserved : Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 1 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 0.

8. Delay Interrupt Generation Module Outline

The delay interrupt generation module is a module that generates interrupts for switching tasks. Generation of a hardware interrupt request is performed by software.

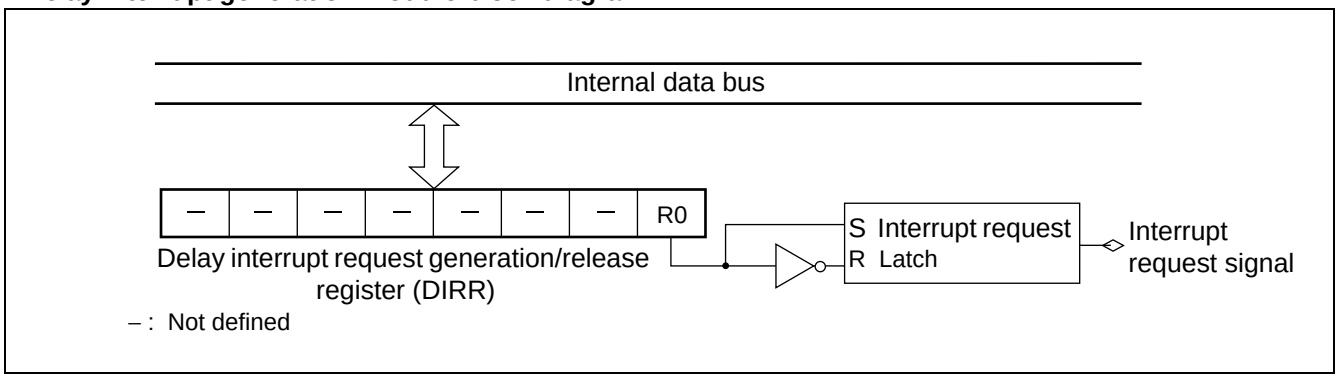
• Delay interrupt generation module outline

Using the delay interrupt generation module, hardware interrupt request is generated and released by software.

Delay interrupt generation module outline

	Function and control
Cause of interrupt	Set “1” in R0 bit of delay interrupt request generation/release register (DIRR: R0=1), generating an interrupt request. Set “0” in R0 bit of delay interrupt request generation/release register (DIRR: R0=0), releasing an interrupt request.
Interrupt number	#42 ($2A_H$)
Interrupt control	No setting of permission register is provided.
Interrupt flag	Retained in DIRR: R0 bit
EI^2OS	Not ready for expanded intelligent I/O service.

• Delay interrupt generation module block diagram



• Interrupt request latch

A latch that retains settings on delay interrupt request generation/release register (generation or release of delay interrupt request).

• Delay interrupt request generation/release register (DIRR)

Generates or releases delay interrupt request.

• Interrupt number

An interrupt number used in delay interrupt generation module is as follows:

Interrupt number: #42 ($2A_H$)

9. DTP/External Interrupt and CAN Wakeup Outline

DTP/external interrupt transfers an interrupt request generated by an external peripheral device or a data transmission request to CPU, generating external interrupt request and activating expanded intelligent I/O service. Input RX of CAN controller is used as external interrupt input.

• DTP/external interrupt and CAN wakeup function

An interrupt request input from external peripheral device to external input pins (INT7 to INT4) and RX pin, just as interrupt request of peripheral device, generates an interrupt request. The interrupt request generates an external interrupt and activates expanded intelligent I/O service (EI^2OS).

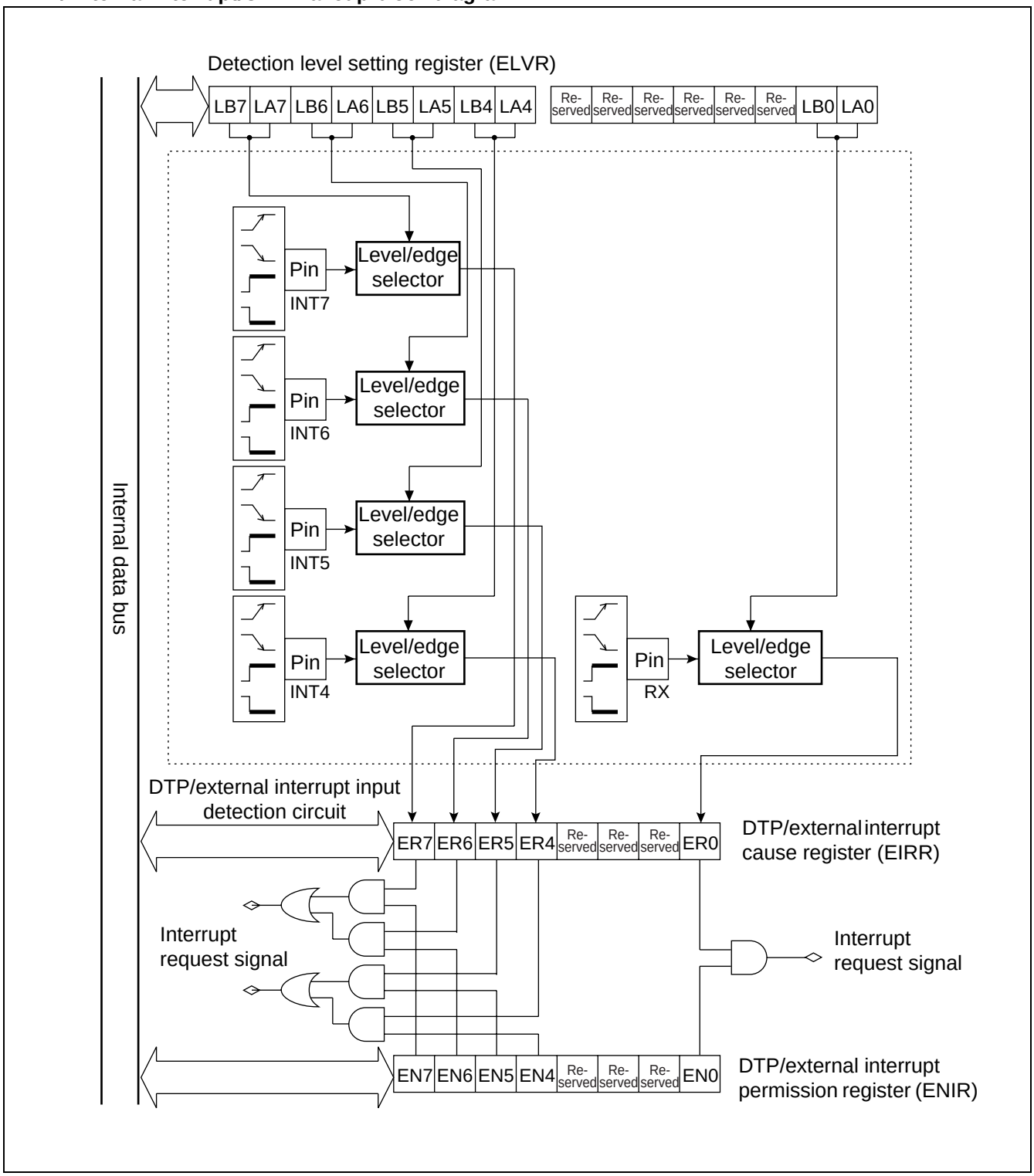
If the expanded intelligent I/O service (EI^2OS) has been disabled by interrupt control register (ICR : ISE=0), external interrupt function is enabled and branches to interrupt processing.

If the EI^2OS has been enabled, (ICR : ISE=1), DTP function is enabled and automatic data transmission is performed by EI^2OS. After performing specified number of data transmission processes, the process branches to interrupt processing.

DTP/external interrupt and CAN wakeup outline

	External interrupt	DTP function
Input pin	5 pins (RX, and INT4 to INT7)	
Interrupt cause	Specify for each pin with detection level setting register (ELVR).	
	Input of “H” level/“L” level/rising edge/falling edge.	Input of “H” level/ “L” level
Interrupt number	#15 ($0F_H$) , #24 (18_H) , #27 ($1B_H$)	
Interrupt control	Enabling or disabling output of interrupt request, using DTP/external interrupt permission register (ENIR).	
Interrupt flag	Retaining interrupt cause with DTP/external interrupt cause register (EIRR).	
Process selection	Disable EI^2OS (ICR : ISE=0)	Enable EI^2OS (ICR : ISE=1)
Process	Branch to external interrupt process	After automatic data transmission by EI^2OS for specified number of times, branch to interrupt process.

• **DTP/External interrupt/CAN wakeup block diagram**



10. 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog input voltage into 8-bit or 10/bit digital value, using the RC-type successive approximation conversion method.

- Input signal is selected among 8 channels of analog input pins.
- Activation trigger is selected among software trigger, internal timer output, and external trigger.

• Functions of 8/10-bit A/D converter

The 8/10-bit A/D converter converts an analog voltage (input voltage) input to analog input pin into an 8-bit or 10-bit digital value (A/D conversion).

The 8/10-bit A/D converter has the following functions:

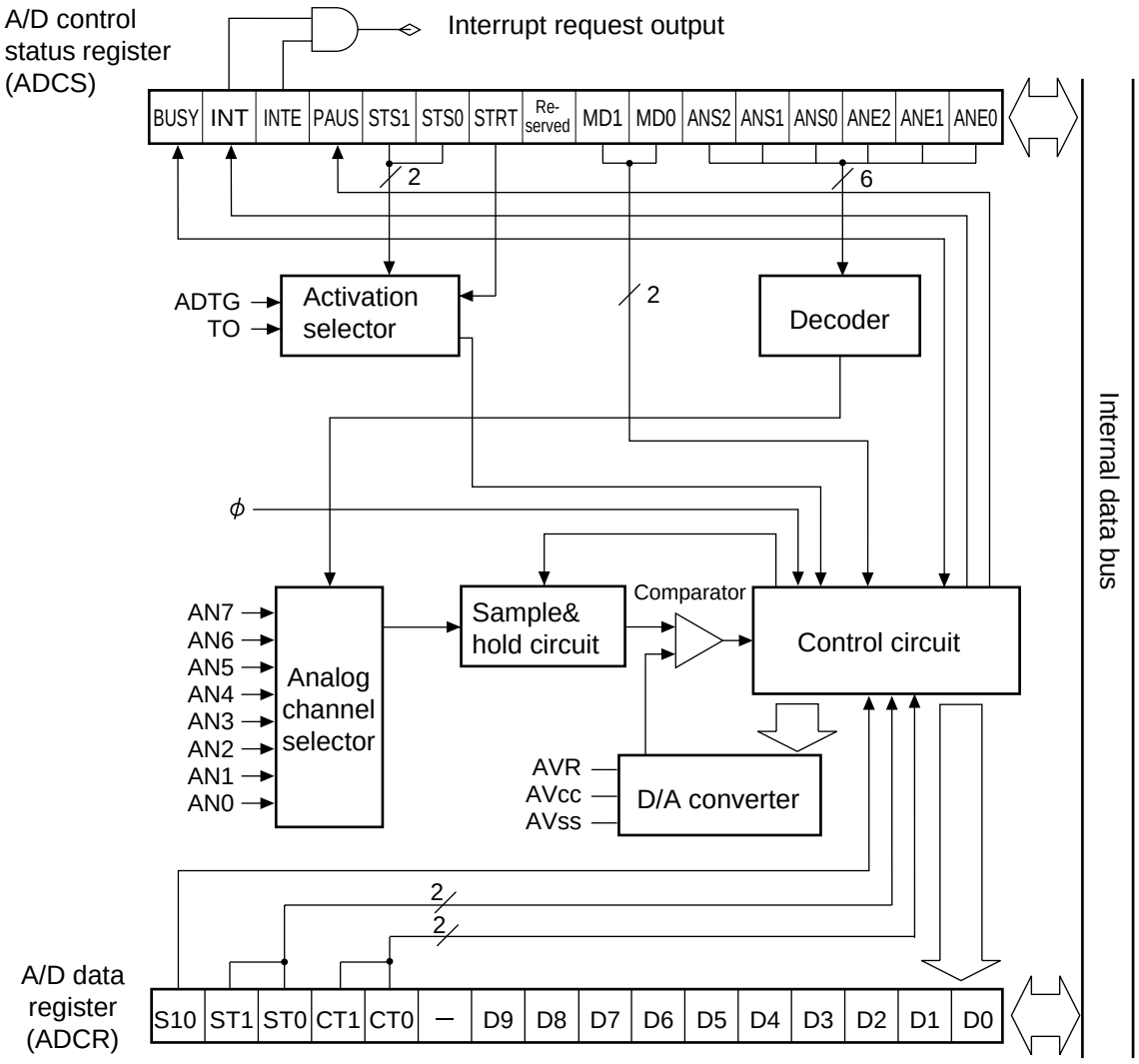
- A/D conversion takes a minimum of 6.12 μs* for one channel, including sampling time. (A/D conversion)
- Sampling of one channel takes a minimum of 2.0 μs*.
- RC-type successive approximation conversion method, with sample & hold circuit is used for conversion.
- Resolution of either 8 bits or 10 bits is specifiable.
- A maximum of 8 channels of analog input pins are allowed for use.
- Generation of interrupt request is allowed, by storing A/D conversion result in A/D data register.
- Activation of EI^{2}OS is allowed upon occurrence of an interrupt request. With use of EI^{2}OS, data loss is avoided even if A/D conversion is performed successively.
- An activation trigger is selectable among software trigger, internal timer output, and external trigger (fall edge).

*: When operating with 16-MHz machine clock

• 8/10-bit A/D converter conversion mode

Conversion mode	Description
Singular conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function stops.
Sequential conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function resumes from the start channel.
Pausing conversion mode	The A/D conversion is performed by pausing at each channel. Upon completion of A/D conversion on an end channel, A/D conversion and pause functions resume from the start channel.

• **8/10-bit A/D converter block diagram**



TO : Internal timer output
– : Not defined
Reserved : Be sure to set to “0”
ϕ : Machine clock

11. UART0/UART1 Outline

UART0/UART1 are general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

- Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.
- Provided with master/slave communication function (multi-processor mode). (Only master side is available.)
- Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.
- Ready for expanded intelligent service, EI^{2}OS.

UART functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI^{2}OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note : Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

UART0/UART1 operation modes

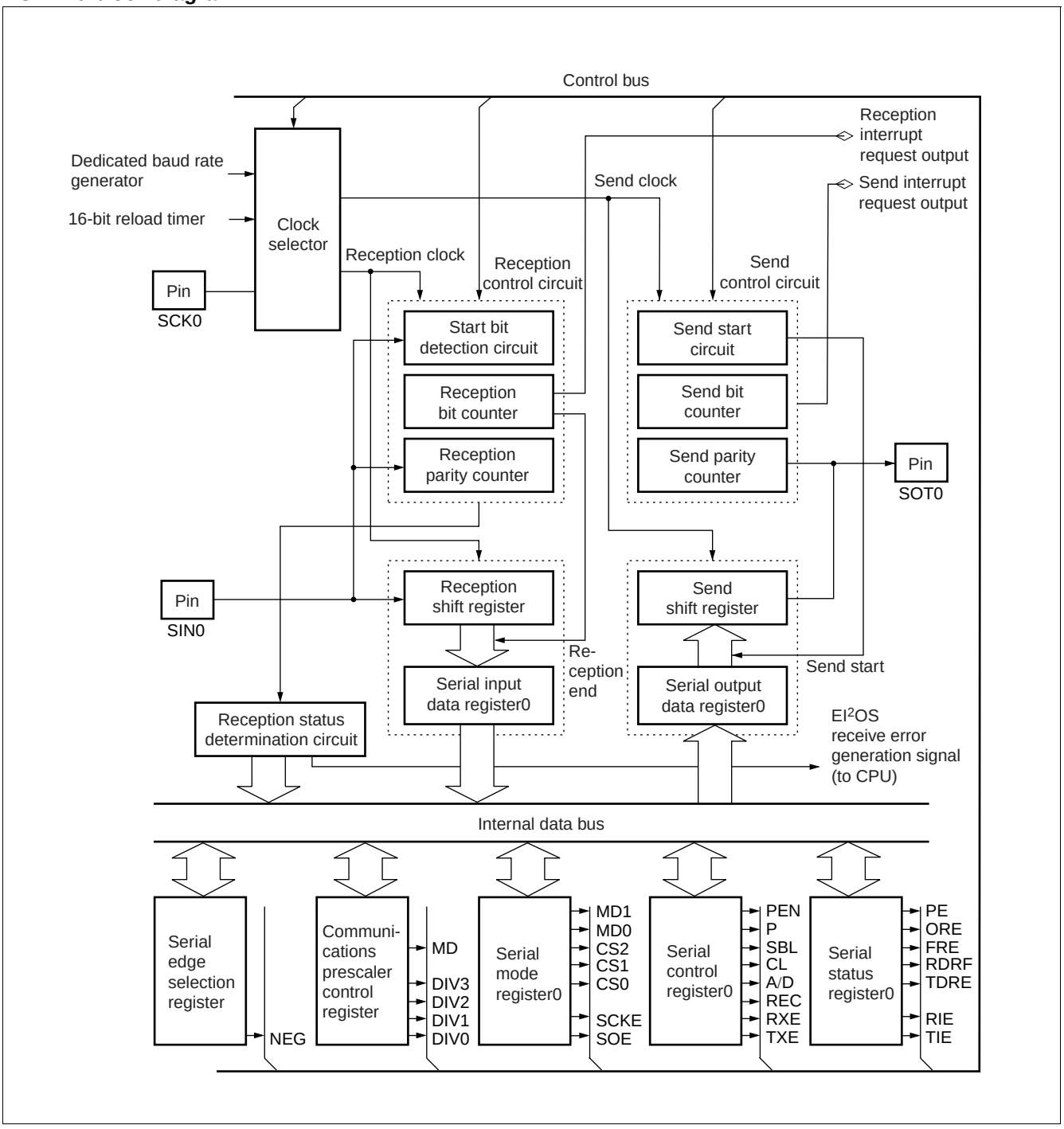
Operation mode		Data length		Synchronization	Stop bit length
		With parity	Without parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1*1	—	Asynchronous	
2	Synchronous mode	8	—	Synchronous	No

— : Disallowed

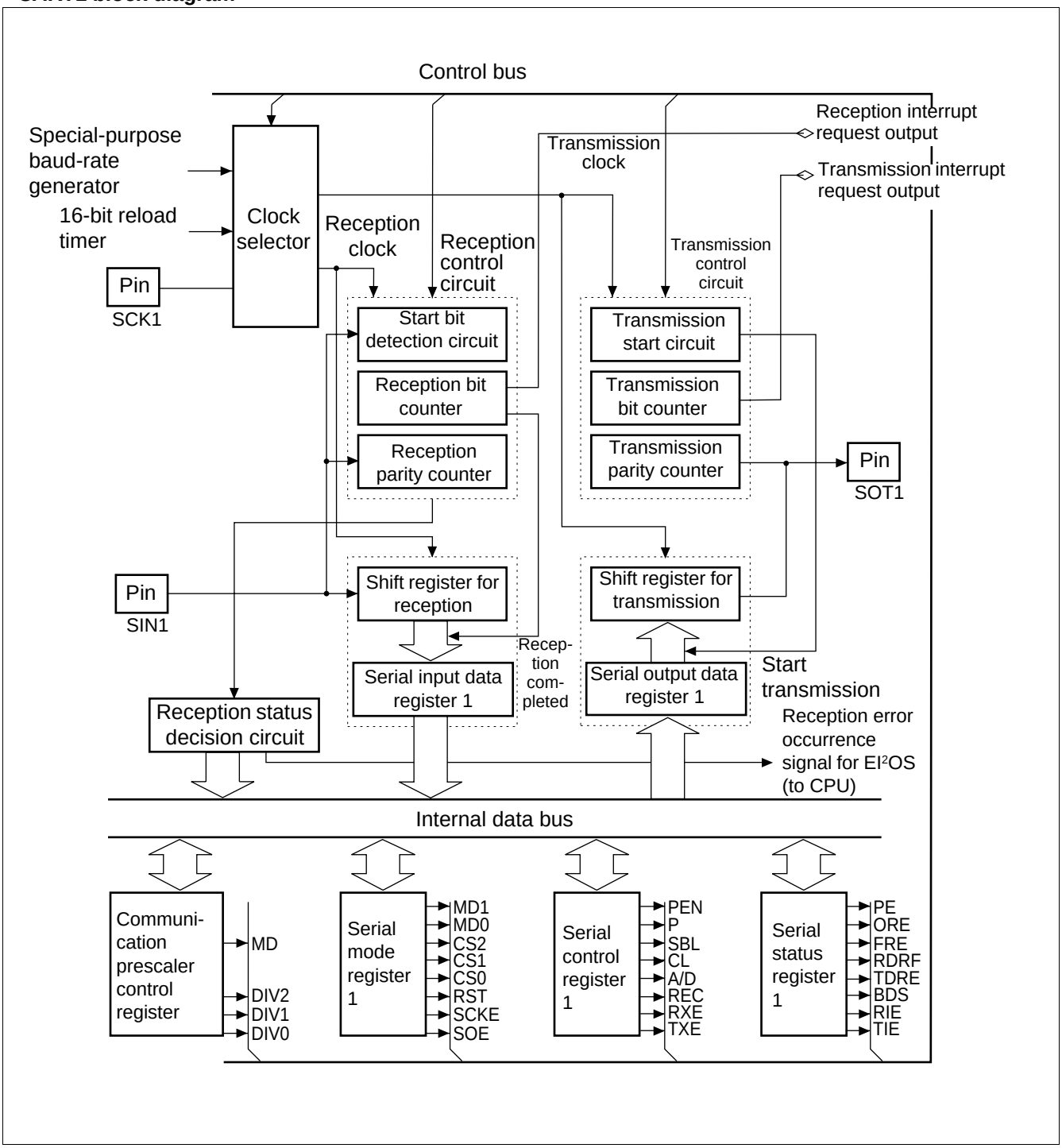
*1 : “+1” is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

*2 : Only 1 bit is detected as a stop bit on data reception.

• **UART0 block diagram**



• **UART1 block diagram**



12. CAN Controller

The Controller Area Network (CAN) is a serial communication protocol compliant with CAN Ver 2.0A and Ver 2.0B. The protocol allows data transmission and reception in both standard frame format and expanded frame format.

• Features of CAN controller

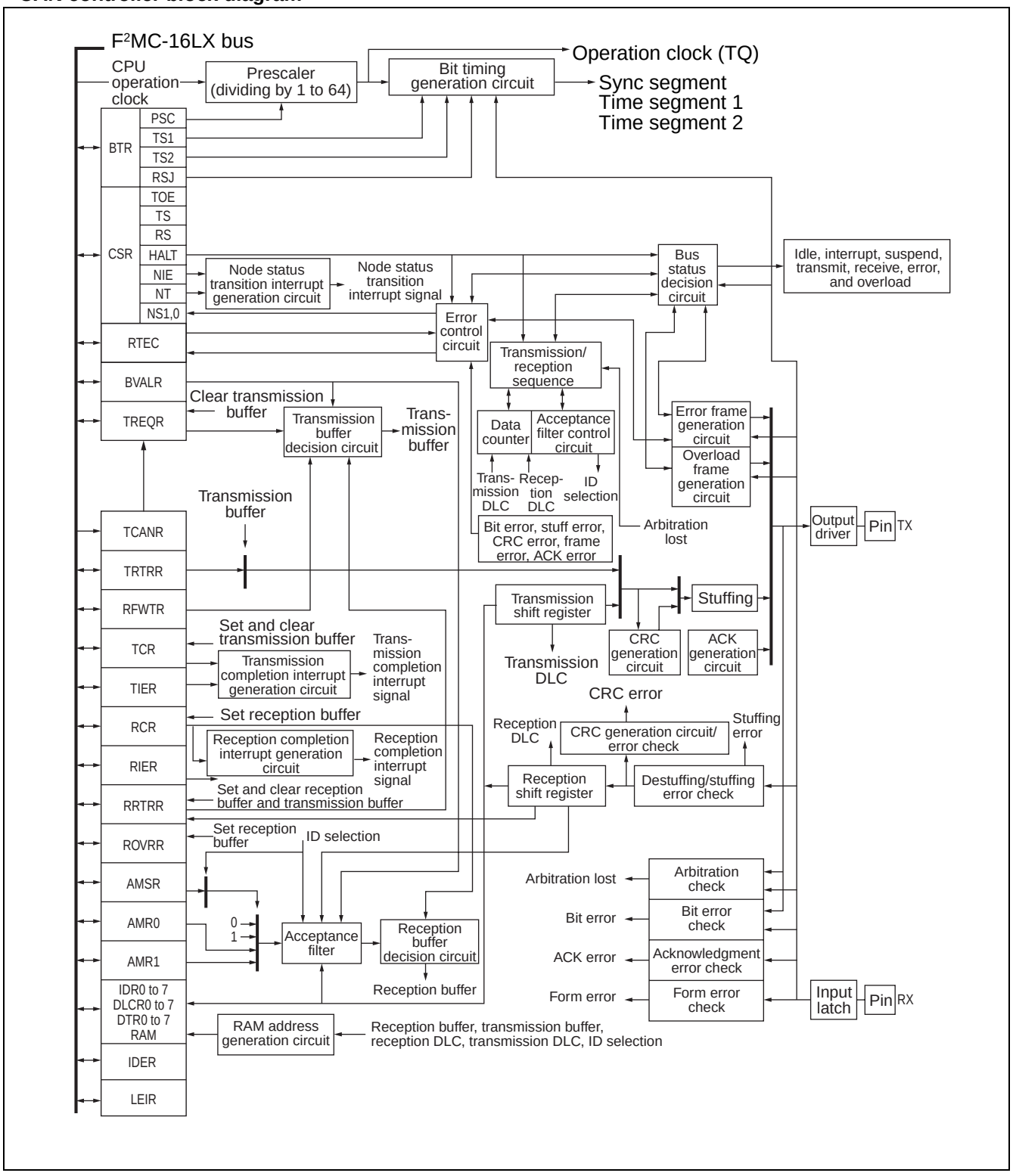
- CAN controller format is compliant with CAN Ver 2.0A and Ver 2.0B.
- The protocol allows data transmission and reception in standard frame format and expanded frame format.
- Automatic transmission of data frame by remote frame reception is allowed.
- Baud rate ranges from 10 Kbps to 1 Mbps (with 16-MHz machine clock).

Data transmission baud rate

Machine clock	Baud rate (Max)
16 MHz	1 Mbps
12 MHz	1 Mbps
8 MHz	1 Mbps
4 MHz	500 Kbps
2 MHz	250 Kbps

- Provided with 8 transmission/reception message buffers.
- Transmission/reception is allowed at ID11bit in standard format, and at ID29bit in expanded frame format.
- Specifying 0 byte to 8 bytes is allowed in message data.
- Multi-level message buffer configuration is allowed.
- CAN controller has two built-in acceptance masks. Mask settings are independently allowed for the two acceptance masks on reception IDs.
- The two acceptance masks allow reception in standard frame format and expanded frame format.
- For types of masking, all-bit comparison, all-bit masking, and partial masking with acceptance mask register 0/1, are specifiable.

• **CAN controller block diagram**



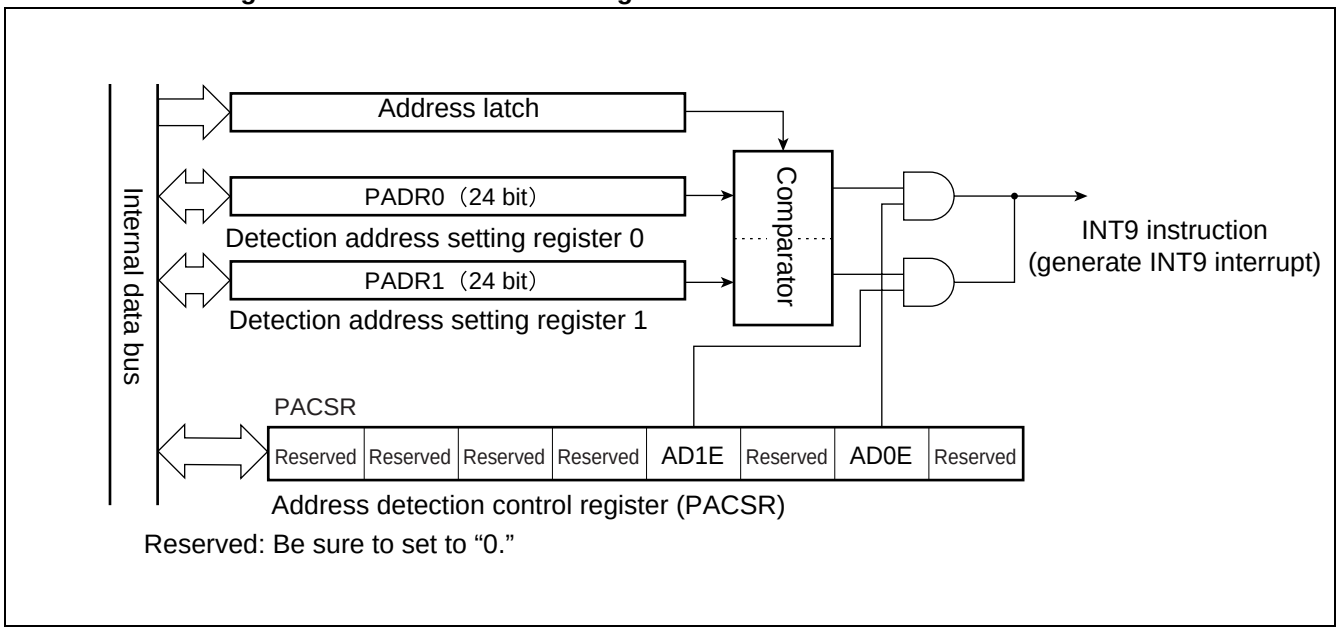
13. Address Matching Detection Function Outline

The address matching detection function checks if an address of an instruction to be processed next to a currently-processed instruction is identical with an address specified in the detection address register. If the addresses match with each other, an instruction to be processed next in program is forcibly replaced with INT9 instruction, and process branches to the interrupt process program. Using INT9 interrupt, this function is available for correcting program by batch processing.

• Address matching detection function outline

- An address of an instruction to be processed next to a currently-processed instruction of the program is always retained in an address latch via internal data bus. By the address matching detection function, the address value retained in the address latch is always compared with an address specified in detection address setting register. If the compared address values match with each other, an instruction to be processed next by CPU is forcibly replaced with INT9 instruction, and an interrupt process program is executed.
- Two detection address setting registers are provided (PADR0 and PADR1), and each register is provided with interrupt permission bit. Generation of interrupt, which is caused by address matching between the address retained in address latch and the address specified in address setting register, is permitted and prohibited on a register-by-register basis.

• Address matching detection function block diagram

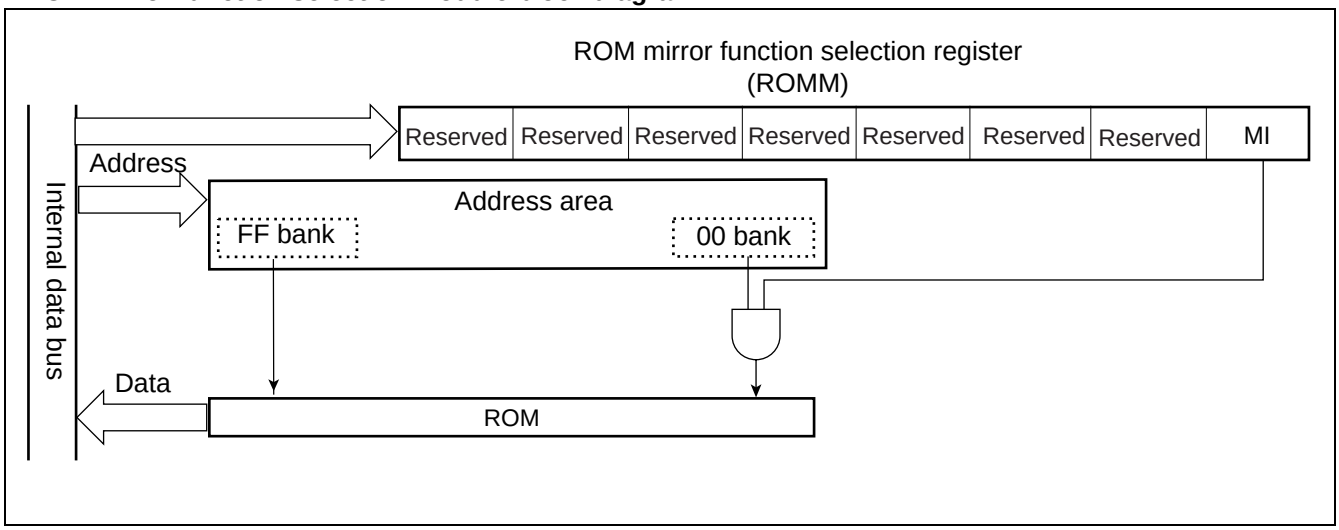


- Address latch
  Retains address value output to internal data bus.
- Address detection control register (PACSR)
  Specifies if interrupt is permitted or prohibited when addresses match with each other.
- Detection address setting (PADR0, PADR1)
  Specifies addresses to be compared with values in address latch.

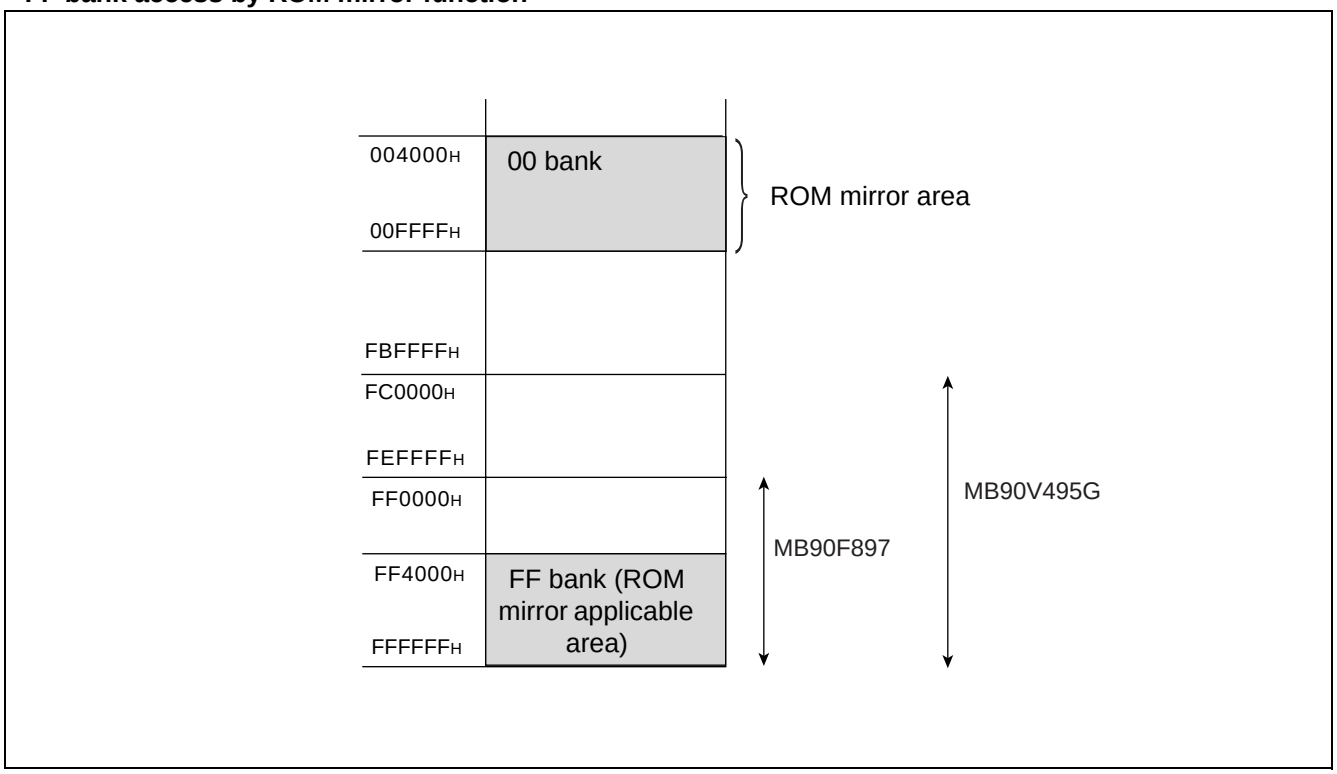
14. ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

• ROM mirror function selection module block diagram



• FF bank access by ROM mirror function



15. 512 Kbit Flash Memory Outline

The following three methods are provided for data writing and deleting on flash memory:

- Parallel writer
- Serial special-purpose writer
- Writing/deleting by program execution

• 512 Kbit flash memory outline

The 512 K-bit flash memory is allocated on FF_H bank of CPU memory map. Using the function of flash memory interface circuit, the memory allows read access and program access from CPU.

The flash memory can be programmed and erased by the instructions from the CPU via the flash memory interface circuit, allowing program code and data to be reprogrammed efficiently even in the on-board state.

Data can be reprogrammed not only by program execution in existing RAM but by program execution in flash memory by dual operation. The different banks (the upper and lower banks) can be used to execute an erase/program and a read concurrently.

• Features of 512 Kbit flash memory

- 64 K words x 8 bits/32 K words x 16 bits (4 K × 4 + 16 K × 2 + 4 K × 4) sector configuration
- Two-bank configuration, enabling simultaneous execution of an erase/program and read.
- Automatic program algorithm (Embedded Algorithm™* : Similar to MBM29LV200.)
- Built-in deletion pause/deletion resume function
- Detection of completed writing/deleting by data polling and toggle bits.
- Detection of completed writing/deleting by CPU interrupt.
- Deletion is allowed on a sector-by-sector basis (sectors are combined freely).
- Number of writing/deleting operations (minimum): 10,000 times
- Flash read cycle time (minimum) : Two machine cycles

* : Embedded Algorithm™ is a registered trademark of Advanced Micro Devices.

Note : A function of reading manufacture code and device code is not provided. These codes are not accessible by command either.

• Flash memory writing/deleting

- A single bank of flash memory cannot be used to program/delete and read at the same time.
- Data can be programmed/deleted into and erased from flash memory by executing either the program residing in the flash memory or the one copied to RAM from the flash memory.

• List of registers and reset values in flash memory

Flash memory control status register (FMCS)

bit	7	6	5	4	3	2	1	0
	0	0	0	X	0	0	0	0

Flash memory write control status register (FMCS)

bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

Flash memory write control status register (FMCS)

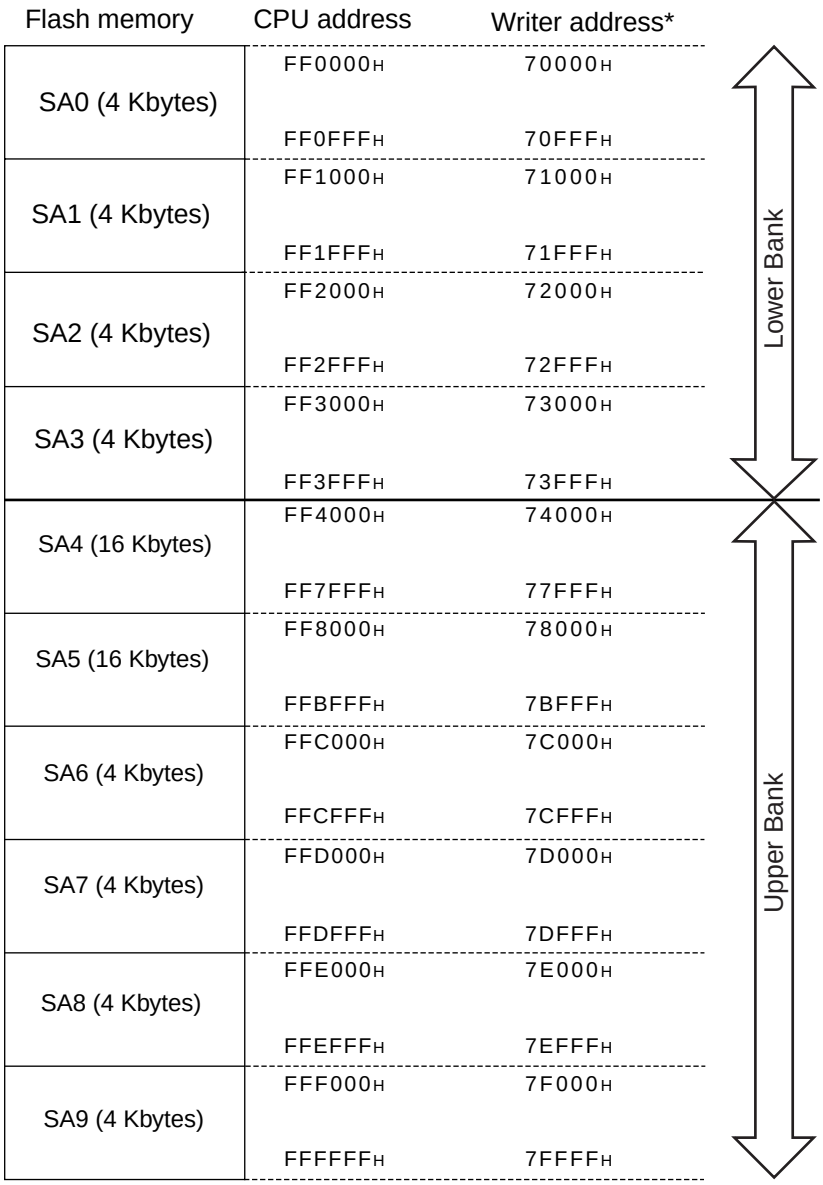
bit	15	14	13	12	11	10	9	8
	0	0	0	0	0	0	0	0

X : Undefined

• **Sector configuration**

For access from CPU, SA0 to SA9 are allocated in FF bank register.

• **Sector configuration of 512 Kbit flash memory**



* : “Writer address” is an address equivalent to CPU address, which is used when data is written on flash memory, using parallel writer. When writing/deleting data with general-purpose writer, the writer address is used for writing and deleting.

■ ELECTRIC CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	$\sum \lvert I_{CLAMP} \rvert$	—	20	mA	*7
“L” level maximum output current	I_{OL1}	—	15	mA	Normal output*4
	I_{OL2}	—	40	mA	High-current output*4
“L” level average output current	I_{OLAV1}	—	4	mA	Normal output*5
	I_{OLAV2}	—	30	mA	High-current output*5
“L” level maximum total output current	$\sum I_{OL1}$	—	125	mA	Normal output
	$\sum I_{OL2}$	—	160	mA	High-current output
“L” level average total output current	$\sum I_{OLAV1}$	—	40	mA	Normal output*6
	$\sum I_{OLAV2}$	—	40	mA	High-current output*6
“H” level maximum output current	I_{OH1}	—	–15	mA	Normal output*4
	I_{OH2}	—	–40	mA	High-current output*4
“H” level average output current	I_{OHAV1}	—	–4	mA	Normal output*5
	I_{OHAV2}	—	–30	mA	High-current output*5
“H” level maximum total output current	$\sum I_{OH1}$	—	–125	mA	Normal output
	$\sum I_{OH2}$	—	–160	mA	High-current output
“H” level average total output current	$\sum I_{OHAV1}$	—	–40	mA	Normal output*6
	$\sum I_{OHAV2}$	—	–40	mA	High-current output*6
Power consumption	P_D	—	297	mW	
Operating temperature	T_A	–40	+105	°C	
		–40	+125	°C	*8
Storage temperature	Tstg	–55	+150	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} =$ 0.0 V.

*2 : AVcc and AVR should not exceed Vcc.

*3 : V_I and V_O should not exceed Vcc + 0.3 V. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : A peak value of an applicable one pin is specified as a maximum output current.

*5 : An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

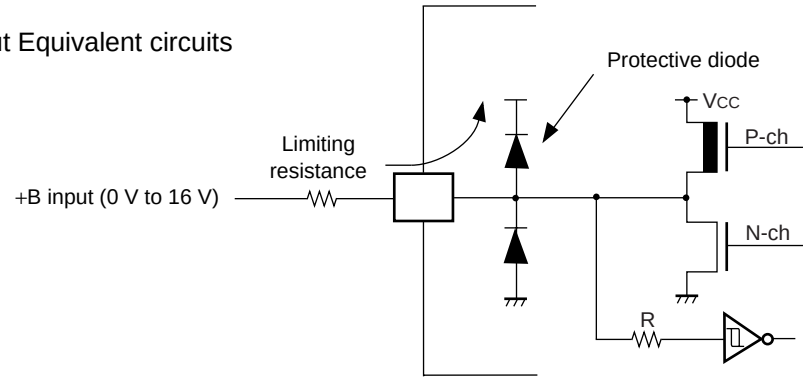
(Continued)

(Continued)

*6 : An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

*7 : • Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35, P36, P37, P40 to P44, P50 to P57
Note: P35 and P36 are MB90F897S only.
• Use within recommended operating conditions.
• Use at DC voltage (current) .
• The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
• The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
• Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
• Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
• Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
• Care must be taken not to leave the +B input pin open.
• Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
• Sample recommended circuits:

• Input/Output Equivalent circuits



*8 : Users considering application exceeding T_A = +105°C are advised to contact their FUJITSU representatives beforehand for reliability limitations.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

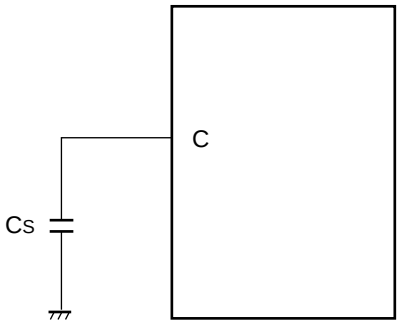
(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.5	5.0	5.5	V	Under normal operation
		3.0	—	5.5	V	Retain status of stop operation
		4.0	—	5.5	V	Accuracy guarantee voltage of A/D converter
Smoothing capacitor	C_S	0.1	—	1.0	µF	*1
Operating temperature	T_A	–40	—	+105	°C	
		–40	—	+125	°C	*2

*1 : Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
Refer to the following figure for connection of smoothing capacitor Cs.

*2 : Users considering application exceeding T_A = +105°C are advised to contact their FUJITSU representatives beforehand for reliability limitations.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	When selected CMOS hysteresis
	V_{IHA}	Automotive input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	When selected Automotive
	V_{IHC}	CMOS input pin (P32, P40)	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	When selected CMOS
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	When selected CMOS hysteresis
	V_{ILA}	Automotive input pin	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	When selected Automotive
	V_{ILC}	CMOS input pin (P32, P40)	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	When selected CMOS
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
"H" level output voltage	V_{OH1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P14 to P17	V_{CC} = 4.5 V, I_{OH} = –14.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P14 to P17	V_{CC} = 4.5 V, I_{OL} = 20.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	All input pins	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	+5	µA	
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 16 MHz, normal operation.	—	25	30	mA	
			V_{CC} = 5.0 V, Internally operating at 16 MHz, writing on flash memory.	—	45	50	mA	MB90F897/S
			V_{CC} = 5.0 V, Internally operating at 16 MHz, deleting on flash memory.	—	45	50	mA	MB90F897/S

* : Test conditions of power supply current are based on a device using external clock.

(Continued)

(Continued)

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

Parameter	Symbol	Pin name	Conditions	Rating			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CCS}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 16 MHz, sleeping.	—	8	12	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internally operating at 2 MHz, transition from main clock mode, in time-base timer mode.	—	0.2	0.35	mA	
	I_{CTSPII}		V_{CC} = 5.0 V, Internally operating at 2 MHz, transition from main clock mode, in time-base timer mode.	—	3	5	mA	
	I_{CCL}		V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock operation, T_A = +25°C	—	40	100	µA	
	I_{CCLS}		V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, T_A = +25°C	—	10	50	µA	
	I_{CCT}		V_{CC} = 5.0 V, Internally operating at 8 kHz, clock mode, T_A = +25°C	—	8	30	µA	
	I_{CCH}		Stopping, T_A = +25°C	—	5	25	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, C, V_{CC}, V_{SS}	—	—	5	15	pF	
Pull-up resistor	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	—	25	50	100	kΩ	FLASH product is not provided with pull-down resistor.

* : Test conditions of power supply current are based on a device using external clock.

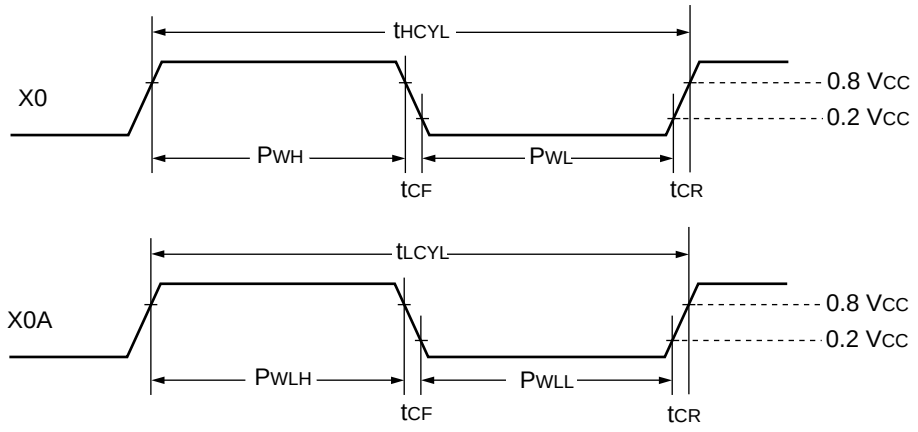
4. AC Characteristics

(1) Clock timing

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

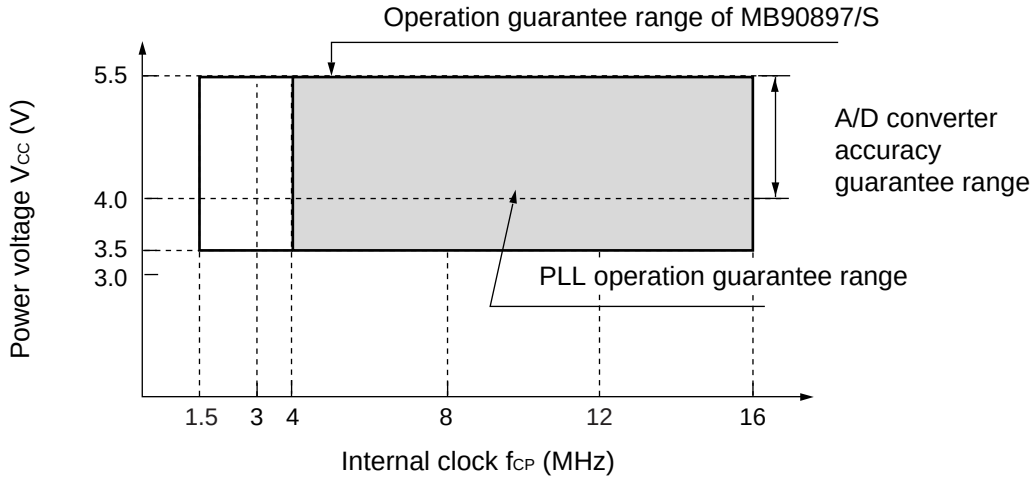
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	8	MHz	When crystal or ceramic resonator is used
			3	—	16	MHz	External clock
			4	—	16	MHz	PLL multipled by 1
			4	—	8	MHz	PLL multipled by 2
			4	—	5.33	MHz	PLL multipled by 3
			4	—	4	MHz	PLL multipled by 4
	f_{CL}	X0A, X1A	—	32.768	—	kHz	MB90F897 only
Clock cycle time	t_{HCYL}	X0, X1	125	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	MB90F897 only
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Set duty factor at 30% to 70% as a guideline.
	P_{WLH},P_{WLL}	X0A	—	15.2	—	µs	MB90F897 only
Input clock rise time and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When external clock is used
Internal operation clock frequency	f_{CP}	—	1.5	—	16	MHz	When main clock is used
	f_{LCP}	—	—	8.192	—	kHz	When sub clock is used, MB90F897 only
Internal operation clock cycle time	t_{CP}	—	62.5	—	666	ns	When main clock is used
	t_{LCP}	—	—	122.1	—	µs	When sub clock is used, MB90F897 only

• Clock timing

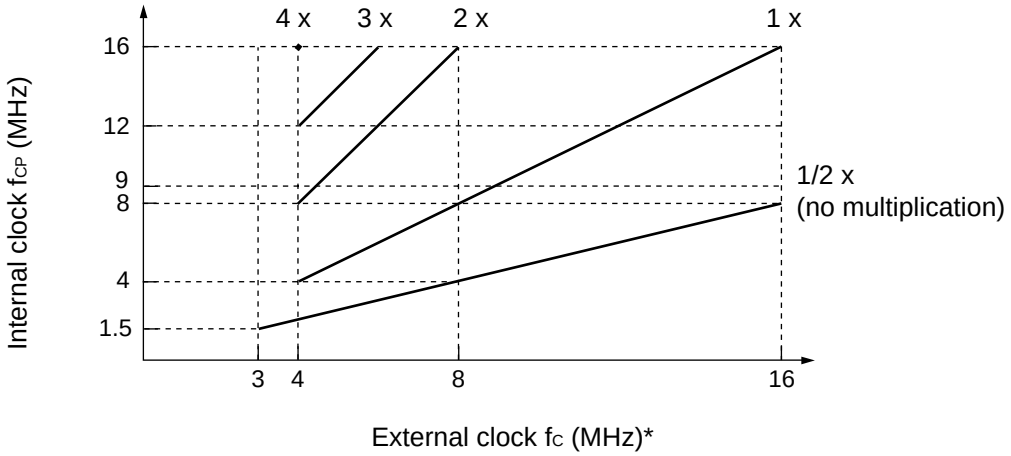


• PLL operation guarantee range

Relation between internal operation clock frequency and power supply voltage



Relation among external clock frequency and internal clock frequency

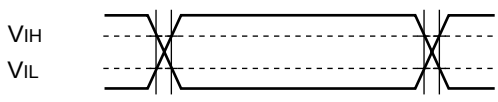


* : fc is 8 MHz at maximum when crystal or ceramic resonator circuit is used.

Rating values of alternating current is defined by the measurement reference voltage values shown below:

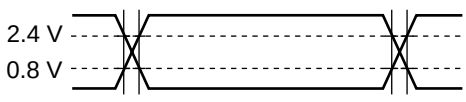
• Input signal waveform

Hysteresis input pin



• Output signal waveform

Output pin



(2) Reset input timing

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

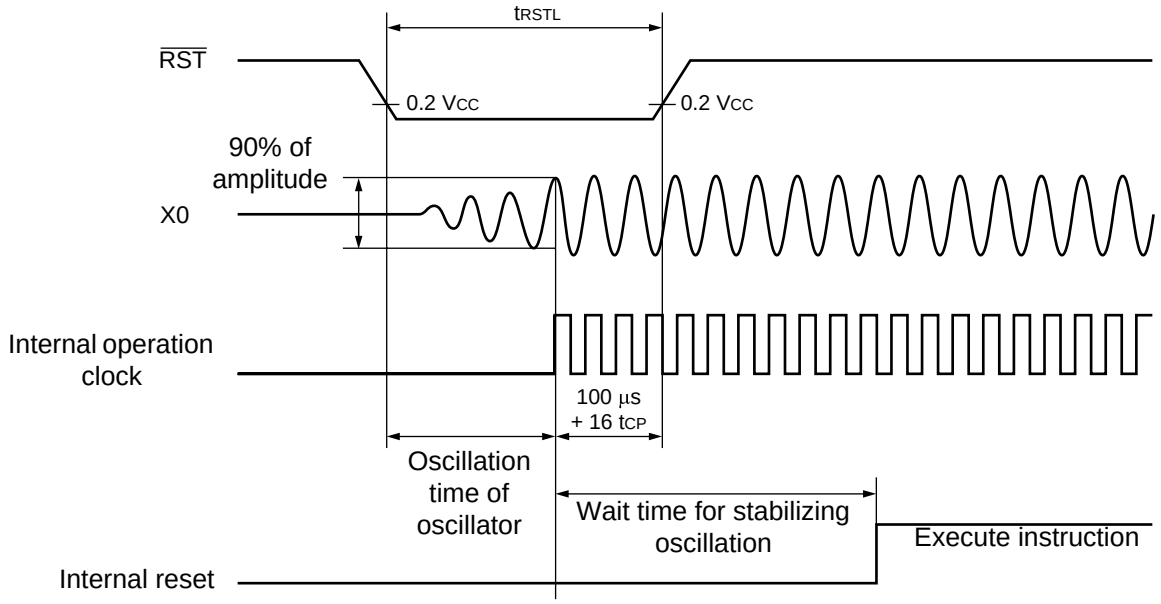
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}*3	—	ns	Normal operation
			Oscillation time of oscillator*1 + 100 µs + 16 t_{CP}*3	—	—	In sub clock*2, sub sleep*2, watch*2 and stop mode
			100	—	µs	In timebase timer

*1 : Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR/ceramic oscillator, the oscillation time is between hundreds of µs to several ms. In the external clock, the oscillation time is 0 ms.

*2 : Except for MB90F387S and MB90387S.

*3 : Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

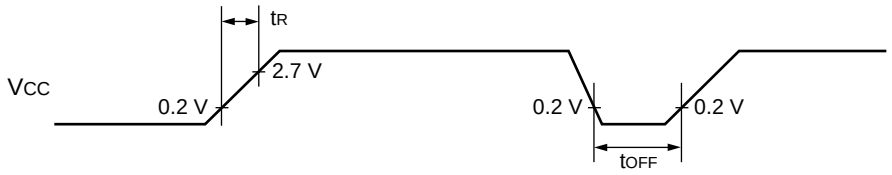
• In sub clock, sub sleep, watch and stop mode



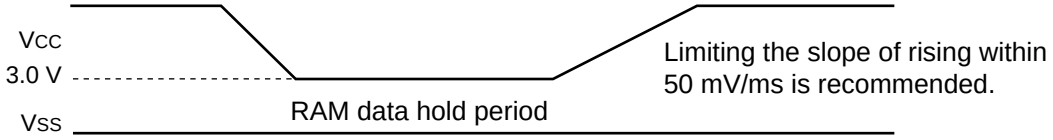
(3) Power-on reset

(V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}	—	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	—	ms	Repeated operation



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.



(4) UART0/UART1 timing

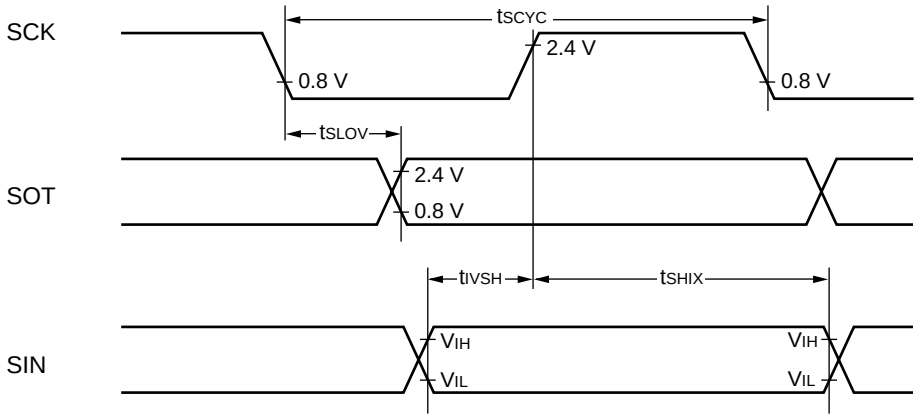
(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0/SCK1	Internal shift clock mode output pin is : C_L = 80 pF+1TTL	8 t_{CP} *	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0/SCK1, SOT0/SOT1		–80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0/SCK1, SIN0/SIN1		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0/SCK1, SIN0/SIN1		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0/SCK1	External shift clock mode output pin is : C_L = 80 pF+1TTL	4 t_{CP} *	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0/SCK1		4 t_{CP} *	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0/SCK1, SOT0/SOT1		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0/SCK1, SIN0/SIN1		60	—	ns	
SCK ↑ →valid SIN hold time	t_{SHIX}	SCK0/SCK1, SIN0/SIN1		60	—	ns	

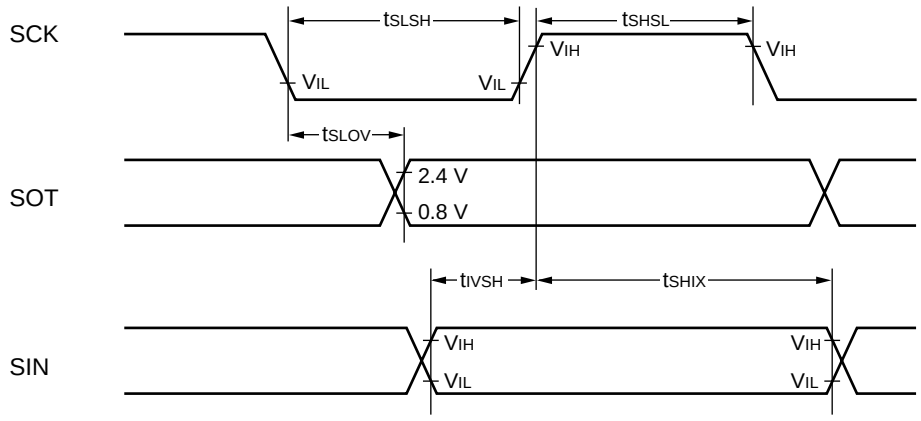
* : Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

Notes: • AC rating in CLK synchronous mode.
• C_L is a load capacitance value on pins for testing.

• Internal shift clock mode



• External shift clock mode



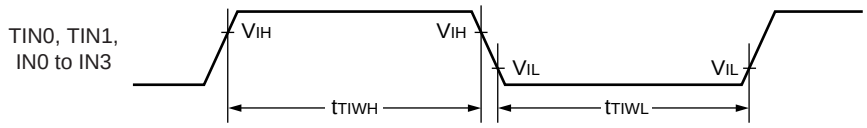
(5) Timer input timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP} *	—	ns	
	t_{TIWL}	IN0 to IN3					

* : Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

• Timer input timing



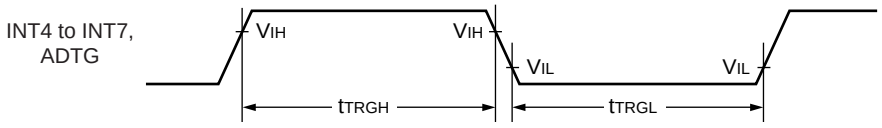
(6) Trigger input timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT4 to INT7, ADTG	—	3 t_{CP} *	—	ns	

* : Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

• Trigger input timing



5. A/D converter

(V_{CC} = AV_{CC} = 5.0 V ± 10 %, 3.0 V ≤ AVR − AV_{SS}, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +125 °C)

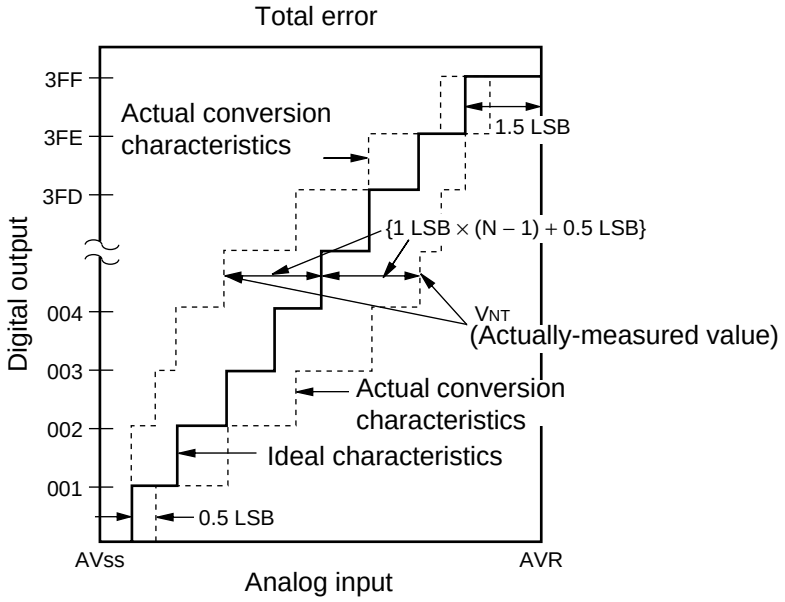
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinear error	—	—	—	—	± 2.5	LSB	
Differential linear error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = AVR/1024
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR − 3.5 LSB	AVR − 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	—	—	66 t_{CP} *1	—	—	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			88 t_{CP} *1	—	—	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Sampling time	—	—	32 t_{CP} *1	—	—	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			128 t_{CP} *1	—	—	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVR	V	
Reference voltage	—	AVR	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*2
Reference voltage supplying current	I_R	AVR	—	165	250	µA	
	I_{RH}	AVR	—	—	5	µA	*2
Variation among channels	—	AN0 to AN7	—	—	4	LSB	

*1 : Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

*2 : If A/D converter is not operating, a current when CPU is stopped is applicable (Vcc=AVcc=AVR=5.0 V).

6. Definition of A/D Converter Terms

Resolution	: Analog variation that is recognized by an A/D converter.
Linear error	: Deviation between a line across zero-transition line (“00 0000 0000” ←→“00 0000 0001”) and full-scale transition line (“11 1111 1110” ←→ “11 1111 1111”) and actual conversion characteristics.
Differential linear error	: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	: Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVR - AV_{SS}}{1024}\ [\text{V}]$$

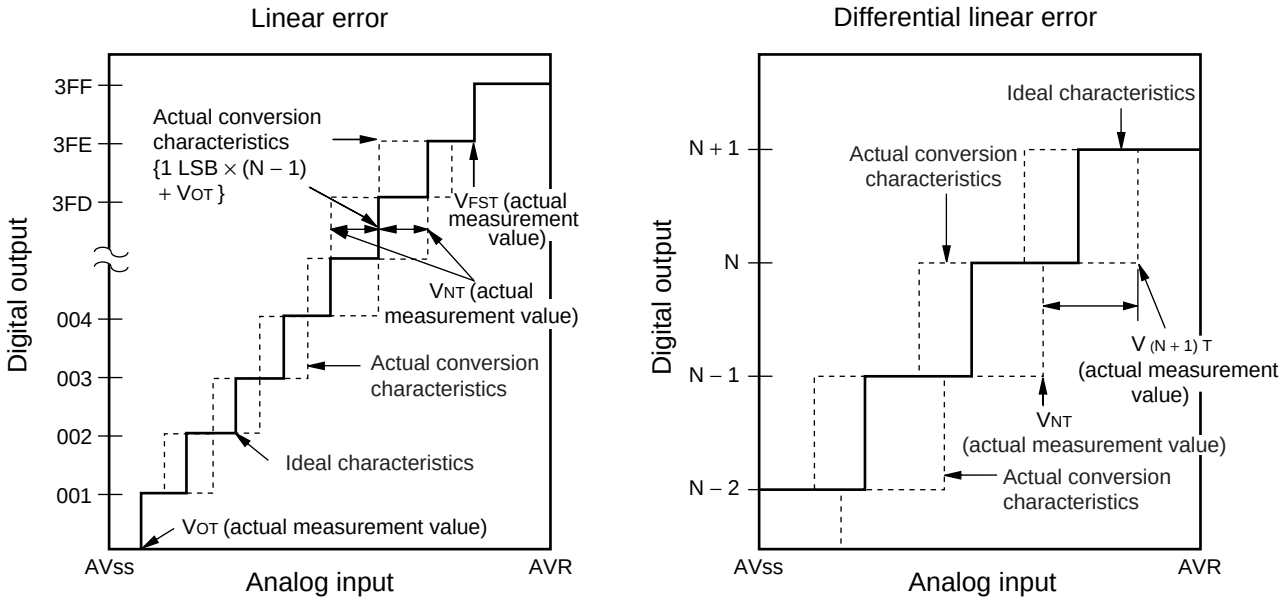
V_{OT} (Ideal value) $= AV_{SS} + 0.5$ LSB [V]

V_{FST} (Ideal value) $= AVR - 1.5$ LSB [V]

V_{NT} : A voltage at which digital output transits from (N-1) to N.

(Continued)

(Continued)



$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

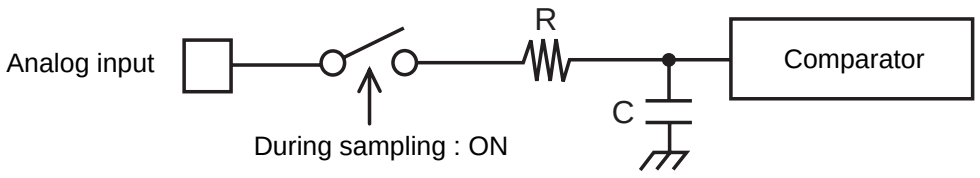
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

7. Notes on A/D Converter Section

<About the external impedance of the analog input and its sampling time>

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model



MB90F897/F897S	R	C
4.5 V ≤ AV_{CC} ≤ 5.5 V	2.4 kΩ (Max)	36.4 pF (Max)
4.0 V ≤ AV_{CC} < 4.5 V	16.4 kΩ (Max)	36.4 pF (Max)

Note : The values are reference values.

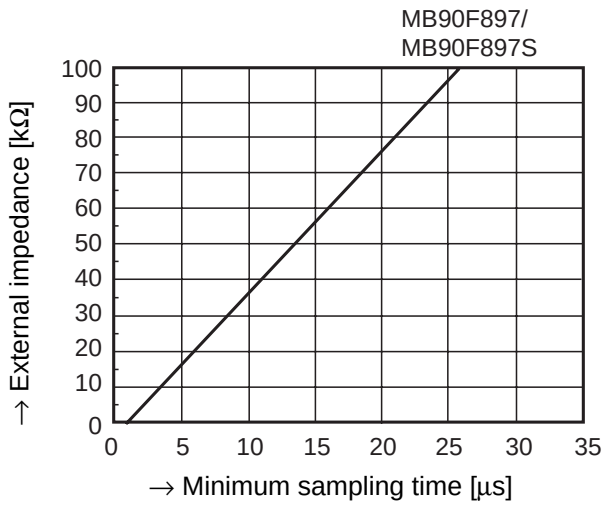
(Continued)

(Continued)

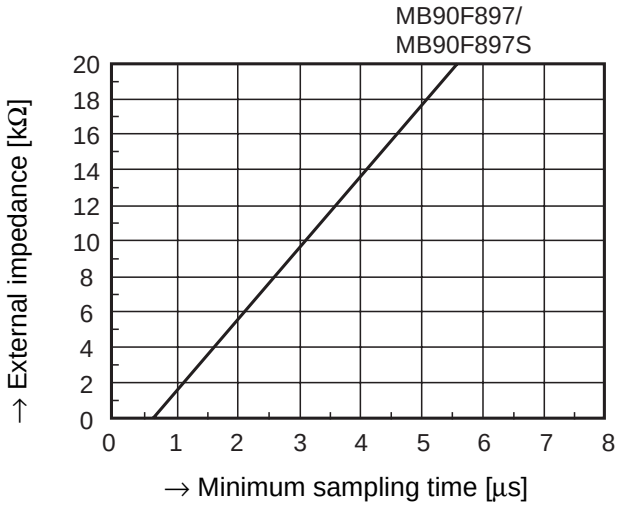
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

(At 4.5 V ≤ AV_{CC} ≤ 5.5 V)

[External impedance = 0 kΩ to 100 kΩ]

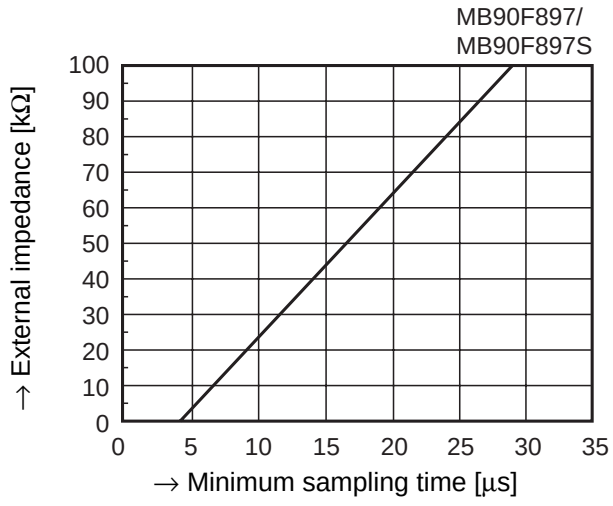


[External impedance = 0 kΩ to 20 kΩ]

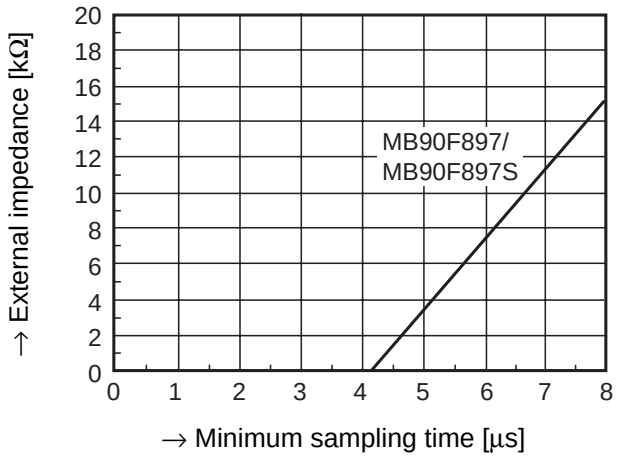


(At 4.0 V ≤ AV_{CC} < 4.5 V)

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]



The relationship between the external impedance and minimum sampling time

- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

<About errors>

- As |AVR – AVss| become smaller, values of relative errors grow larger.

8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 KB sector)	T_A = + 25 °C, V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes 00_H programming prior to erasure
Sector erase time (16 KB sector)		—	0.5	7.5	s	Excludes 00_H programming prior to erasure
Chip erase time		—	2.6	—	s	Excludes 00_H programming prior to erasure
Word (16 bit width) programming time		—	16	3,600	µs	Except for the over head time of the system
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Data Retention Time	Average T_A = + 85 °C	20	—	—	Years	*

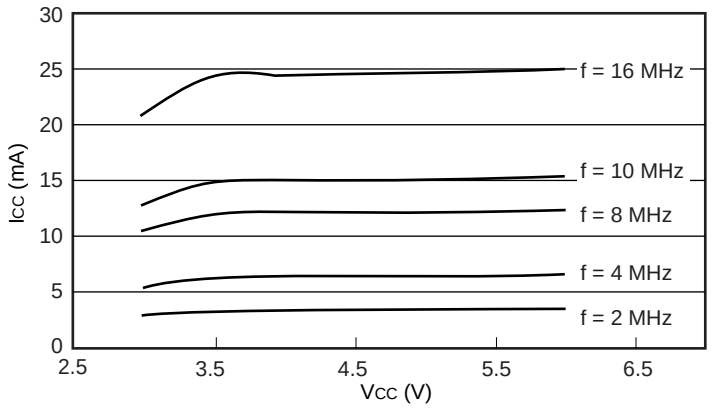
* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

■ EXAMPLE CHARACTERISTICS

• MB90F897

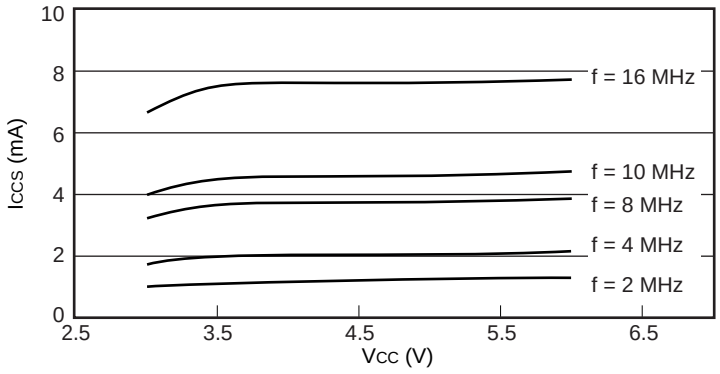
$I_{CC} - V_{CC}$

T_A = +25 °C, In external clock operation
f = Internal operating frequency



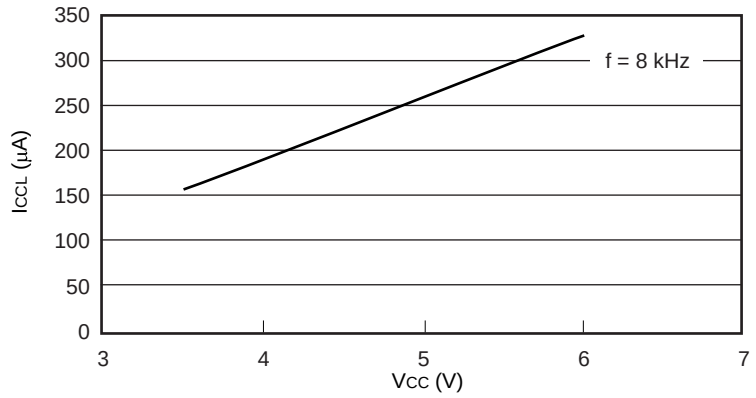
$I_{CCS} - V_{CC}$

T_A = +25 °C, In external clock operation
f = Internal operating frequency



$I_{CCL} - V_{CC}$

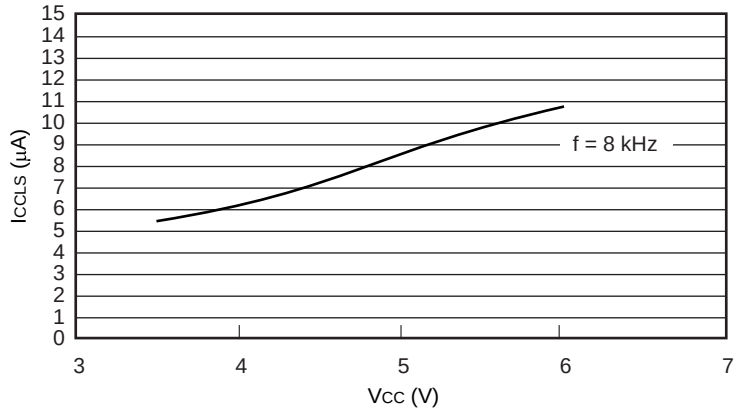
T_A = +25 °C, In external clock operation
f = Internal operating frequency



(Continued)

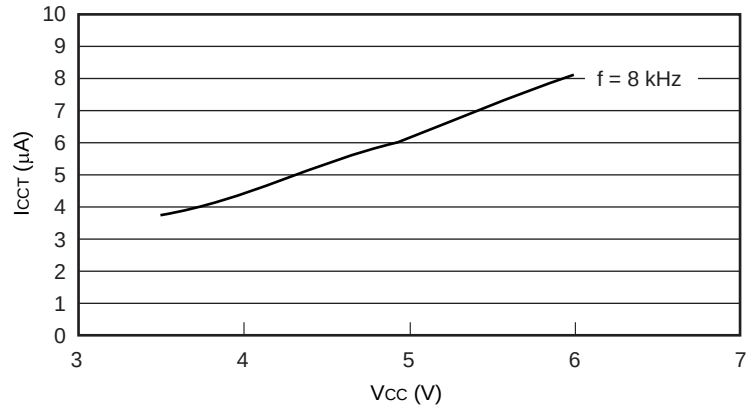
I_{CCLS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



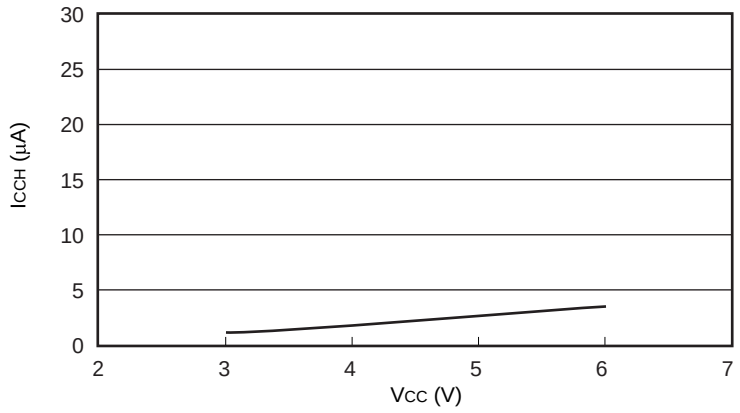
I_{CCT} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCH} – V_{CC}

Stopping, T_A = +25 °C



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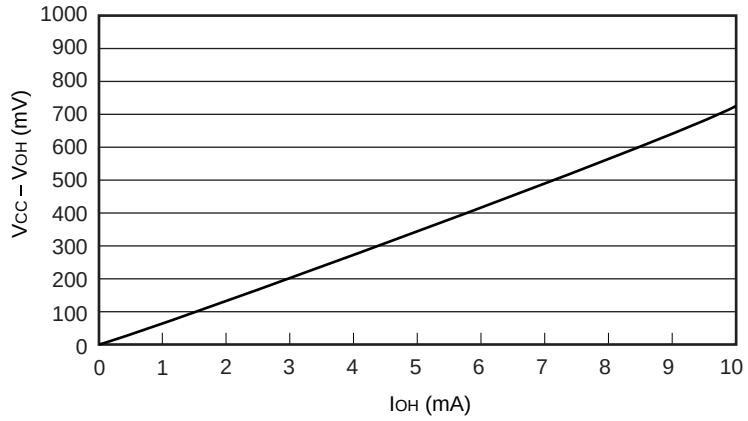
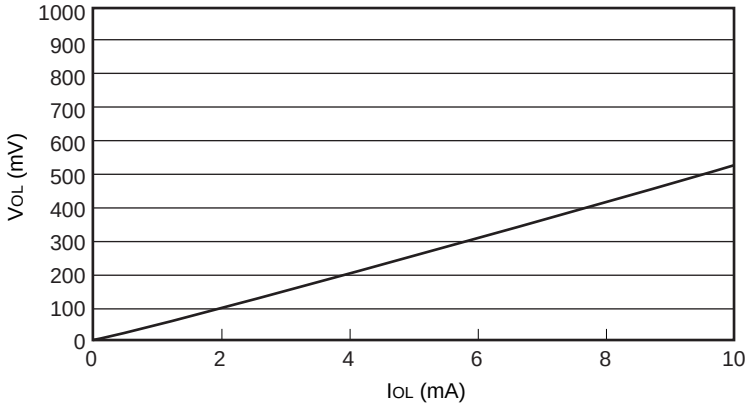
$(V_{CC} - V_{OH})$ – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



V_{OL} – I_{OL}

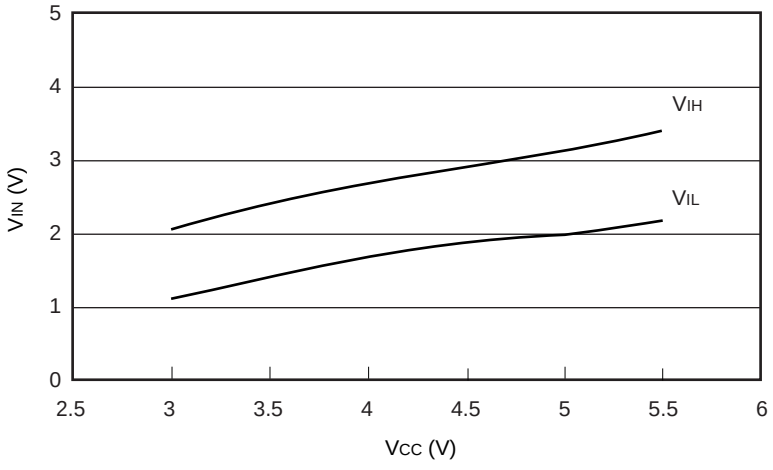
T_A = +25 °C, V_{CC} = 4.5 V



“H” level input voltage/ “L” level input voltage

V_{IN} – V_{CC}

T_A = +25 °C



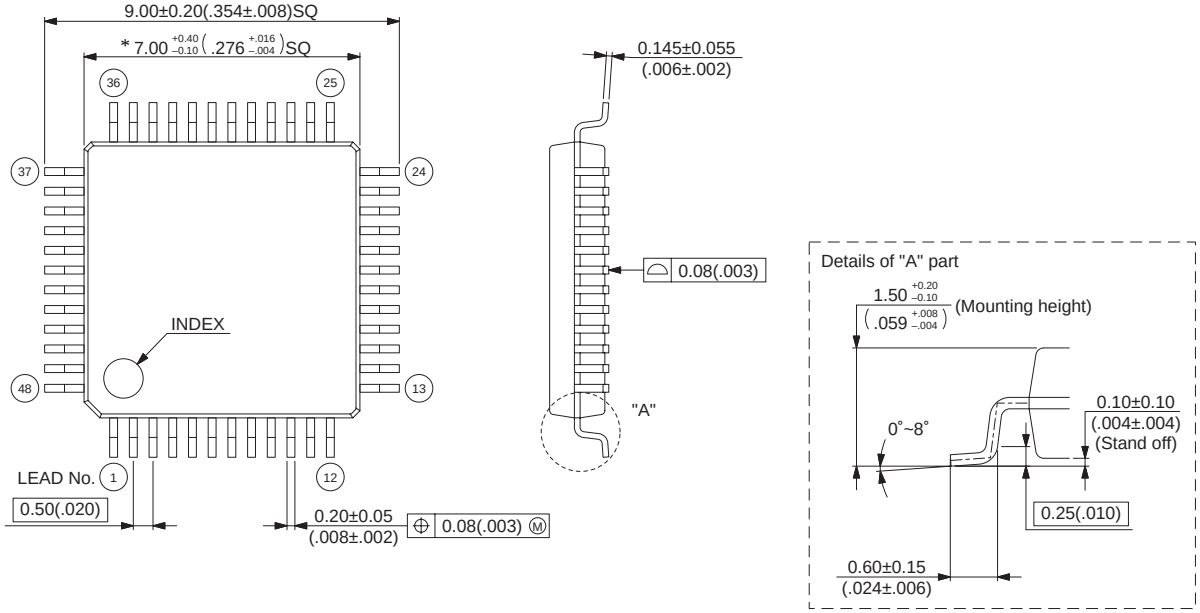
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F897PMT MB90F897SPMT	48-pin plastic LQFP (FPT-48P-M26)	

■ PACKAGE DIMENTION

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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