FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00010-2v0-E

Memory FRAM

16 K (2 K × 8) Bit I²C

MB85RC16V

■ DESCRIPTION

The MB85RC16V is an FRAM (Ferroelectric Random Access Memory) chip in a configuration of 2,048 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

Unlike SRAM, the MB85RC16V is able to retain data without using a data backup battery.

The memory cells used in the MB85RC16V have at least 10^{10} Read/Write operation endurance per bit, which is a significant improvement over the number of read and write operations supported by other nonvolatile memory products.

The MB85RC16V can provide writing in one byte units because the long writing time is not required unlike Flash memory and E²PROM. Therefore, the writing completion waiting sequence like a write busy state is not required.

■ FEATURES

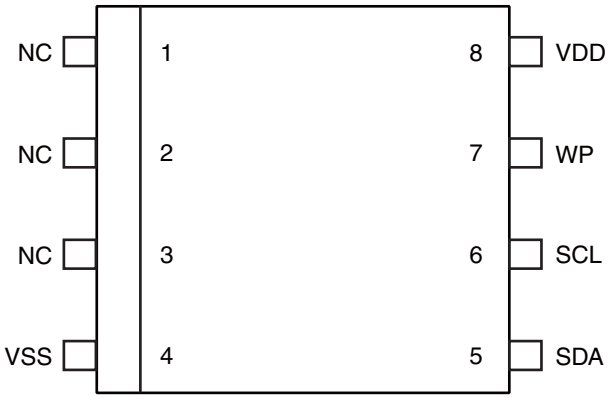
- Bit configuration : 2,048 words × 8 bits
- Operating power supply voltage : 3.0 V to 5.5 V
- Operating frequency : 400 kHz (Max)
- Two-wire serial interface : Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating temperature range : − 40 °C to + 85 °C
- Data retention : 10 years (+ 85 °C)
- Read/Write endurance : 10^{10} times
- Package : Plastic / SOP, 8-pin (FPT-8P-M02)
- Low power consumption : Operating current 80 μA (Max: @400 kHz), Standby current 5 μA (Typ)

2011.10

FUJITSU

■ PIN ASSIGNMENT

(TOP VIEW)

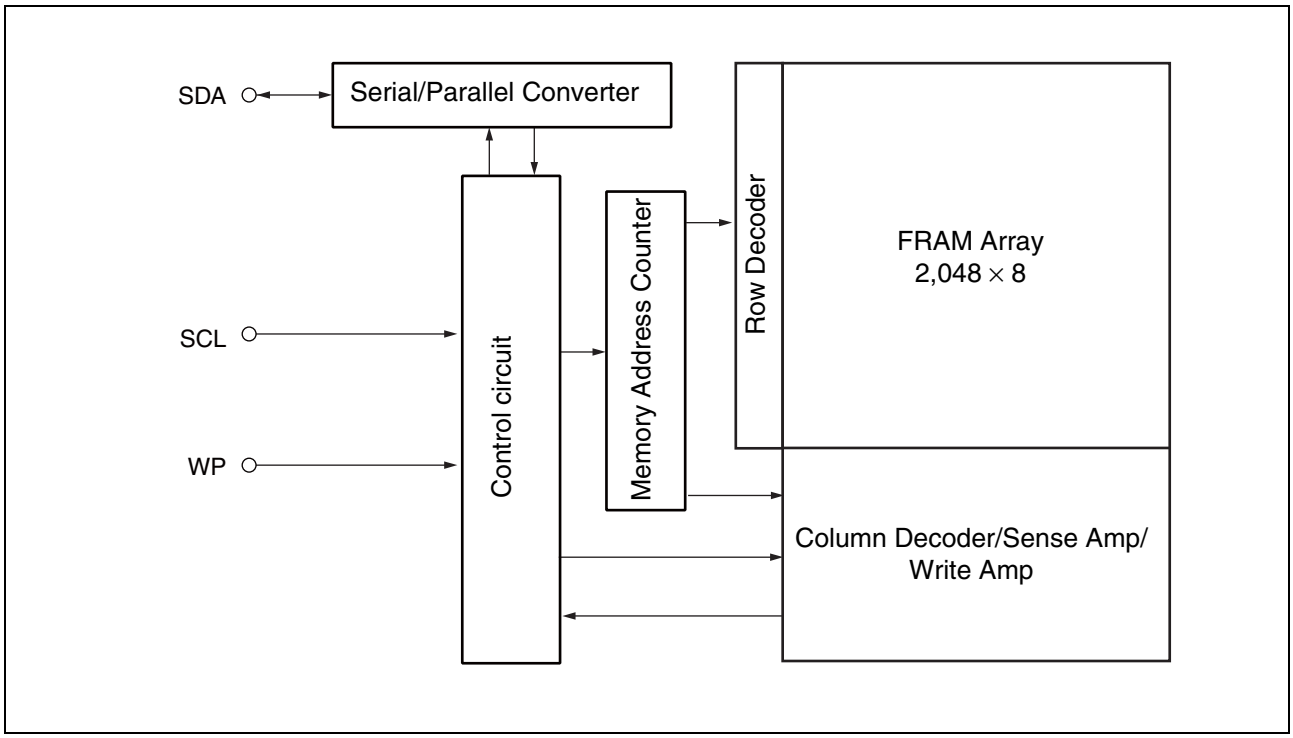


(FPT-8P-M02)

■ PIN FUNCTIONAL DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 3	NC	No Connect pins Leave it unconnected.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin of serial data for performing bidirectional communication of memory address and writing or reading data. It is possible to connect some devices. It is an open drain output, so a pull-up resistance is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output timing serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When Write Protect pin is “H” level, writing operation is disabled. When Write Protect pin is “L” level, the entire memory region can be overwritten. Reading operation is always enabled regardless of the Write Protect pin state. The write protect pin is internally pulled down to the VSS pin and that is recognized as the “L” level (write enabled) when the pin is the open state.
8	VDD	Supply Voltage pin

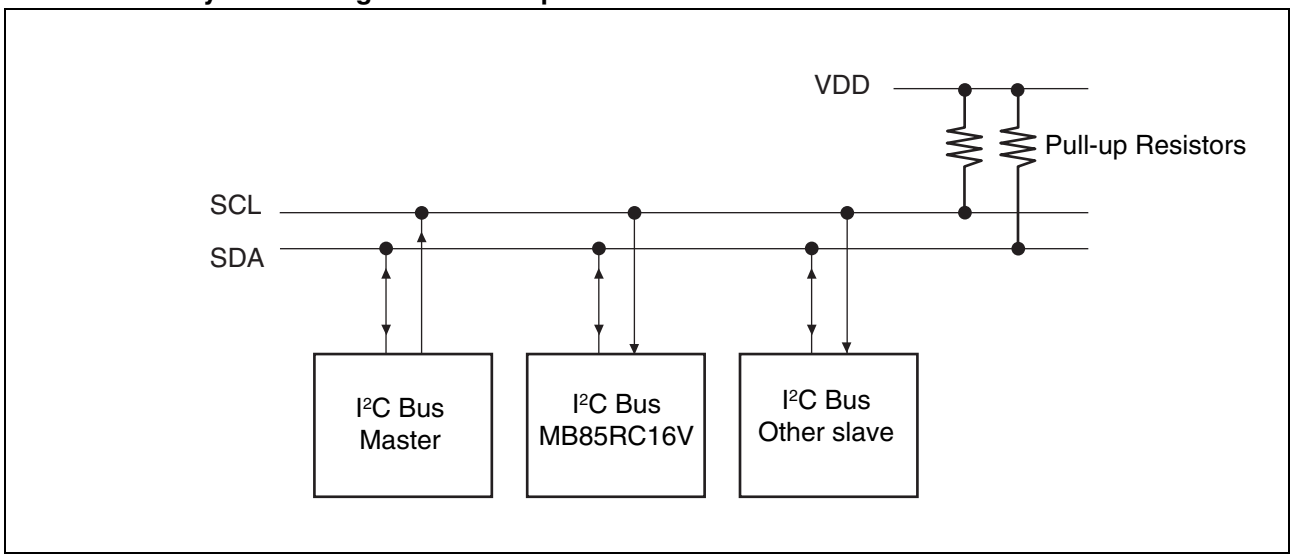
■ BLOCK DIAGRAM



■ I²C (Inter-Integrated Circuit)

The MB85RC16V has the two-wire serial interface and the I²C bus, and operates as a slave device.
The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, a I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration.

• I²C Interface System Configuration Example



■ I²C COMMUNICATION PROTOCOL

The I²C bus provides communication by two wires only, therefore, the SDA input should change while SCL is the “L” level. However, when starting and stopping the communication sequence, SDA is allowed to change while SCL is the “H” level.

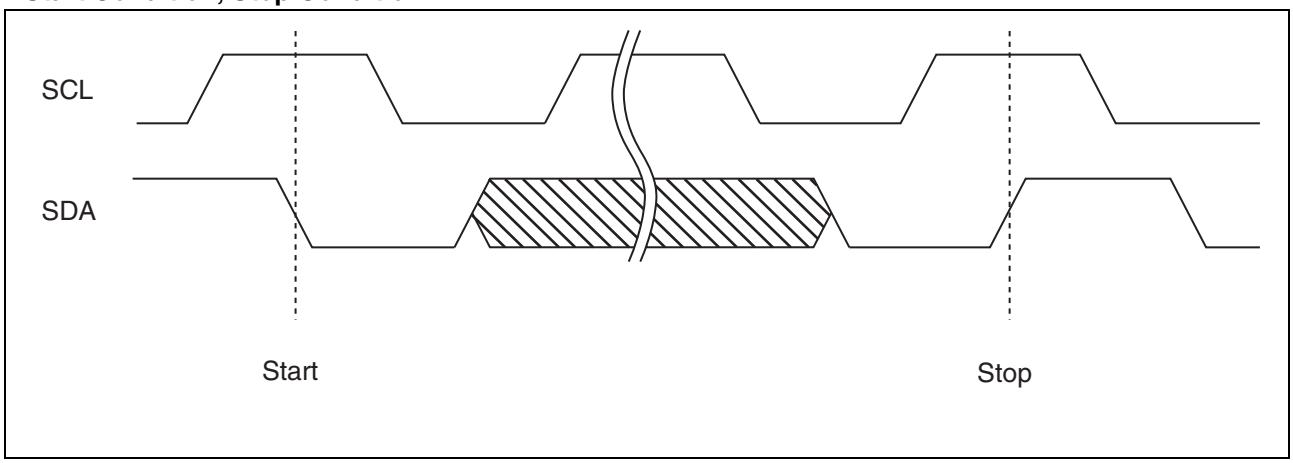
- Start Condition

To start read or write operations by the I²C bus, change the SDA input from the “H” level to the “L” level while the SCL input is in the “H” level.

- Stop Condition

To stop the I²C bus communication, change the SDA input from the “L” level to the “H” level while the SCL input is in the “H” level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data and enters the standby state.

• Start Condition, Stop Condition



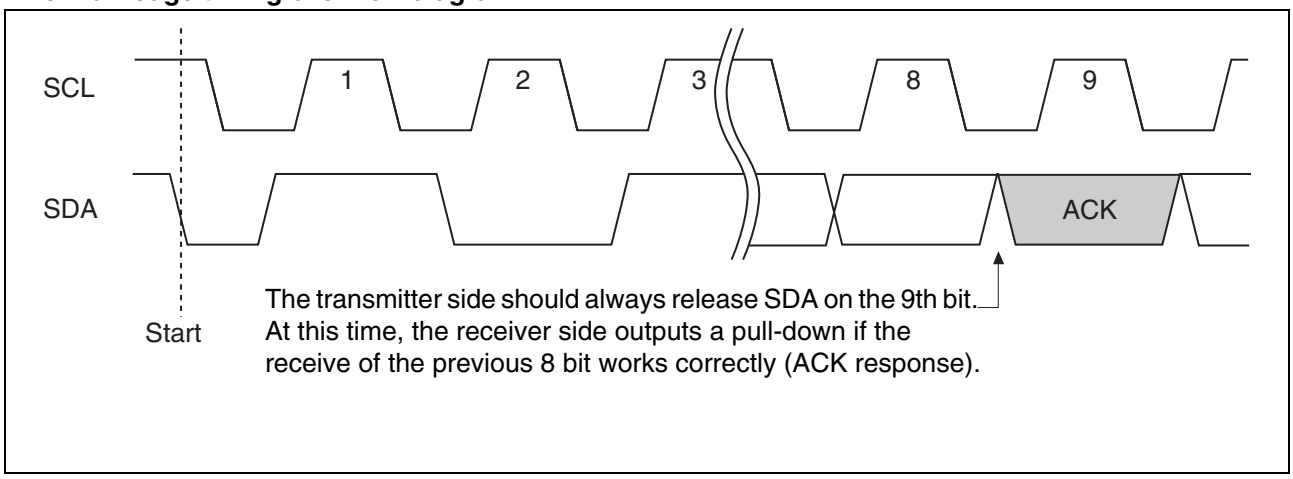
Note : The FRAM device does not need the programming wait time (t_{WC}) after issuing the Stop Condition during the write operation.

■ ACKNOWLEDGE (ACK)

In the I²C bus, serial data including memory address or memory information is sent in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the “L” level every time on the 9th SCL clock after every 8 bits are successfully transmitted. On the transmitter side, the bus is temporarily released on this 9th clock to allow the acknowledge signal to be received and checked. During this released period, the receiver side pulls the SDA line down to indicate that the communication works correctly.

If the receiver side receives the stop condition before transmitting the acknowledge “L” level, the read operation ends and the I²C bus enters the standby state. If the acknowledge “L” level is not detected, and the Stop condition is not sent, the bus remains in the released state without doing anything.

• Acknowledge timing overview diagram



■ MEMORY ADDRESS STRUCTURE

The MB85RC16V has the memory address buffer to store the 11-bit information for the memory address.

As for byte write, page write and random read commands, the complete 11-bit memory address is configured by inputting the memory upper address (3 bits) and the memory lower address (8 bits), and saving to the memory address buffer and access to the memory is performed.

As for a current address read command, the complete 11-bit memory address is configured by inputting the memory upper address (3 bits) and by the memory address lower 8-bit which has saved in the memory address buffer, and saving to the memory address buffer and access to the memory is performed.

■ DEVICE ADDRESS WORD

Following the start condition, the 8 bit device address word is input. Inputting the device address word decides whether the master or the slave drives the data line. However, the clock is always driven by the master. The device address word (8bits) consists of a device Type code (4bits), memory upper address code (3bits), and a Read/Write code (1bit).

- Device Type Code (4bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at “1010” for the MB85RC16V.

- Memory Upper Address Code (3bits)

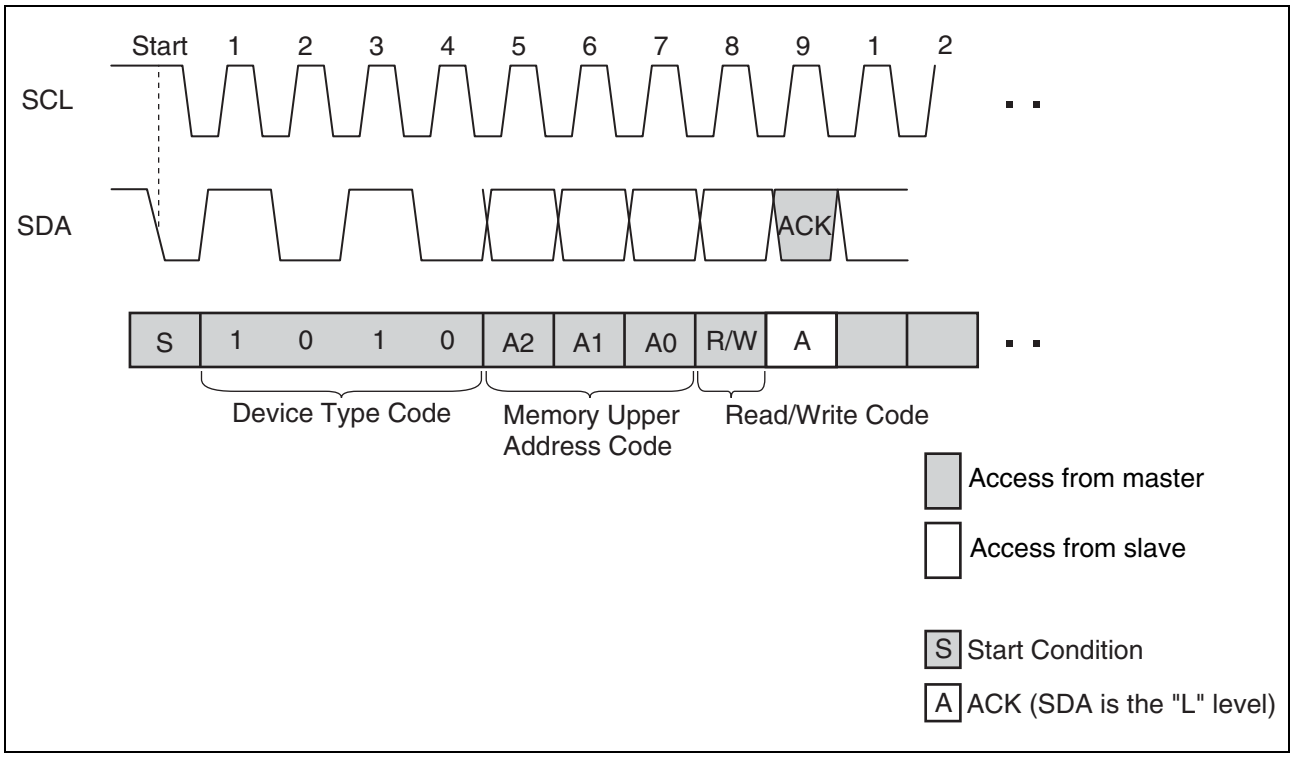
Following the device type code, the 3 bits of the memory upper address code are input.

The slave address selection is not performed by the external pin setting on this device. These 3 bits are not the setting bits for the slave address, but the upper 3-bit setting bits for the memory address.

- Read/Write Code (1bit)

The 8th bit of the device address word is the R/W (Read/Write) code. When the R/W code is “0” input, a write operation is enabled, and the R/W code is “1” input, a read operation is enabled for the MB85RC16V. If the device code is not “1010”, the Read/Write operation is not performed and the standby state is chosen.

• Device Address Word



■ DATA STRUCTURE

The master inputs the device address word (8 bits) following the start condition, and then the slave outputs the Acknowledge “L” level on the ninth bit. After confirming the Acknowledge response, the sequential 8-bit memory lower address is input, to the byte write, page write and random read commands.

As for the current address read command, inputting the memory lower address is not performed, and the address buffer lower 8-bit is used as the memory lower address.

When inputting the memory lower address finishes, the slave outputs the Acknowledge “L” level on the ninth bit again.

Afterwards, the input and the output data continue in 8-bit units, and then the Acknowledge “L” level is output for every 8-bit data.

■ FRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC16V performs the high speed write operations, so any waiting time for an ACK* by the acknowledge polling does not occur.

*: In Flash memory and E²PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

■ WRITE PROTECT (WP)

The entire memory array can be write protected by setting the WP pin to the “H” level. When the WP pin is set to the “L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

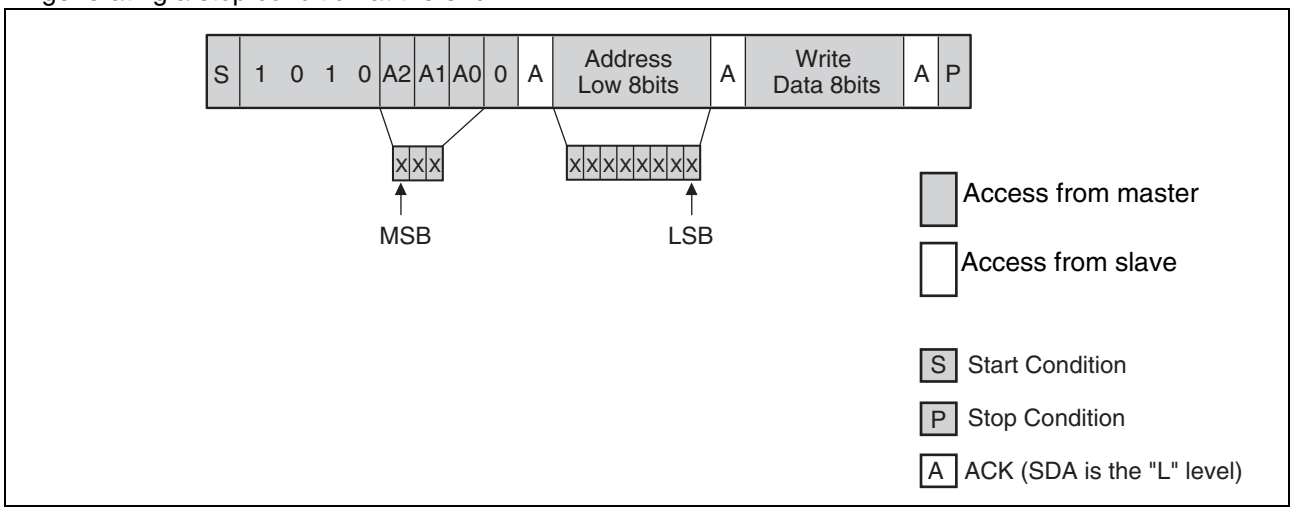
Do not change the WP signal level during the communication period from the start condition to the stop condition.

Note : The WP pin is pulled down internally to the VSS pin, therefore if the WP pin is open, the pin status is recognized as the “L” level (write enabled).

■ COMMAND

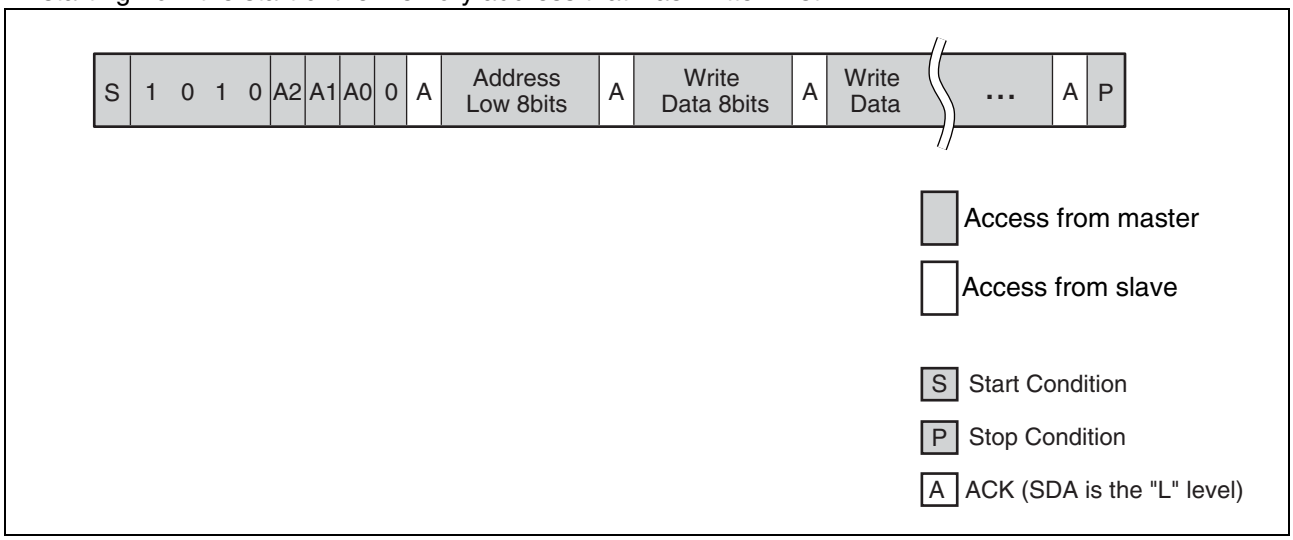
• Byte Write

If the device address word (R/W “0” input) is sent after the start condition, an ACK responds from the slave. After this ACK, write memory addresses and write data are sent in the same way, and the write ends by generating a stop condition at the end.



• Page Write

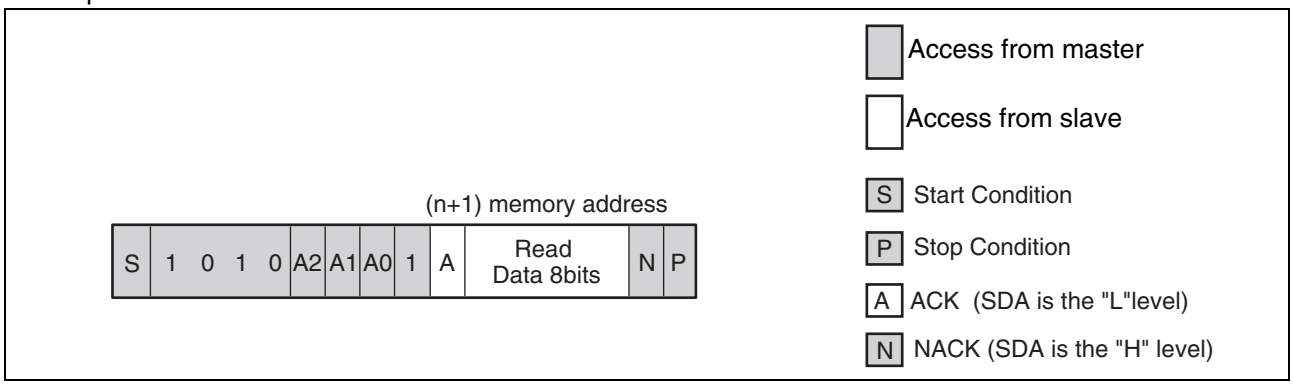
If data is continuously sent after the following address when the same command (expect stop condition) as Byte Write was sent, a page write is performed. The memory address rolls over to first memory address (000_H) at the end of the address. Therefore, if more than 2 Kbytes are sent, the data is overwritten in order starting from the start of the memory address that was written first.



• Current Address Read

If the last write or read operation finishes correctly up to the end of stop condition, the memory address that was accessed last remains in the memory address buffer (the length is 11 bits).

When sending this command without turning the power off, it is possible to read from the memory address n+1 which adds 1 to the total 11-bit memory address n, which consists of the memory upper address 3-bit from the device address word input and the lower 8-bit of the memory address buffer. If the memory address n is the last address, it is possible to read with rolling over to the head of the memory address (000_H). The current address (address that the memory address buffer indicates) is undefined immediately after turning the power on.

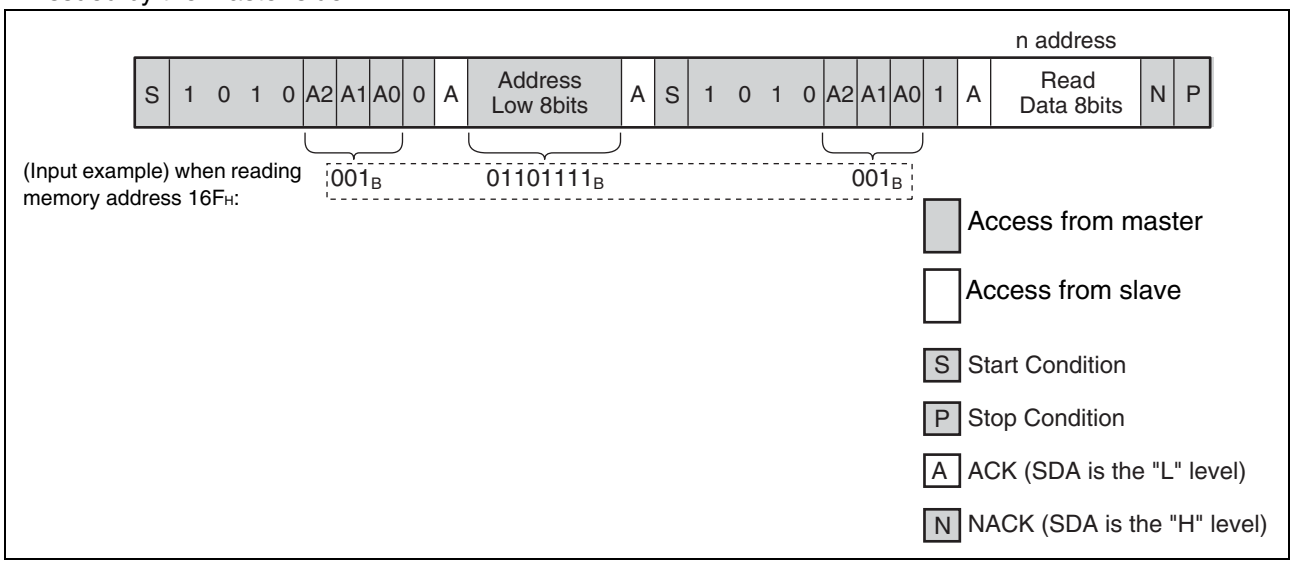


• Random Read

After specifying the address as well as for write system command, issuing another start condition, by transmitting Device Address Word (R/W “1” input), the one byte data from the memory address saved in the memory address buffer can be read synchronously to SCL.

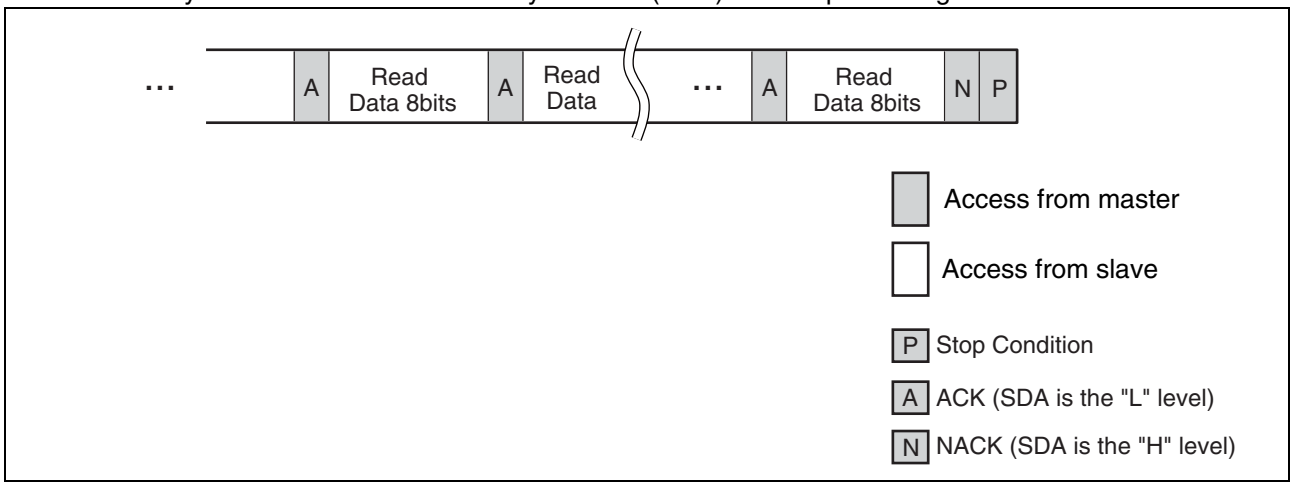
Setting values for the first and the second memory upper address codes should be the same (The figure below shows the input example).

The final NACK (SDA is the “H” level) is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



• Sequential Read

Data can be received continuously following the Device address word (R/W “1” input) after specifying the address in the same way as for Random Read. If the read reaches the end of address, the read address automatically rolls over to the first memory address (000_H) and keeps reading.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 6.0	V
Input voltage*	V_{IN}	− 0.5	V_{DD} + 0.5 (≤ 6.0)	V
Output voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5 (≤ 6.0)	V
Ambient temperature	T_A	− 40	+ 85	°C
Storage temperature	T_{STG}	− 40	+ 125	°C

*: These parameters are based on the condition that Vss is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*	V_{DD}	3.0	—	5.5	V
“H” level input voltage*	V_{IH}	$V_{DD} \times 0.8$	—	5.5	V
“L” level input voltage*	V_{IL}	V_{SS}	—	$V_{DD} \times 0.2$	V
Ambient temperature	T_A	− 40	—	+ 85	°C

*: These parameters are based on the condition that Vss is 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	—	—	1	µA
Output leakage current*2	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}	—	—	1	µA
Operating power supply current	I_{CC}	SCL = 400 kHz	—	40	80	µA
Standby current	I_{SB}	SCL, SDA = V_{DD} WP = 0V or V_{DD} or OPEN T_A = +25 °C in stop condition	—	5	10	µA
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
Input resistance for WP pin	R_{IN}	V_{IN} = V_{IL} (Max)	50	—	—	kΩ
		V_{IN} = V_{IH} (Min)	1	—	—	MΩ

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

2. AC Characteristics

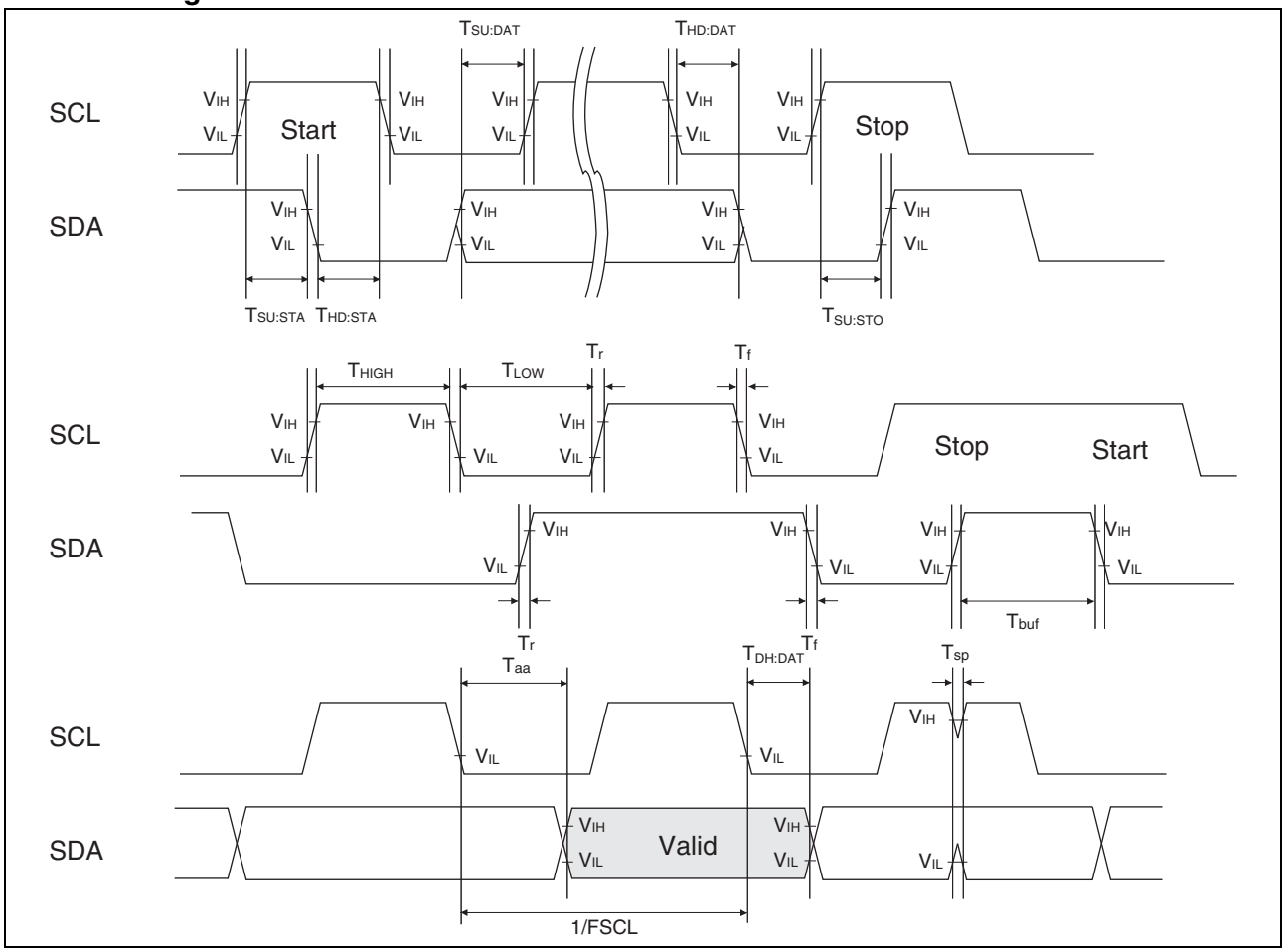
(within recommended operating conditions)

Parameter	Symbol	Value				Unit
		STANDARD MODE		FAST MODE		
		Min	Max	Min	Max	
SCL clock frequency	FSCL	0	100	0	400	kHz
Clock high time	T_{HIGH}	4.0	—	0.6	—	µs
Clock low time	T_{LOW}	4.7	—	1.3	—	µs
SCL/SDA rise time	T_r	—	1000	—	300	ns
SCL/SDA fall time	T_f	—	300	—	300	ns
Start condition hold	$T_{HD:STA}$	4.0	—	0.6	—	µs
Start condition setup	$T_{SU:STA}$	4.7	—	0.6	—	µs
SDA input hold	$T_{HD:DAT}$	0	—	0	—	ns
SDA input setup	$T_{SU:DAT}$	250	—	100	—	ns
SDA output hold	$T_{DH:DAT}$	0	—	0	—	ns
Stop condition setup	$T_{SU:STO}$	4.0	—	0.6	—	µs
SDA output access after SCL fall	T_{AA}	—	3	—	0.9	µs
Pre-charge time	T_{BUF}	4.7	—	1.3	—	µs
Noise suppression time constant on SCL, SDA	T_{SP}	—	50	—	50	ns

AC characteristics were measured under the following measurement conditions.

Power supply voltage : 3.0 V to 5.5 V
Operating temperature : – 40 °C to + 85 °C
Input voltage amplitude : $V_{DD} \times 0.2$ to $V_{DD} \times 0.8$
Input rise time : 5 ns
Input fall time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

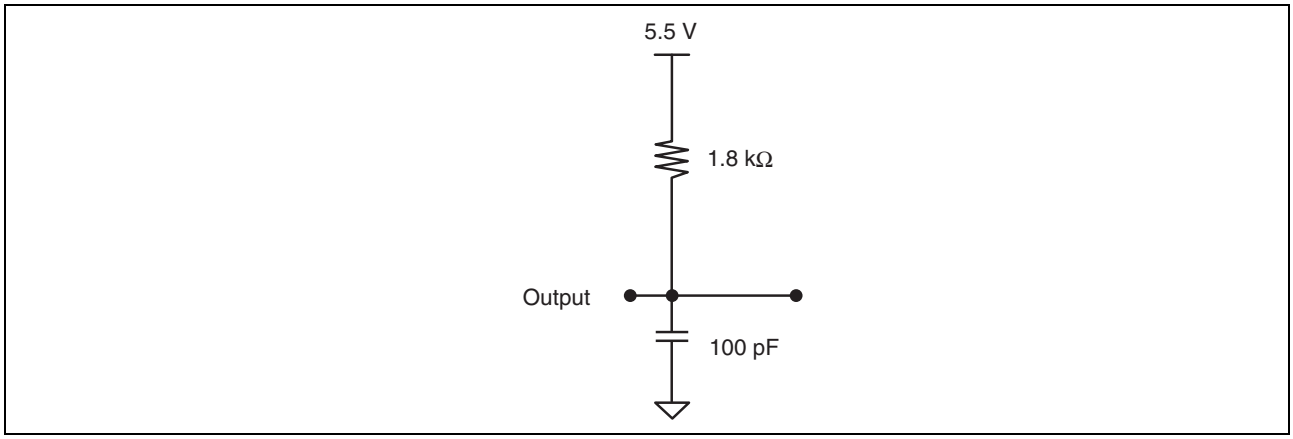
3. AC Timing Definitions



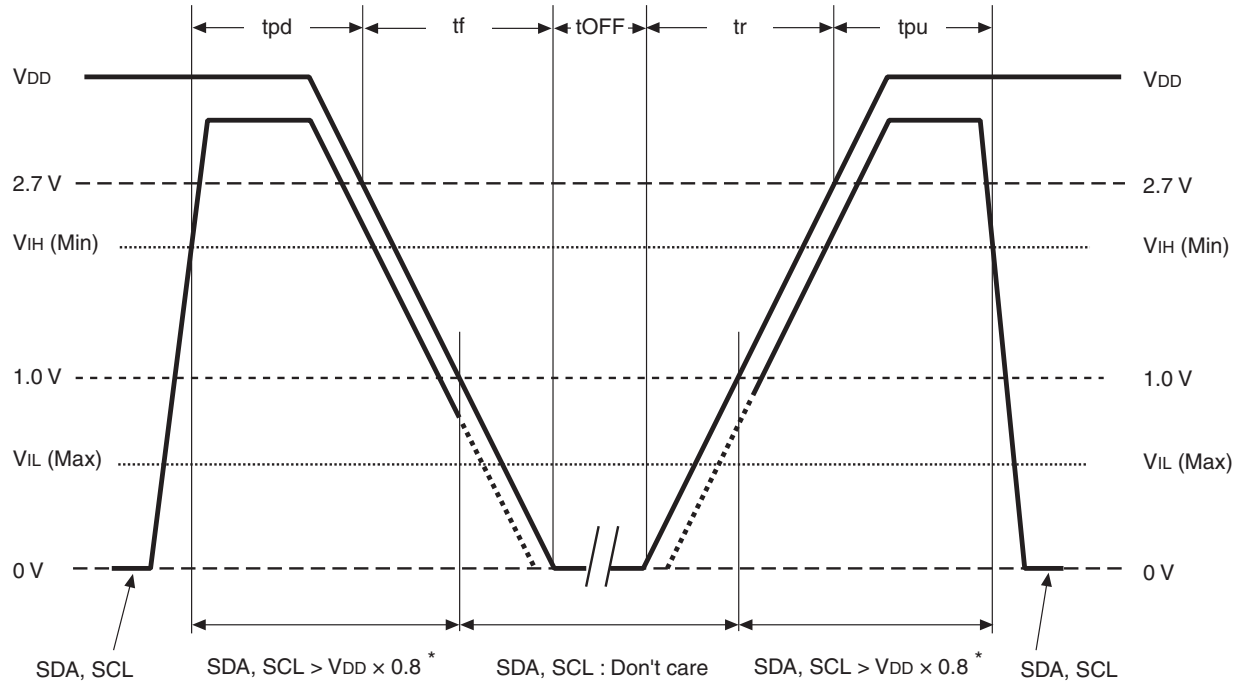
4. Pin capacitance

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I/O capacitance	$C_{I/O}$	$V_{DD} = V_{IN} = V_{OUT} = 0V$, f = 1 MHz, T_A = + 25 °C	—	—	15	pF
Input capacitance	C_{IN}		—	—	15	pF

5. AC Test Load Circuit



■ POWER ON SEQUENCE



* : SDA, SCL (Max) < V_{DD} + 0.5 V

Parameter	Symbol	Value		Unit
		Min	Max	
SDA, SCL level hold time during power down	tpd	85	—	ns
SDA, SCL level hold time during power up	tpu	85	—	ns
Power supply rise time	tr	0.5	50	ms
Power supply fall time	tf	0.01	50	ms
Power off time	tOFF	50	—	ms

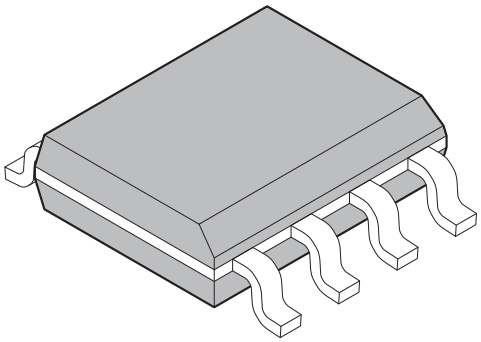
■ NOTES ON USE

- Data written before performing IR reflow is not guaranteed after IR reflow.
- VDD is required to be rising from 0 V because turning the power on from an intermediate level may cause malfunctions, when the power is turned on.

■ ORDERING INFORMATION

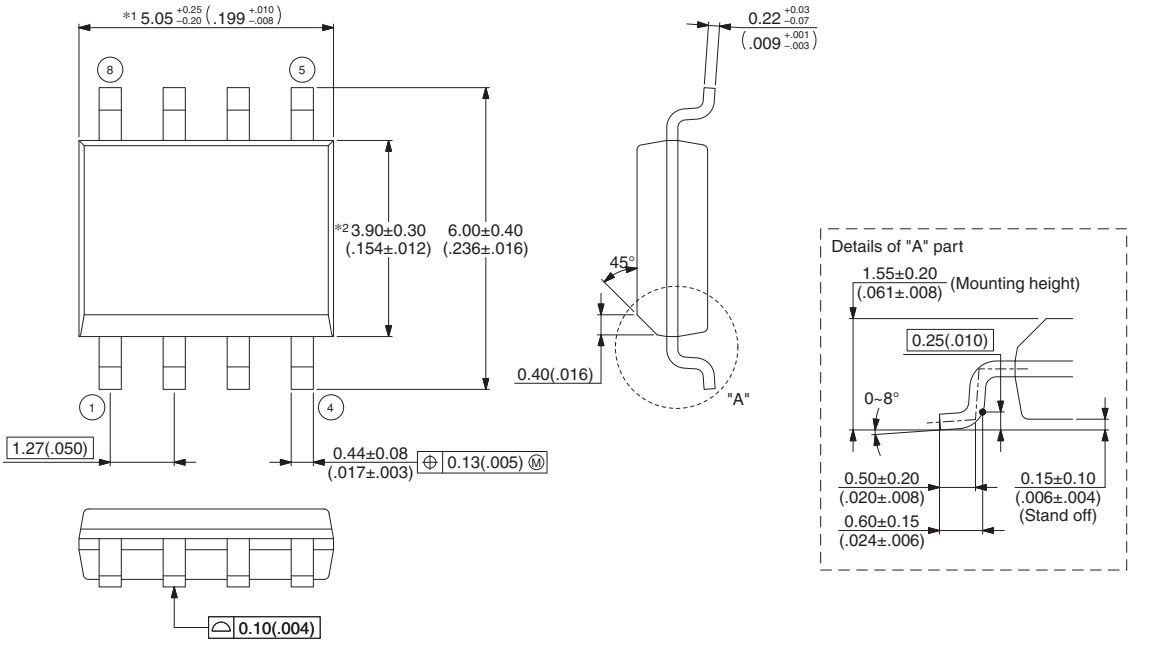
Part number	Package	Remarks
MB85RC16VPNF-G-JNE1	8-pin, plastic SOP (FPT-8P-M02)	
MB85RC16VPNF-G-JNERE1	8-pin, plastic SOP (FPT-8P-M02)	Embossed Carrier tape

■ PACKAGE DIMENSION

8-pin plastic SOP		
 (FPT-8P-M02)	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g

8-pin plastic SOP
(FPT-8P-M02)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAJOR CHANGES IN THIS EDITION

The vertical lines marked in the left side of the page shown the changes.

Page	Section	Change Results
1	■FEATURES • Data retention	Changed the temperature of data retention. + 75 °C → + 85 °C

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fsk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://sg.fujitsu.com/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fss/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fsp/

Edited: Sales Promotion Department

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for fujitsu ***manufacturer:***

Other Similar products are found below :

FCN-268D008-G/1F FCN-234D050-G/E FCN-361P040-AU FCN-364J016-AU FCN-744G010-AU/0 FCN-264D008-G/2F FCN-260C008-A/S3 FCN-268D008-G/21 FCN-268D008-G/3M-R FCN-723D010/2 FCN-361J016-AU FCN-268D024-G/10-R FCN-264D008-G/2D FCN-237B050-G/W FCN-361J024-AU FCN-268D008-G/20 FCN-230C050-C/E FCN-363J008 MAT4Z-DR FCN-268M024-G/1D FTP-639USL202 FTR-F1AA024V FTR-H1CA012V FTR-K3AB012W FTR-MYAA005D FTR-P6GN012WA PZ-2A2415 PZ-2A2425 PZ-2A2430 PZ-2A2445 PZ-4A2620 PZ-4A2650 PZ-6A2805 PZ-6A2810 PZ-6A2830 PZ-6A2840 GZ-12C GZ-12W GZ-18H GZ-9H AL-24W-K DZ4E-12V ITT2B-EH ITT2-BR 25A04C24C 25A04C28C RY-48W-K RY-5WZ-K 26A06C54E RZ-24C