

SCOPE

This specification describes YC324 series chip resistor arrays with lead-free terminations made by thick film process.

ORDERING INFORMATION

Part number is identified by the series, size, tolerance, packing type, temperature coefficient, taping reel and resistance value.

PHYCOMP ORDERING CODE

I2NC CODE

2350 XXX XXXXX L
 (1) (2) (3) (4)

| TYPE/ I220 | START IN ⁽¹⁾ | TOL. (%) | RESISTANCE RANGE | EMBOSSED TAPE ON REEL (units) ⁽²⁾ 4,000 |
|---------------|----------------------------|-------------|---------------------|---|
| YC324 | 2350 | ±5% | 10 to 1 MΩ | 039 10xxx |
| YC324 | 2350 | ±1% | 10 to 1 MΩ | 029 1xxx |

- (1) The resistors have a 12-digit ordering code starting with 2350.
- (2) The subsequent 4 or 5 digits indicate the resistor tolerance and packaging.
- (3) The remaining 4 or 3 digits represent the resistance value with the last digit indicating the multiplier as shown in the table of "Last digit of I2NC".
- (4) "L" means lead-free terminations.

| Last digit of I2NC | |
|----------------------------------|------------|
| Resistance decade ⁽³⁾ | Last digit |
| 0.01 to 0.0976 Ω | 0 |
| 0.1 to 0.976 Ω | 7 |
| 1 to 9.76 Ω | 8 |
| 10 to 97.6 Ω | 9 |
| 100 to 976 Ω | 1 |
| 1 to 9.76 kΩ | 2 |
| 10 to 97.6 kΩ | 3 |
| 100 to 976 kΩ | 4 |
| 1 to 9.76 MΩ | 5 |
| 10 to 97.6 MΩ | 6 |

Example: 0.02 Ω = 0200 or 200
 0.3 Ω = 3007 or 307
 1 Ω = 1008 or 108
 33 kΩ = 3303 or 333
 10 MΩ = 1006 or 106

ORDERING EXAMPLE

The ordering code of a YC324 convex chip resistor array, value 1,000 Ω with ±5% tolerance, supplied in tape of 4,000 units per reel is: 235003910102L.

CTC CODE

YC324 - X X X XX XXXX L
 (1) (2) (3) (4) (5) (6)

(1) TOLERANCE

F = ±1%
 J = ±5%

(2) PACKAGING TYPE

K = Embossed taping reel

(3) TEMPERATURE COEFFICIENT OF RESISTANCE

-- = Base on spec

(4) TAPING REEL

07 = 7 inch dia. Reel

(5) RESISTANCE VALUE

56R, 560R, 5K6, 56K, 1M

(6) RESISTOR TERMINATIONS

L = Lead free terminations (pure Tin)

ORDERING EXAMPLE

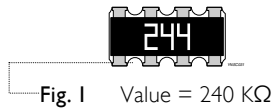
The ordering code of a YC324 convex chip resistor array, value 1,000 Ω with ±5% tolerance, supplied in 7-inch tape reel is: YC324-JK-071KL.

NOTE

- 1. The "L" at the end of the code is only for ordering. On the reel label, the standard CTC or I2NC will be mentioned an additional stamp "LFP"= lead free production.
- 2. Products with lead in terminations fulfil the same requirements as mentioned in this datasheet.
- 3. Products with lead in terminations will be phased out in the coming months (before July 1st, 2006)

MARKING

YC324



E-24 series: 3 digits

First two digits for significant figure and 3rd digit for number of zeros

For marking codes, please see EIA-marking code rules in data sheet “Chip resistors marking”.

CONSTRUCTION

The resistors are constructed out of a high-grade ceramic body. Internal metal electrodes are added at each end and connected by a resistive paste. The composition of the paste is adjusted to give the approximate required resistance and laser cutting of this resistive layer that achieves tolerance trims the value. The resistive layer is covered with a protective coat. Finally, the eight external terminations (pure Tin) are added. See fig. 2.

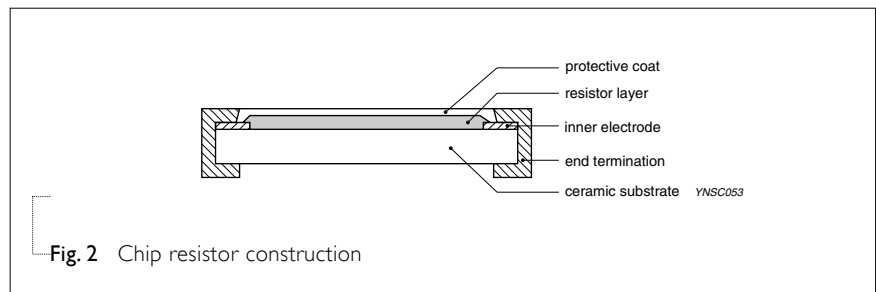


Fig. 2 Chip resistor construction

DIMENSIONS

Table I

| TYPE | YC324 |
|---------------------|------------|
| B (mm) | 0.50 ±0.20 |
| H (mm) | 1.10 ±0.15 |
| P (mm) | 1.27 ±0.05 |
| L (mm) | 5.08 ±0.20 |
| H ₂ (mm) | 0.90 ±0.15 |
| T (mm) | 0.60 ±0.10 |
| W ₁ (mm) | 0.50 ±0.15 |
| W ₂ (mm) | 3.20 ±0.20 |

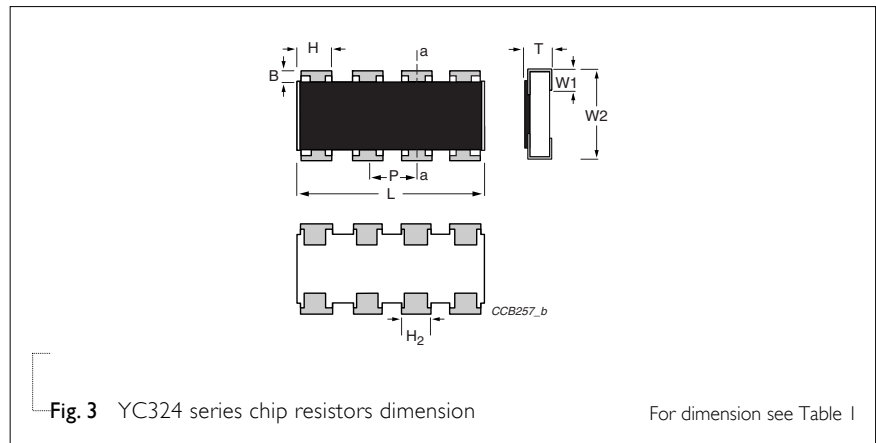


Fig. 3 YC324 series chip resistors dimension

For dimension see Table I

SCHEMATIC

For dimension see Fig. 3 and Table I



Fig. 4 Equivalent circuit diagram

ELECTRICAL CHARACTERISTICS

Table 2

| CHARACTERISTICS | YC324 1/8 W |
|---------------------------------|---------------------------|
| Operating Temperature Range | -55 °C to +155 °C |
| Maximum Working Voltage | 200 V |
| Maximum Overload Voltage | 500 V |
| Dielectric Withstanding Voltage | 500 V |
| Number of Resistors | 4 |
| Resistance Range | 5% (E24) 10 Ω to 1 MΩ |
| | 1% (E24/E96) 10 Ω to 1 MΩ |
| Temperature Coefficient | ±200 ppm/°C |

FOOTPRINT AND SOLDERING PROFILES

For recommended footprint and soldering profiles, please see the special data sheet “Chip resistors mounting”.

ENVIRONMENTAL DATA

For material declaration information (IMDS-data) of the products, please see the separated info “Environmental data” conformed to EU RoHS.

PACKING STYLE AND PACKAGING QUANTITY

Table 3 Packing style and packaging quantity

| PRODUCT TYPE | PACKING STYLE | REEL DIMENSION | QUANTITY PER REEL |
|--------------|--------------------------|----------------|-------------------|
| YC324 | Embossed taping reel (K) | 7" (178 mm) | 4,000 units |

NOTE

- For embossed tape and reel specification/dimensions, please see the special data sheet “Packing” document.

FUNCTIONAL DESCRIPTION

POWER RATING

YC324 rated power at 70°C is 1/8 W

RATED VOLTAGE

The DC or AC (rms) continuous working voltage corresponding to the rated power is determined by the following formula:

$$V = \sqrt{P \times R}$$

Where

V = Continuous rated DC or AC (rms) working voltage (V)

P = Rated power (W)

R = Resistance value (Ω)

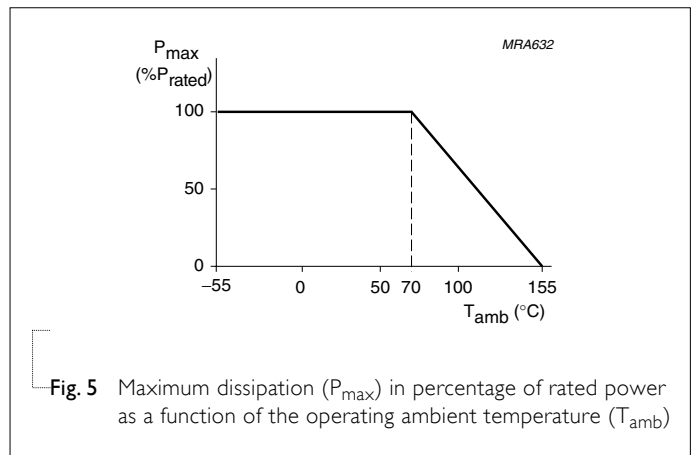


Fig. 5 Maximum dissipation (P_{max}) in percentage of rated power as a function of the operating ambient temperature (T_{amb})

TESTS AND REQUIREMENTS

Table 4 Test condition, procedure and requirements

| TEST | TEST METHOD | PROCEDURE | REQUIREMENTS |
|--|---|--|--|
| Temperature Coefficient of Resistance (T.C.R.) | MIL-STD-202F-method 304; | At +25/-55 °C and +25/+125 °C | Refer to table 2 |
| | JIS C 5202-4.8 | <p>Formula:</p> $T.C.R = \frac{R_2 - R_1}{R_1(t_2 - t_1)} \times 10^6 \text{ (ppm/°C)}$ <p>Where $t_1 = +25 \text{ °C}$ or specified room temperature $t_2 = -55 \text{ °C}$ or +125 °C test temperature $R_1 =$ resistance at reference temperature in ohms $R_2 =$ resistance at test temperature in ohms</p> | |
| Thermal Shock | MIL-STD-202F-method 107G; IEC 60115-1 4.19 | At -65 (+0/-10) °C for 2 minutes and at +155 (+10/-0) °C for 2 minutes; 25 cycles | ±(0.5% +0.05 Ω) for 1% tol. ±(1.0% +0.05 Ω) for 5% tol. |
| Low Temperature Operation | MIL-R-55342D-Para 4.7.4 | At -65 (+0/-5) °C for 1 hour; RCWV applied for 45 (+5/-0) minutes | ±(0.5% +0.05 Ω) for 1% tol . ±(1.0% +0.05 Ω) for 5% tol. No visible damage |
| Short Time Overload | MIL-R-55342D-Para 4.7.5; IEC 60115-1 4.13 | 2.5 × RCWV applied for 5 seconds at room temperature | ±(1.0% +0.05 Ω) for 1% tol. ±(2.0% +0.05 Ω) for 5% tol. No visible damage |
| Insulation Resistance | MIL-STD-202F-method 302; IEC 60115-1 4.6.1.1 | RCOV for 1 minute <u>Type</u> YC324 <u>Voltage (DC)</u> 500 V | ≥10 GΩ |
| Dielectric Withstand Voltage | MIL-STD-202F-method 301; IEC 60115-1 4.6.1.1 | Maximum voltage (V_{rms}) applied for 1 minute <u>Type</u> YC324 <u>Voltage (AC)</u> 500 V_{rms} | No breakdown or flashover |
| Resistance to Soldering Heat | MIL-STD-202F-method 210C; IEC 60115-1 4.18 | Unmounted chips; 260 ±5 °C for 10 ±1 seconds | ±(0.5% +0.05 Ω) for 1% tol. ±(1.0% +0.05 Ω) for 5% tol. No visible damage |
| Life | MIL-STD-202F-method 108A; IEC 60115-1 4.25.1 | At 70 ±2 °C for 1,000 hours; RCWV applied for 1.5 hours on and 0.5 hour off | ±(1% +0.05 Ω) for 1% tol. ±(3% +0.05 Ω) for 5% tol. |

| TEST | TEST METHOD | PROCEDURE | REQUIREMENTS | | | | | | | | | | | | | | |
|--------------------------|---|--|---|-----------------|-------|-----------|-------|------------------|-------|------------------|-------|--------------------|-------|-------------------|-------|------------------|-------|
| Solderability | MIL-STD-202F-method 208A; IEC 60115-1 4.17 | Solder bath at 245 ±3 °C Dipping time: 2 ±0.5 seconds | Well tinned (≥95% covered) No visible damage | | | | | | | | | | | | | | |
| Bending Strength | JIS C 5202.6.14; IEC 60115-1 4.15 | Resistors mounted on a 90 mm glass epoxy resin PCB (FR4) Bending: 1 mm | ±(1.0% +0.05 Ω) for 1% tol. ±(1.0% +0.05 Ω) for 5% tol. No visible damage | | | | | | | | | | | | | | |
| Resistance to Solvent | MIL-STD-202F-method 215; IEC 60115-1 4.29 | Isopropylalcohol (C ₃ H ₇ OH) or dichloromethane (CH ₂ Cl ₂) followed by brushing | No smeared | | | | | | | | | | | | | | |
| Noise | JIS C 5202 5.9; IEC 60115-1 4.12 | Maximum voltage (V _{rms}) applied. | <table border="1"> <thead> <tr> <th>Resistors range</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>R < 100 Ω</td> <td>10 dB</td> </tr> <tr> <td>100 Ω ≤ R < 1 KΩ</td> <td>20 dB</td> </tr> <tr> <td>1 KΩ ≤ R < 10 KΩ</td> <td>30 dB</td> </tr> <tr> <td>10 KΩ ≤ R < 100 KΩ</td> <td>40 dB</td> </tr> <tr> <td>100 KΩ ≤ R < 1 MΩ</td> <td>46 dB</td> </tr> <tr> <td>1 MΩ ≤ R ≤ 22 MΩ</td> <td>48 dB</td> </tr> </tbody> </table> | Resistors range | Value | R < 100 Ω | 10 dB | 100 Ω ≤ R < 1 KΩ | 20 dB | 1 KΩ ≤ R < 10 KΩ | 30 dB | 10 KΩ ≤ R < 100 KΩ | 40 dB | 100 KΩ ≤ R < 1 MΩ | 46 dB | 1 MΩ ≤ R ≤ 22 MΩ | 48 dB |
| Resistors range | Value | | | | | | | | | | | | | | | | |
| R < 100 Ω | 10 dB | | | | | | | | | | | | | | | | |
| 100 Ω ≤ R < 1 KΩ | 20 dB | | | | | | | | | | | | | | | | |
| 1 KΩ ≤ R < 10 KΩ | 30 dB | | | | | | | | | | | | | | | | |
| 10 KΩ ≤ R < 100 KΩ | 40 dB | | | | | | | | | | | | | | | | |
| 100 KΩ ≤ R < 1 MΩ | 46 dB | | | | | | | | | | | | | | | | |
| 1 MΩ ≤ R ≤ 22 MΩ | 48 dB | | | | | | | | | | | | | | | | |
| Humidity (steady state) | JIS C 5202 7.5; IEC 60115-8 4.24.8 | 1,000 hours; 40 ±2 °C; 93(+2/-3)% RH RCWV applied for 1.5 hours on and 0.5 hour off | ±(0.5% +0.05 Ω) for 1% tol. ±(2.0% +0.05 Ω) for 5% tol. | | | | | | | | | | | | | | |
| Leaching | EIA/IS 4.13B; IEC 60115-8 4.18 | Solder bath at 260 ±5 °C Dipping time: 30 ±1 seconds | No visible damage | | | | | | | | | | | | | | |
| Intermittent Overload | JIS C 5202 5.8 | At room temperature; 2.5 × RCWV applied for 1 second on and 25 seconds off; total 10,000 cycles | ±(1.0% +0.05 Ω) for 1% tol. ±(2.0% +0.05 Ω) for 5% tol. | | | | | | | | | | | | | | |
| Resistance to Vibration | On request | On request | | | | | | | | | | | | | | | |
| Moisture Resistance Heat | MIL-STD-202F-method 106F; IEC 60115-1 4.24.2 | 42 cycles; total 1,000 hours Shown as Fig. 6 | ±(0.5% +0.05Ω) for 1% tol. ±(2.0% +0.05Ω) for 5% tol. No visible damage | | | | | | | | | | | | | | |

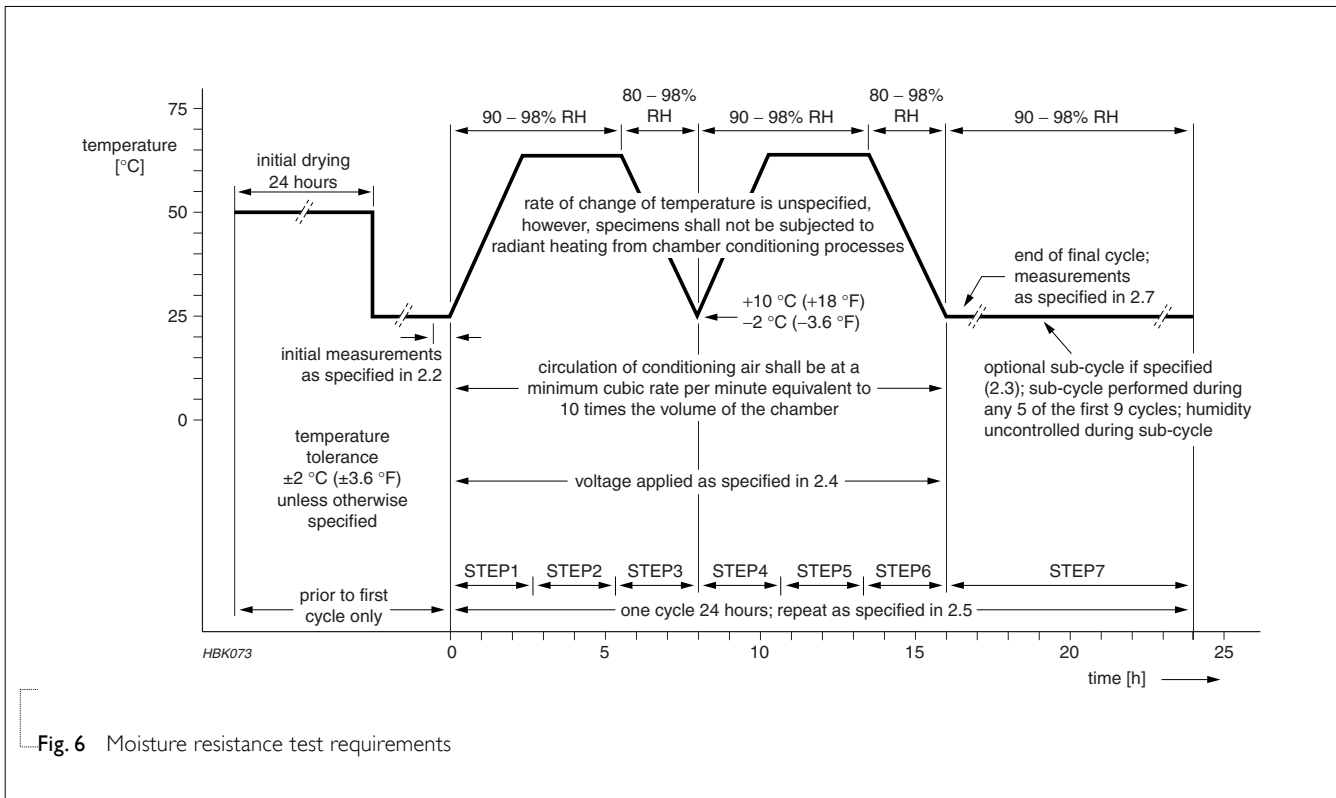


Fig. 6 Moisture resistance test requirements

REVISION HISTORY

| REVISION | DATE | CHANGE NOTIFICATION | DESCRIPTION |
|-----------|--------------|---------------------|--|
| Version 1 | Feb 22, 2005 | - | - New datasheet for YC324 convex type chip resistor arrays 1% and 5% with lead-free terminations |

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