BLF644P

Broadband power LDMOS transistor

Rev. 1 — 11 June 2013 Objective data sheet

1. Product profile

1.1 General description

A 70 W LDMOS RF power transistor for broadcast transmitter and industrial applications. The transistor is suitable for the frequency range HF to 1300 MHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital applications.

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source test circuit.

Test signal	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	IMD (dBc)
CW, class-A	860	32	90	22	<tbd>	-
CW pulsed, class-AB	860	32	100	23.5	66	<tbd>
2-tone, class-AB	860	32	45	23	<tbd>	<tbd>

1.2 Features and benefits

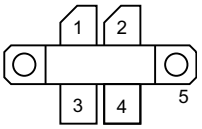
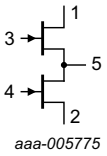
- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Communication transmitter applications in the HF to 1300 MHz frequency range
- Industrial applications in the HF to 1300 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

aaa-005775

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF644P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1228A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 90 W	[1]	<tbd>	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 32 V; I_D = 50 mA	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_{Dq} = 250 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	9.0	-	A
I_{GSS}	gate leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	-	50	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.5 A	-	3.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.75 A	-	300	-	mΩ

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	39	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	15	-	pF
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	0.84	-	pF

Table 8. RF characteristics

Test signal: CW pulsed, class-AB; f = 860 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 200 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 100 W	23	23.5	-	dB
η_D	drain efficiency	P_L = 100 W	61	66	-	%
RL_{in}	input return loss	P_L = 100 W	-	–15	–10	dBc

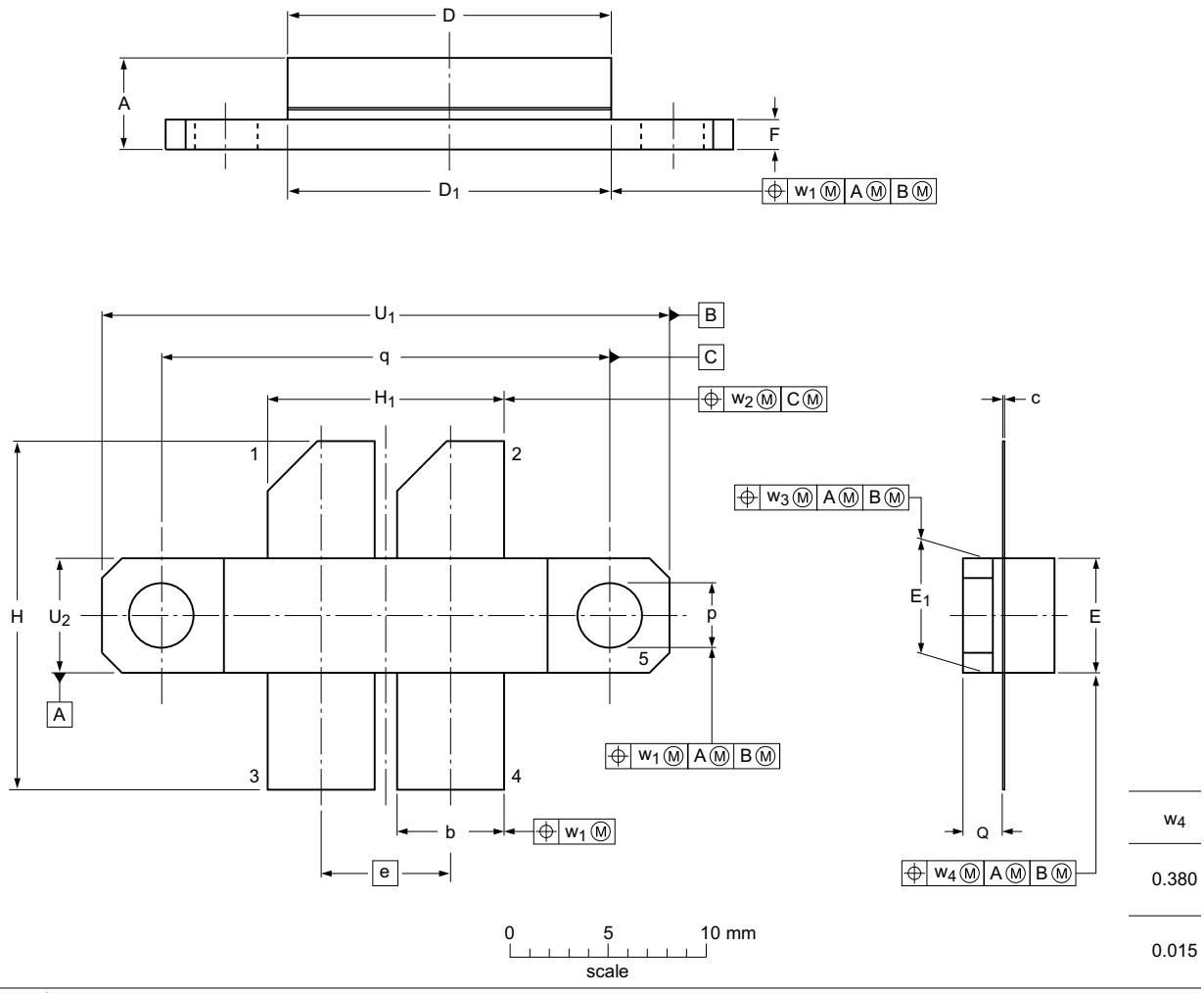
7. Test information

7.1 Ruggedness in class-AB operation

The BLF644P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; f = 1300 MHz at rated load power.

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads **SOT1228A**



w4
0.380
0.015

Dimensions

Unit[1]		A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q[2]	q	U_1	U_2	w_1	w_2	w_3
mm	max	5.2	5.59	0.15	16.66	16.69		5.92	5.97	1.65	18.29	12.19	3.43	2.21		29.08	5.97			
	nom						6.60								22.86			0.25	0.51	0.125
	min	4.5	5.33	0.08	16.36	16.33		5.77	5.72	1.40	17.27	11.94	3.18	1.96		28.83	5.72			
inches	max	0.205	0.220	0.006	0.656	0.657		0.233	0.235	0.065	0.720	0.480	0.135	0.087		1.145	0.235			
	nom						0.26								0.900			0.01	0.02	0.005
	min	0.177	0.210	0.003	0.644	0.643		0.227	0.225	0.055	0.680	0.470	0.125	0.077		1.135	0.225			

Note
1. Millimeter dimensions are derived from the original inch dimensions.
2. Dimension is measured 0.030 inch (0.76 mm) from body.

sot1228a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1228A						~~12-06-11~~ 13-05-16

Fig 1. Package outline SOT1228A

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF644P v.1	20130611	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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