

# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### General Description

The MAX44280 offers a unique combination of high speed, precision, low noise, and low-voltage operation making it ideally suited for a large number of signal processing functions such as filtering and amplification of signals in portable and industrial equipment.

The amplifier features an input offset of less than 50 $\mu$ V and a high-gain bandwidth product of 50MHz while maintaining a low 1.8V supply rail. The device is internally compensated for gains of 5V/V or greater. The device's rail-to-rail input/outputs and low noise guarantee maximum dynamic range in demanding applications such as 12- to 16-bit SAR ADC drivers. Unlike traditional rail-to-rail input structures, input crossover distortion is absent due to an optimized input stage with an ultra-quiet charge pump.

The MAX44280 includes a fast-power-on shutdown mode for further power savings.

The MAX44280 operates from a supply range of 1.8V to 5.5V over the -40°C to +125°C temperature range and can operate down to 1.7V over the 0°C to +70°C temperature range. The MAX44280 is available in a small, 6-pin SC70 package and is also available in a 1mm x 1.5mm thin  $\mu$ DFN (ultra-thin LGA) package.

**Ordering Information** appears at end of data sheet.

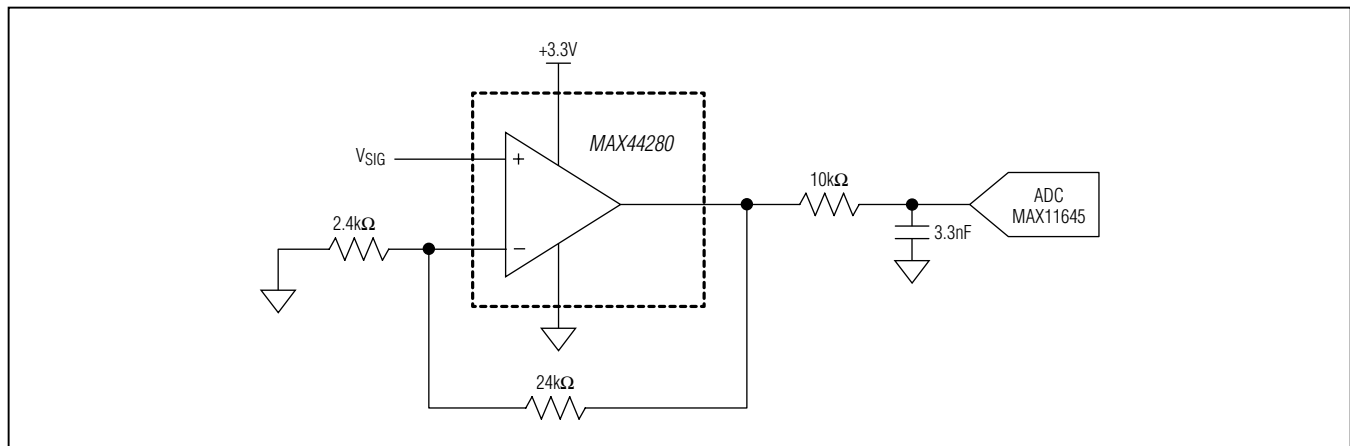
### Features

- ◆ Low 1.8V Supply Rail Over the -40°C to +125°C Range
- ◆ 1.7V Supply Rail Over the 0°C to +70°C Range
- ◆ 50MHz Bandwidth
- ◆ Low 12.7nV/ $\sqrt{\text{Hz}}$  Input Voltage-Noise Density
- ◆ Low 1.2fA/ $\sqrt{\text{Hz}}$  Input Current-Noise Density
- ◆ Low 50 $\mu$ V (max) VOS at +25°C
- ◆ 500fA Low Input Bias Current
- ◆ 750 $\mu$ A Quiescent Current per Amplifier
- ◆ < 1 $\mu$ A Supply Current in Shutdown
- ◆ Small, 2mm x 2mm SC70 and 1mm x 1.5mm Thin  $\mu$ DFN Packages
- ◆ Low -110dB Total Harmonic Distortion
- ◆ 5V/V Minimum Stable Gain

### Applications

Notebooks  
 3G/4G Handsets  
 Portable Media Players  
 Portable Medical Instruments  
 Battery-Operated Devices  
 Analog-to-Digital Converter Buffers  
 Transimpedance Amplifiers  
 General-Purpose Signal Processing

### Typical Application Circuit



For related parts and recommended products to use with this part, refer to: [www.maximintegrated.com/MAX44280.related](http://www.maximintegrated.com/MAX44280.related)

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### ABSOLUTE MAXIMUM RATINGS

IN+, IN-, OUT .....	(V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V)	Thin µDFN (Ultra-Thin LGA)
V <sub>DD</sub> to V <sub>SS</sub> .....	-0.3V to +6V	(derate 2.1mW/°C above +70°C) .....
SHDN.....	-0.3V to +6V	110.2mW
Output to Short-Circuit Ground Duration .....	10s	Operating Temperature Range .....
Continuous Input Current into Any Pin.....	±20mA	-40°C to +125°C
Continuous Power Dissipation (T <sub>A</sub> = +70°C)		Junction Temperature .....
SC70 (derate 3.1mW/°C above +70°C) .....	245mW	+150°C
		Lead Temperature (soldering, 10s) .....
		+300°C
		Soldering Temperature (reflow) .....
		+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### PACKAGE THERMAL CHARACTERISTICS (Note 1)

SC70	Thin µDFN (Ultra-Thin LGA)		
Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) ....	326.5°C/W	Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) .....	470°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) .....	115°C/W	Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) .....	120°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 3.3V, V<sub>SS</sub> = 0V, V<sub>IN+</sub> = V<sub>IN-</sub> = V<sub>DD</sub>/2, R<sub>L</sub> = 10kΩ to V<sub>DD</sub>/2, V<sub>SHDN</sub> = V<sub>DD</sub>, T<sub>A</sub> = -40°C to +125°C. Typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC CHARACTERISTICS</b>						
Input Voltage Range	V <sub>IN+</sub> V <sub>IN-</sub>	Guaranteed by CMRR test	-0.1		V <sub>DD</sub> + 0.1	V
Input Offset Voltage	V <sub>OS</sub>	T <sub>A</sub> = +25°C		10	50	µV
		T <sub>A</sub> = -40°C to +125°C after calibration			100	
		T <sub>A</sub> = -40°C to +125°C			500	
Input Offset Voltage Drift	V <sub>OS</sub> - TC			0.8	5	µV/°C
Input Bias Current (Note 3)	I <sub>B</sub>	T <sub>A</sub> = +25°C		0.01	0.5	pA
		T <sub>A</sub> = -40°C to +85°C			10	
		T <sub>A</sub> = -40°C to +125°C			100	
Input Capacitance	C <sub>IN</sub>			0.4		pF
Common-Mode Rejection Ratio	CMRR	V <sub>CM</sub> = -0.1V to (V <sub>DD</sub> + 0.1V)	75	90		dB
Open-Loop Gain	A <sub>OL</sub>	0.4V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> - 0.4V, R <sub>OUT</sub> = 10kΩ	100	115		dB
		0.4V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> - 0.4V, R <sub>OUT</sub> = 600Ω	91	100		
		0.4V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> - 0.4V, R <sub>OUT</sub> = 32Ω		80		
Output Short-Circuit Current	I <sub>SC</sub>	To V <sub>DD</sub> or V <sub>SS</sub>		85		mA

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $\overline{V_{SHDN}} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing	$V_{OL} - V_{SS}$	$R_{OUT} = 10k\Omega$			20	mV
		$R_{OUT} = 600\Omega$			50	
		$R_{OUT} = 32\Omega$	400		700	
	$V_{DD} - V_{OH}$	$R_{OUT} = 10k\Omega$			10	
		$R_{OUT} = 600\Omega$			40	
		$R_{OUT} = 32\Omega$	400		800	
<b>AC CHARACTERISTICS</b>						
Input Voltage-Noise Density	$e_n$	$f = 10kHz$		12.7		$nV/\sqrt{Hz}$
Input Current-Noise Density	$i_n$	$f = 10kHz$		1.2		$fA/\sqrt{Hz}$
Gain-Bandwidth Product	GBWP			50		MHz
Minimum Stable Gain	$A_{MIN}$			5		V/V
Slew Rate	SR			30		V/ $\mu s$
Settling Time		$V_{OUT} = 2V_{P-P}$ , $V_{DD} = 3.3V$ , $A_V = 5V/V$ , $C_L = 30pF$ (load), settle to 0.01%		0.6		$\mu s$
Capacitive Load	$C_{LOAD}$	No sustained oscillation, 5V/V		80		pF
		No sustained oscillation, 10V/V		500		
Total Harmonic Distortion	THD	$f = 10kHz$ , $V_O = 2V_{P-P}$ , $A_V = 5V/V$ , $R_{OUT} = 10k\Omega$		-110		dB
Output Transient Recovery Time		$\Delta V_{OUT} = 0.2V$ , $V_{DD} = 3.3V$ , $A_V = 5V/V$ ; $R_S = 20\Omega$ , $C_L = 1nF$ (load)		1		$\mu s$
<b>POWER-SUPPLY CHARACTERISTICS</b>						
Power-Supply Range	$V_{DD}$	Guaranteed by PSRR	1.8		5.5	V
		$T_A = 0^\circ C$ to $+70^\circ C$	1.7		5.5	
Power-Supply Rejection Ratio	PSRR	$V_{CM} = V_{DD}/2$	82	95		dB
Quiescent Current	$I_{DD}$			750	1200	$\mu A$
Shutdown Supply Current	$\overline{I_{SHDN}}$				1	$\mu A$
Shutdown Input Low	$V_{IL}$				0.7	V
Shutdown Input High	$V_{IH}$		1.3			V
Output Leakage Current in Shutdown	$\overline{I_{SHDN}}$			100		pA
Shutdown Input Bias Current	$I_{IL}/I_{IH}$				1	$\mu A$
Shutdown Turn-On Time	$t_{SHDN}$			15		$\mu s$
Turn-On Time	$t_{ON}$			10		ms

**Note 2:** All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.

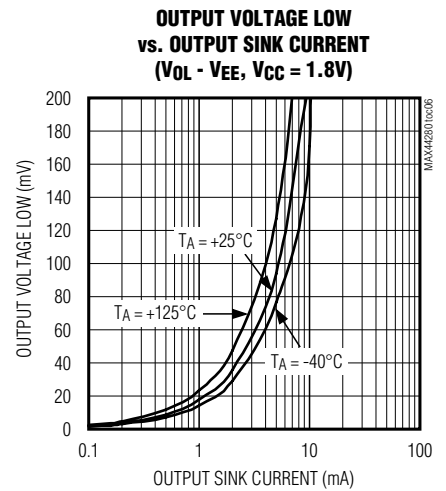
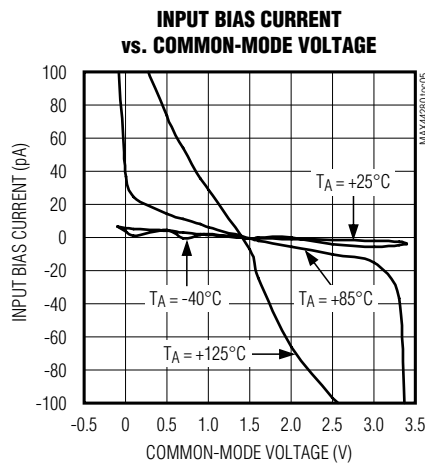
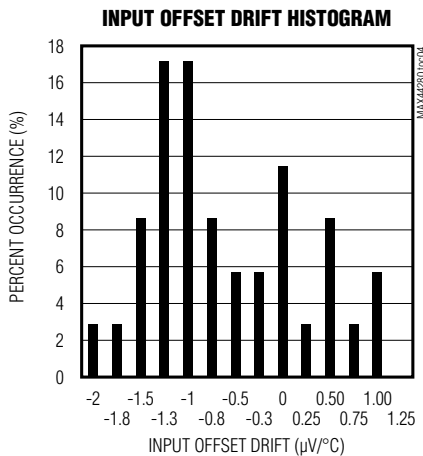
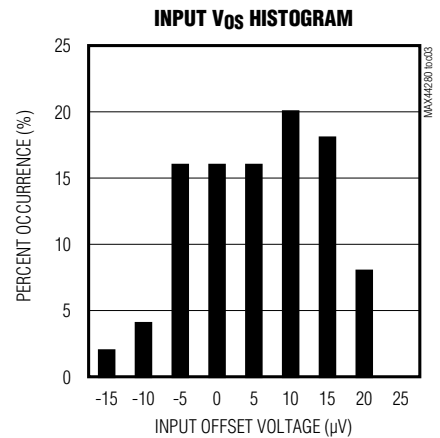
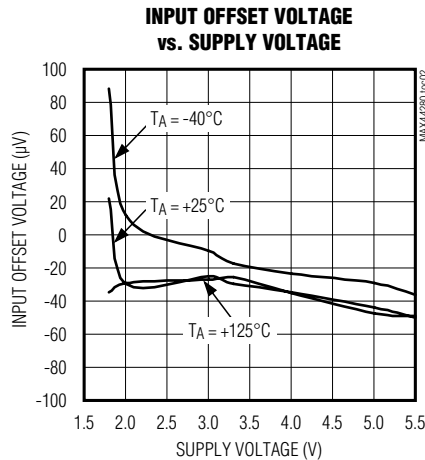
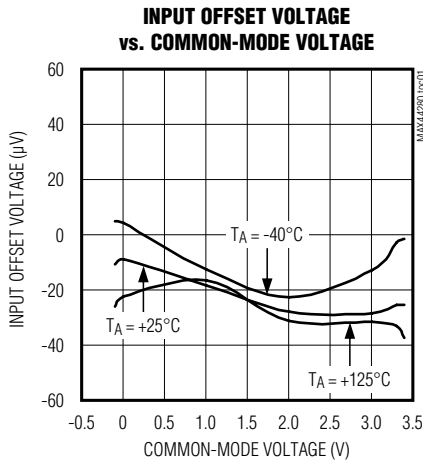
**Note 3:** Guaranteed by design.

# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### Typical Operating Characteristics

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.)

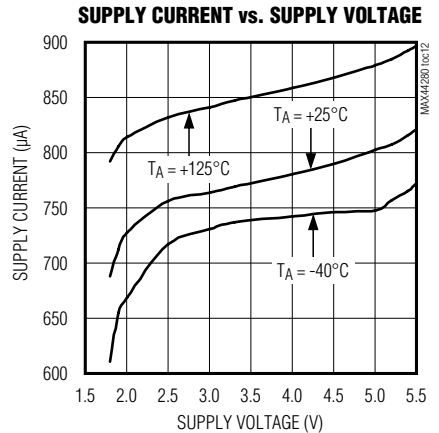
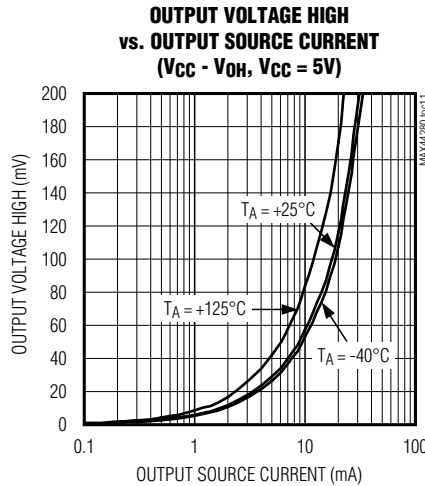
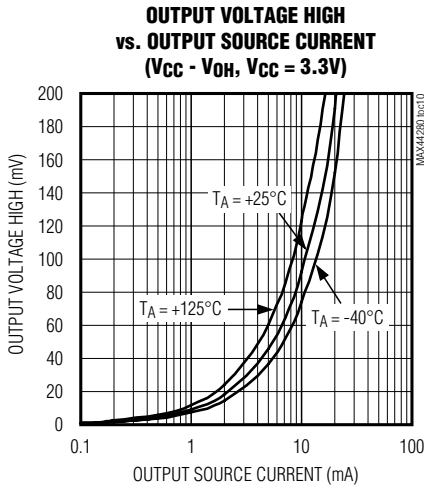
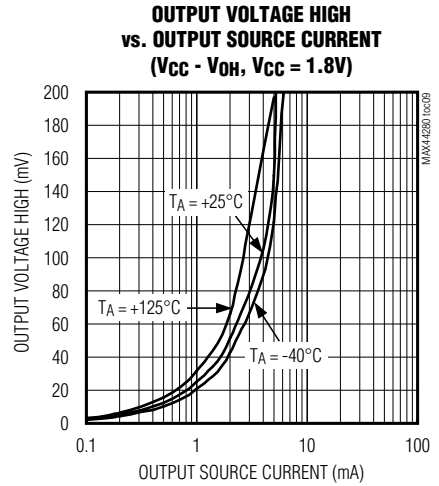
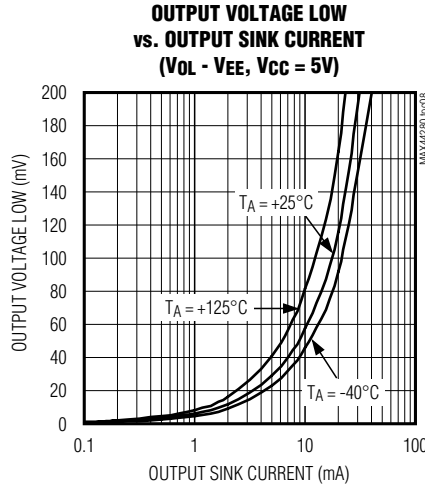
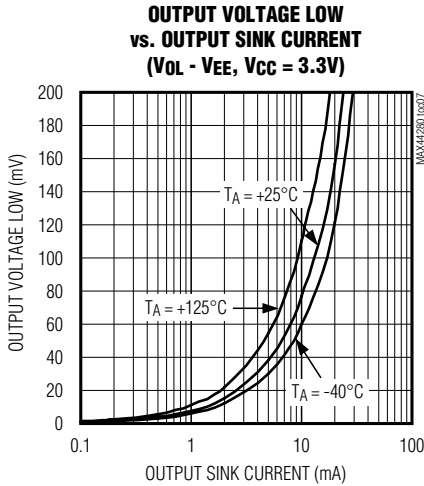


# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### Typical Operating Characteristics (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.)



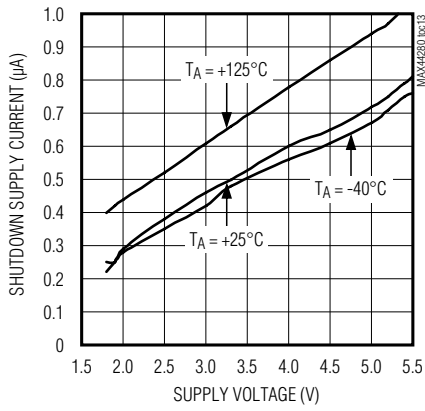
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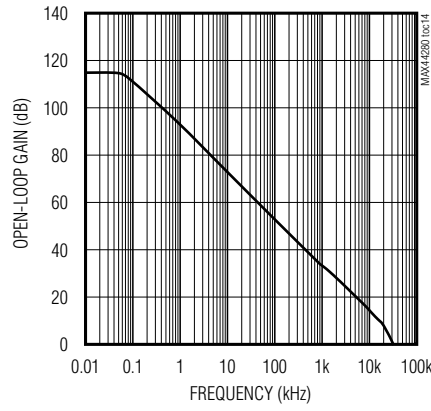
### Typical Operating Characteristics (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.)

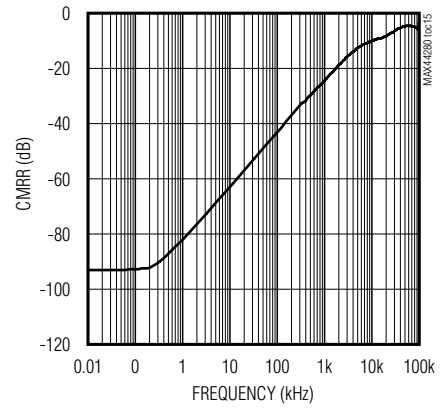
**SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE**  
( $V_{SHDN} = V_{EE}$ )



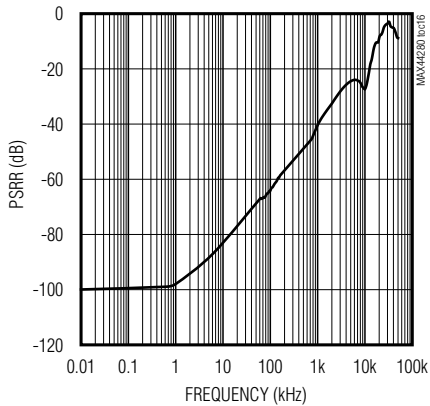
**OPEN-LOOP GAIN vs. FREQUENCY**



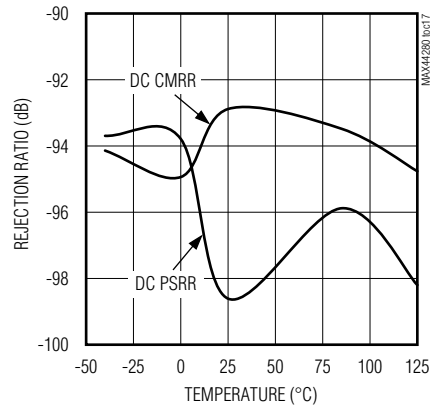
**COMMON-MODE REJECTION RATIO vs. FREQUENCY**



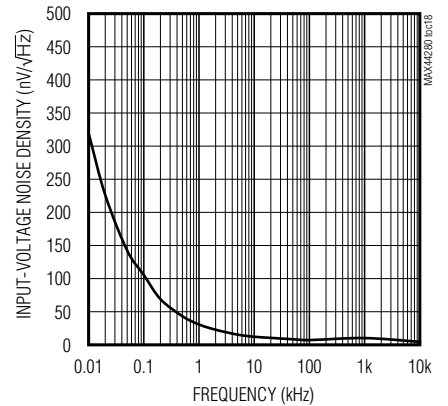
**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY**



**DC CMRR AND PSRR vs. TEMPERATURE**



**INPUT VOLTAGE-NOISE DENSITY vs. FREQUENCY**



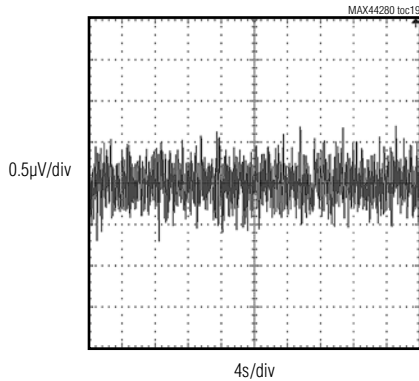
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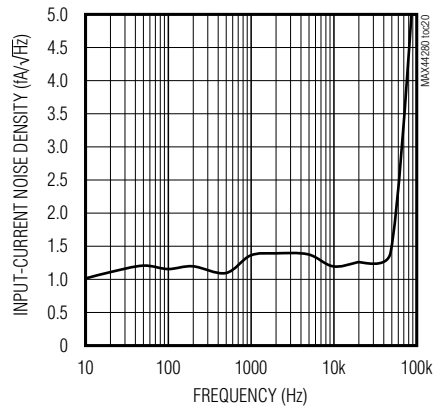
### Typical Operating Characteristics (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.)

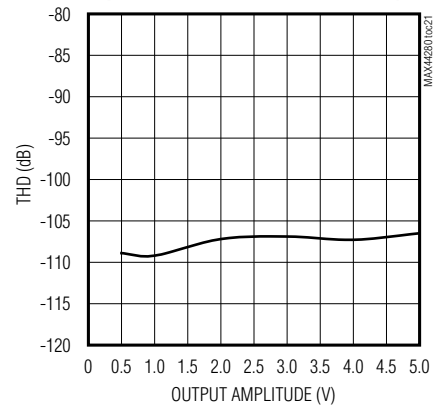
**0.1Hz TO 10Hz OUTPUT-VOLTAGE NOISE**



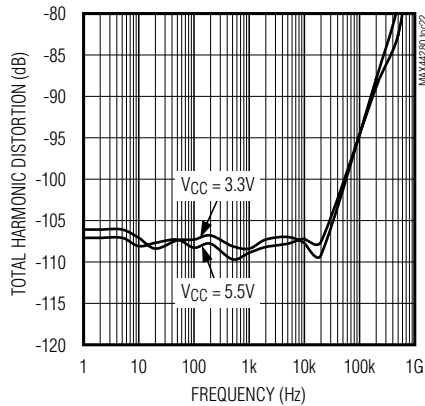
**INPUT CURRENT-NOISE DENSITY vs. FREQUENCY**



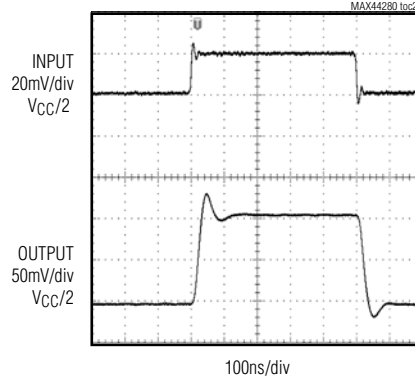
**TOTAL HARMONIC DISTORTION vs. INPUT AMPLITUDE**  
( $f = 10kHz$ ,  $V_{CC} = 5.5V$ ,  $A_V = 5V/V$ )



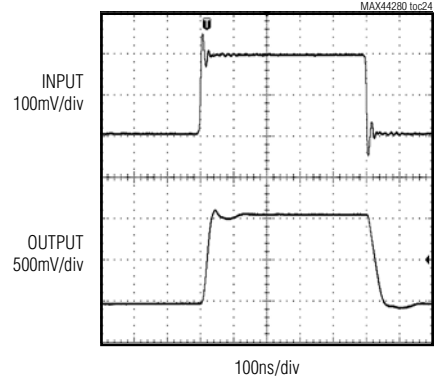
**TOTAL HARMONIC DISTORTION vs. FREQUENCY**  
( $V_{OUT} = 2VP-P$ )



**SMALL-SIGNAL TRANSIENT RESPONSE**  
( $A_V = 5V/V$ ,  $R_F = 4k\Omega$ ,  $R_G = 1k\Omega$ )



**LARGE-SIGNAL TRANSIENT RESPONSE**  
( $A_V = 5V/V$ ,  $R_F = 4k\Omega$ ,  $R_G = 1k\Omega$ )

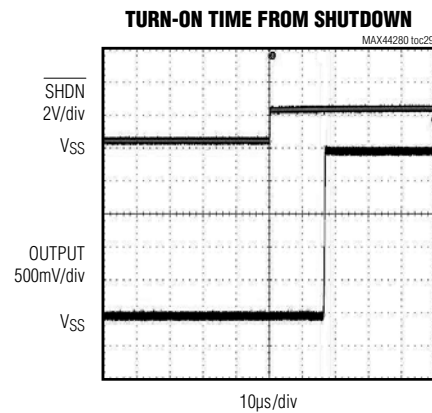
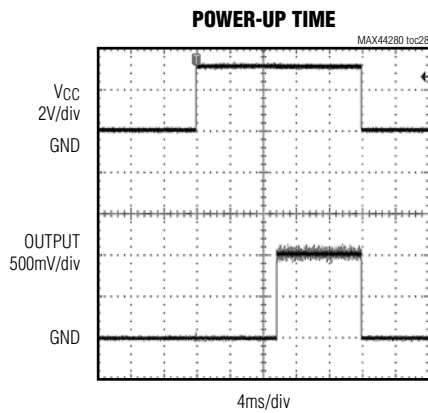
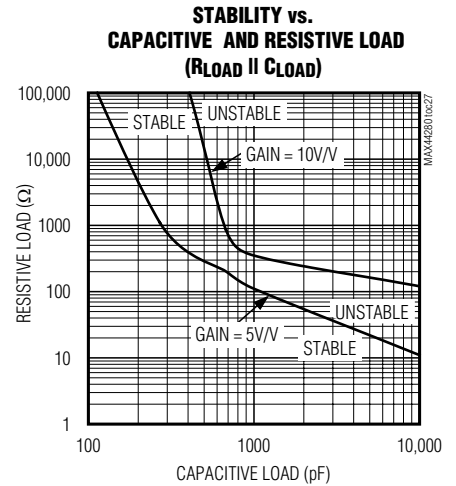
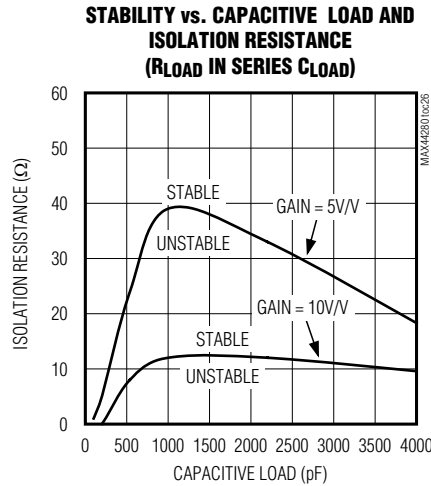
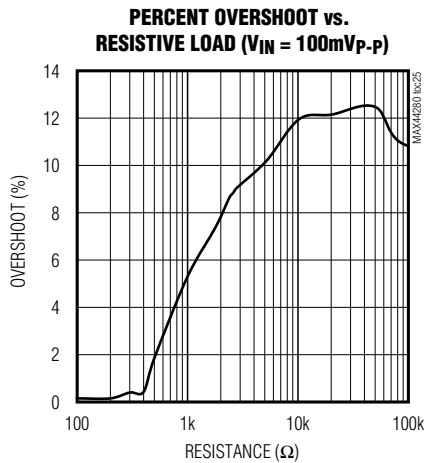


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## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### Typical Operating Characteristics (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.)

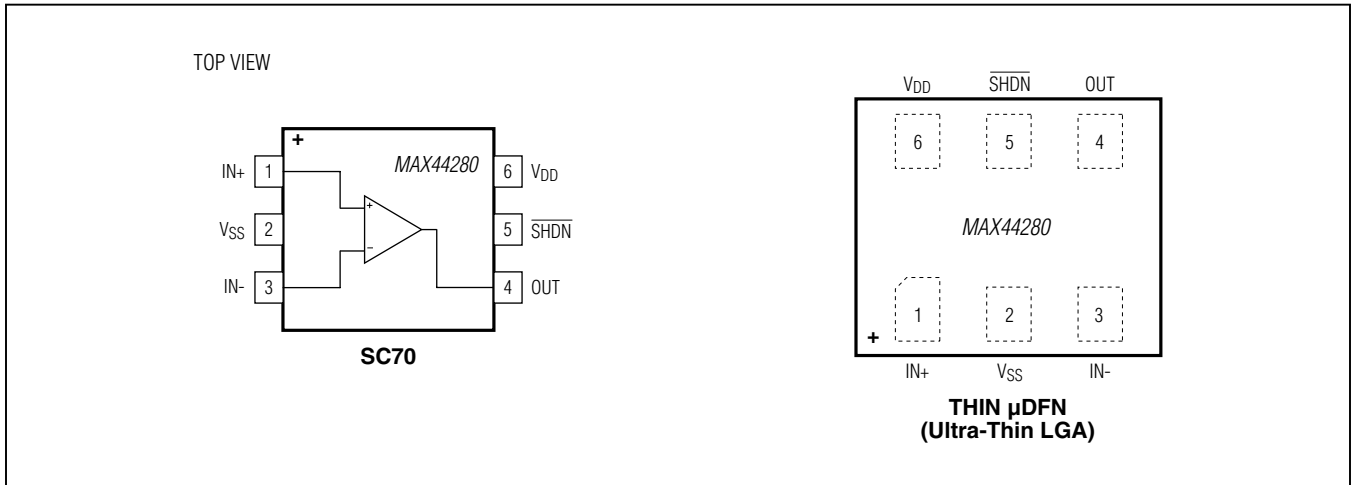




# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### Pin Configurations



### Pin Description

PIN	NAME	FUNCTION
1	IN+	Positive Input
2	V <sub>SS</sub>	Negative Power Supply. Bypass with a 0.1μF capacitor to ground.
3	IN-	Negative Input
4	OUT	Output
5	SHDN	Active-Low Shutdown
6	V <sub>DD</sub>	Positive Power Supply. Bypass with a 0.1μF capacitor to ground.

# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### Detailed Description

The MAX44280 is a high-speed low-power op amp ideal for signal processing applications due to the device's high precision and low-noise CMOS inputs. The device self-calibrates on power-up to eliminate effects of temperature and power-supply variation.

The MAX44280 also features a low-power shutdown mode that greatly reduces quiescent current while the device is not operational and recovers in 30 $\mu$ s.

### Crossover Distortion

This op amp features a low-noise integrated charge pump that creates an internal voltage rail 1V above  $V_{DD}$ , which is used to power the input differential pair of pMOS transistors as shown in [Figure 1](#). Such a unique architecture eliminates crossover distortion common in traditional CMOS input architecture ([Figure 2](#)), especially when used in a noninverting configuration, such as for Sallen-Key filters.

The charge pump's operating frequency lies well above the unity-gain frequency of the amplifier. Thanks to its high-frequency operation and ultra-quiet circuitry, the charge pump generates little noise, does not require external components, and is entirely transparent to the user.

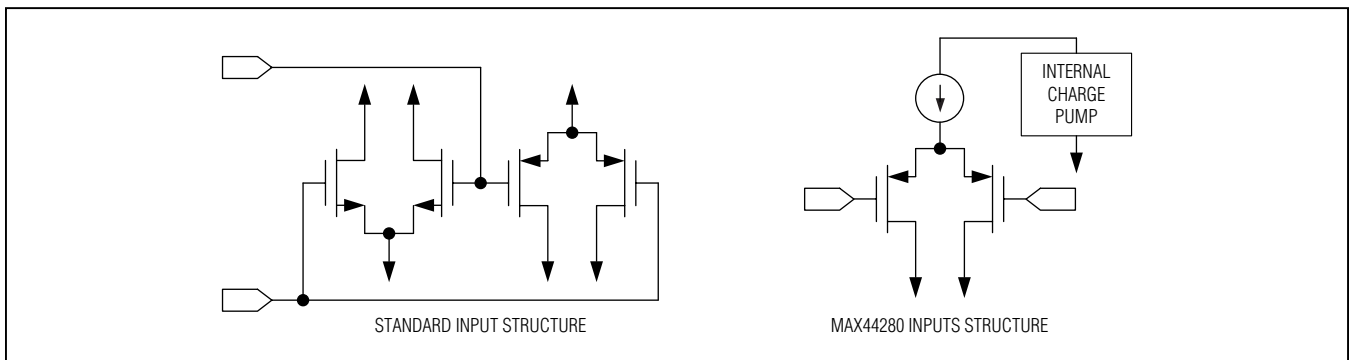


Figure 1. Comparing the Input Structure of the MAX44280 to Standard Op-Amp Inputs

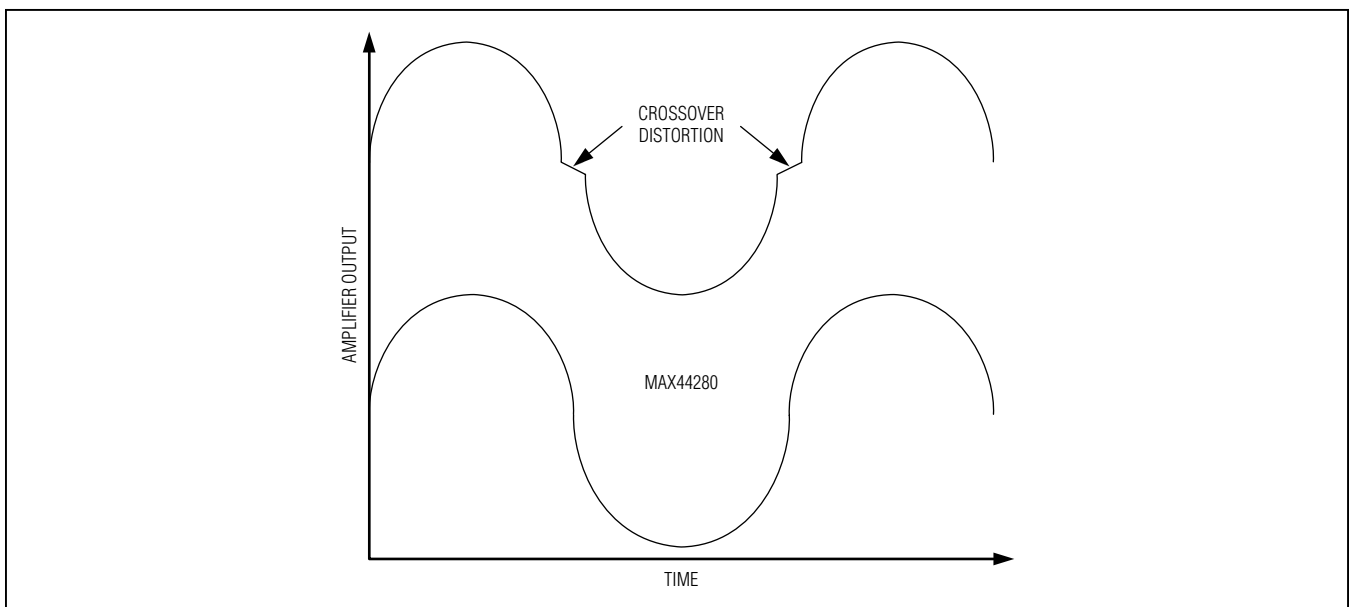


Figure 2. Crossover Distortion of Typical Amplifiers

# MAX44280

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### **Applications Information**

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#### **Power-Up Autotrim**

The IC features an automatic trim that self-calibrates the  $V_{OS}$  of this device to less than 50 $\mu$ V of input offset voltage on power-up. This self-calibration feature allows the device to eliminate input offset voltage effects due to power supply and operating temperature variation simply by cycling its power. The autotrim sequence takes approximately 10ms to complete and is triggered by an internal power-on-reset (POR) circuitry. During this time, the inputs and outputs are put into high impedance and left unconnected.

#### **Shutdown Operation**

The MAX44280 features an active-low shutdown mode that puts both inputs and outputs into high impedance and substantially lowers the quiescent current to less than 1 $\mu$ A. Putting the output into high impedance allows multiple outputs to be multiplexed onto a single output line without the additional external buffers. The device does not self-calibrate when exiting shutdown mode and retains its power-up trim settings. The device also recovers from shutdown in under 30 $\mu$ s.

The shutdown logic levels of the device is independent of supply, allowing the shutdown feature of the device to operate off of a 1.8V or 3.3V microcontroller, regardless of supply voltage.

#### **Rail-to-Rail Input/Output**

The input voltage range of the IC extends 100mV above  $V_{DD}$  and below  $V_{SS}$ . The wide input common-mode voltage range allows the op amp to be used as a buffer and as a differential amplifier in a wide-variety of signal processing applications. Output voltage high/low is designed to be only 50mV above  $V_{SS}$  and below  $V_{DD}$  allowing maximum dynamic range in single-supply applications. The high output current and capacitance drive capability of the device make it ideal as an ADC driver and a line driver.

#### **Input Bias Current**

The IC features a high-impedance CMOS input stage and a specialized ESD structure that allows low-input bias current operation at low-input, common-mode voltages. Low-input bias current is useful when interfacing with high-ohmic sensors. It is also beneficial for designing transimpedance amplifiers for photodiode sensors. This makes the device ideal for ground-referenced medical and industrial sensor applications.

#### **Active Filters**

The MAX44280 is ideal for a wide variety of active filter circuits that makes use of the wide bandwidth, rail-to-rail input/output stages and high-impedance CMOS inputs.

#### **Driver for Interfacing with the MAX11645 ADC**

The IC's tiny size and low noise make it a good fit for driving 12- to 16-bit resolution ADCs in space-constrained applications. The [Typical Application Circuit](#) shows the MAX44280 amplifier output connected to a lowpass filter driving the MAX11645 ADC. The MAX11645 is part of a family of 3V and 5V, 12-bit and 10-bit, 2-channel ADCs.

The MAX11645 offers sample rates up to 94ksps and measures two single-ended inputs or one differential input. These ADCs dissipate 670 $\mu$ A at the maximum sampling rate, but just 6 $\mu$ A at 1ksps and 0.5 $\mu$ A in shutdown. Offered in the ultra-tiny, 1.9mm x 2.2mm WLP and  $\mu$ MAX-8 packages, the MAX11645 ADCs are an ideal fit to pair with the MAX44280 amplifier in portable applications.

Where higher resolution is required, refer to the MAX1069 (14-bit) and MAX1169 (16-bit) ADC families.

# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### **Chip Information**

PROCESS: BiCMOS

### **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX44280AXT+	-40°C to +125°C	6 SC70	+AED
MAX44280AYT+	-40°C to +125°C	6 Thin $\mu$ DFN (Ultra-Thin LGA)	+AZ

+Denotes a lead(Pb)-free/RoHS-compliant package.

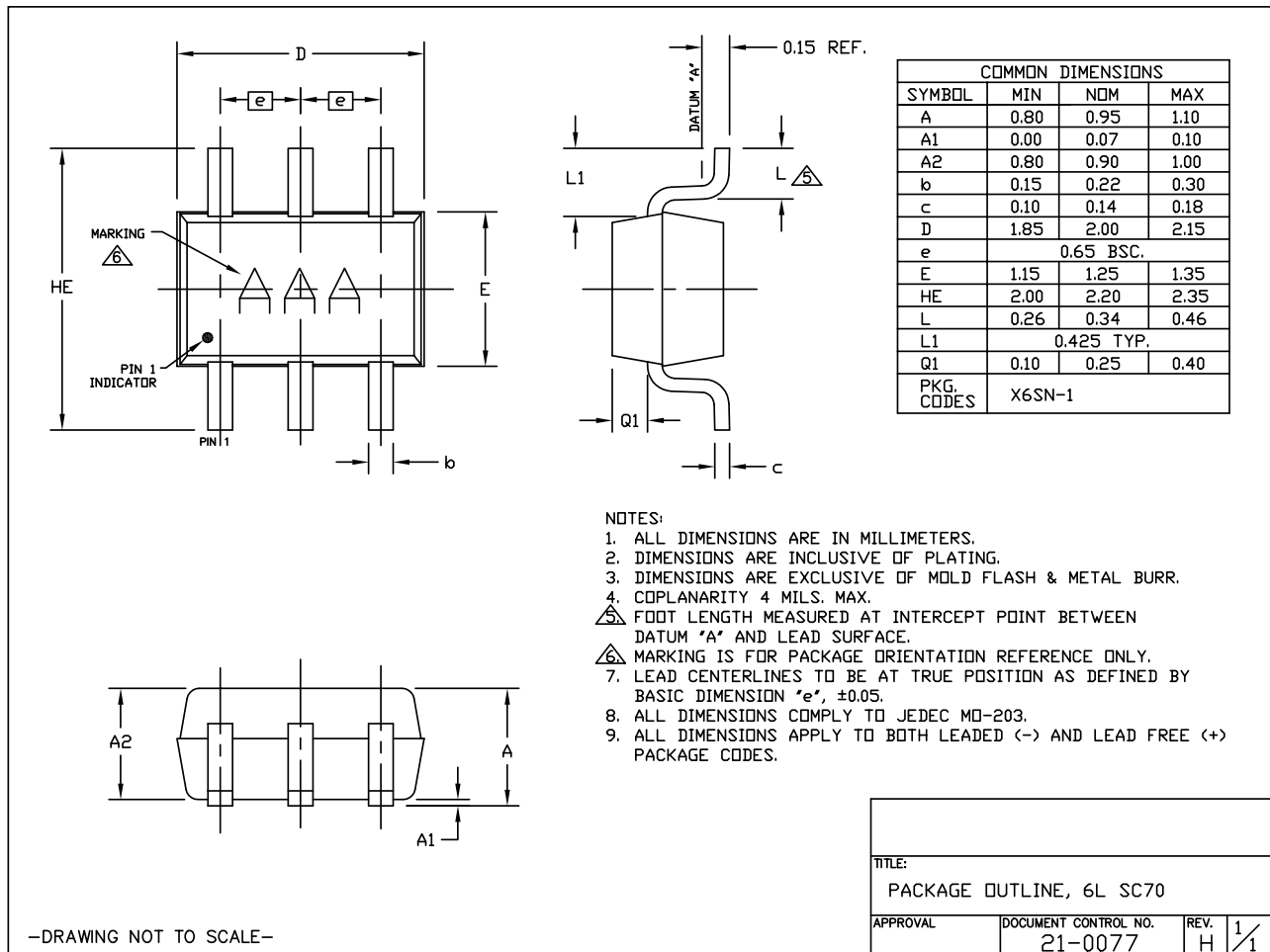
# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 SC70	X6SN+1	<a href="#">21-0077</a>	<a href="#">90-0189</a>
6 Thin $\mu$ DFN (Ultra-Thin LGA)	Y61A1+1	<a href="#">21-0190</a>	<a href="#">90-0233</a>

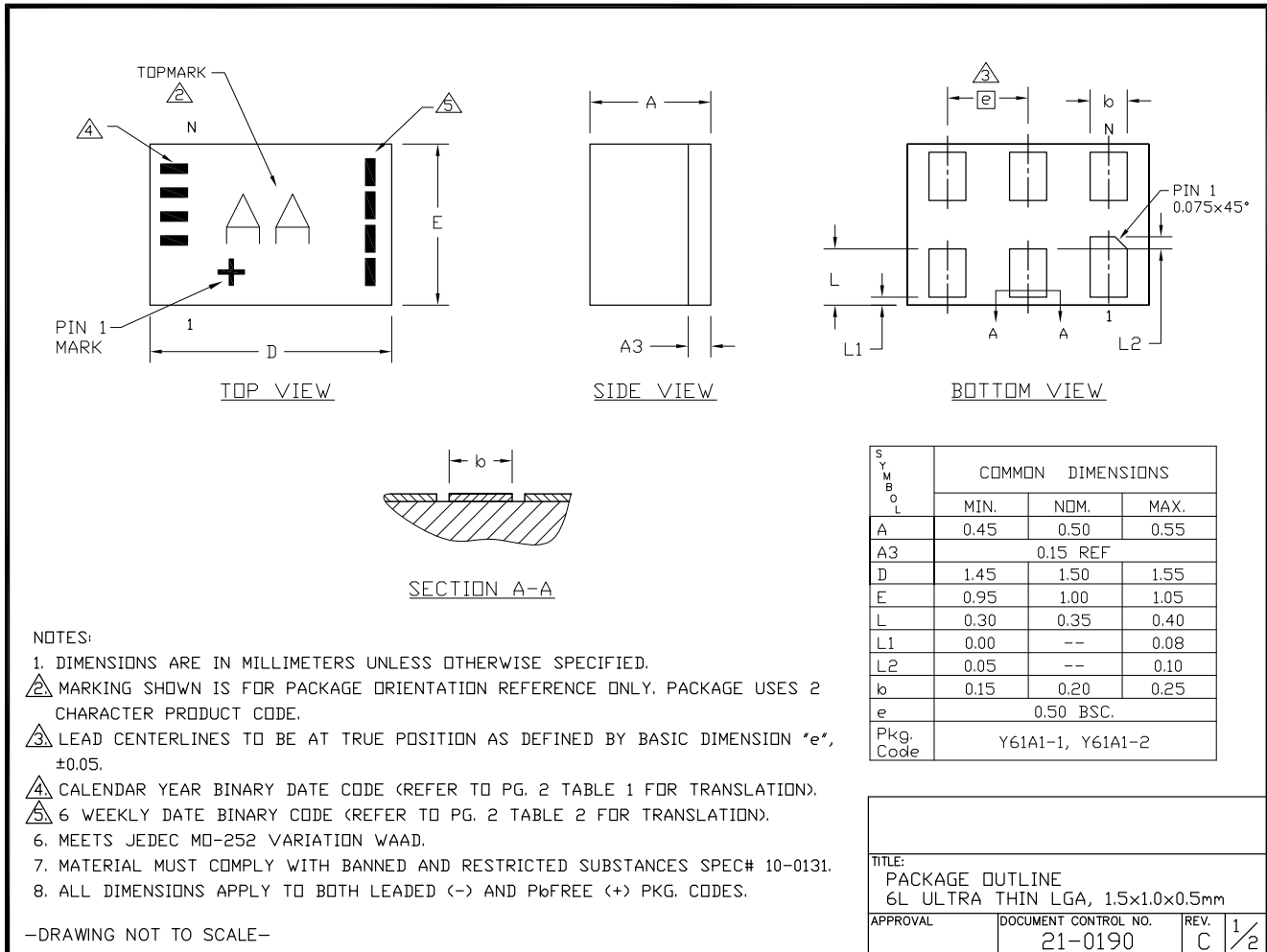


# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### Package Information (continued)

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### Package Information (continued)

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

**TABLE 1** Translation Table for Calendar Year Code

Calendar Year	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
	□	□	□	■	□	□	■	□	■	■
	□	□	■	□	□	■	□	■	□	□
	□	■	□	□	■	□	□	■	■	■
	■	□	□	□	■	■	■	□	□	□

Legend: ■ Marked with bar □ Blank space - no bar required

**TABLE 2** Translation Table for Payweek Binary Coding

Payweek	06-11	12-17	18-23	24-29	30-35	36-41	42-47	48-51	52-05
	□	□	□	■	□	□	■	□	■
	□	□	■	□	□	■	□	■	□
	□	■	□	□	■	□	□	■	■
	■	□	□	□	■	■	■	□	□

Legend: ■ Marked with bar □ Blank space - no bar required

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE 6L ULTRA THIN LGA, 1.5x1.0x0.5mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0190	REV. C	2/2

# MAX44280

## 1.8V, 50MHz, Low-Offset, Low-Power, Rail-to-Rail I/O Op Amp

### Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—
1	4/12	Updated <i>Package Thermal Characteristics, Electrical Characteristics, and Ordering Information.</i>	2, 3, 12
2	8/12	Added Note 3 to <i>Electrical Characteristics.</i>	2, 3



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