



PSMN057-200B

N-channel TrenchMOS SiliconMAX standard level FET

15 August 2013

Product data sheet

1. General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

2. Features and benefits

- Higher operating power due to low thermal resistance
- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

3. Applications

- DC-to-DC converters
- Switched-mode power supplies

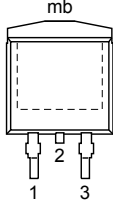
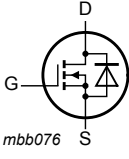
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	200	V
I_D	drain current	$T_{mb} = 25\text{ °C}$	-	-	39	A
P_{tot}	total power dissipation		-	-	250	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 17\text{ A}; T_j = 25\text{ °C}$	-	41	57	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 39\text{ A}; V_{DS} = 160\text{ V}; T_j = 25\text{ °C}$	-	37	50	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>D2PAK (SOT404)</p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN057-200B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN057-200B	PSMN057-200B

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	200	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	200	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{mb} = 100\text{ °C}$	-	27.5	A
		$T_{mb} = 25\text{ °C}$	-	39	A
I_{DM}	peak drain current	pulsed; $T_{mb} = 25\text{ °C}$	-	156	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	250	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C

Symbol	Parameter	Conditions	Min	Max	Unit
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	39	A
I_{SM}	peak source current	pulsed; $T_{mb} = 25\text{ °C}$	-	156	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 35\text{ A}$; $V_{sup} \leq 50\text{ V}$; unclamped; $t_p = 100\text{ }\mu\text{s}$; $R_{GS} = 50\text{ }\Omega$	-	300	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	35	A

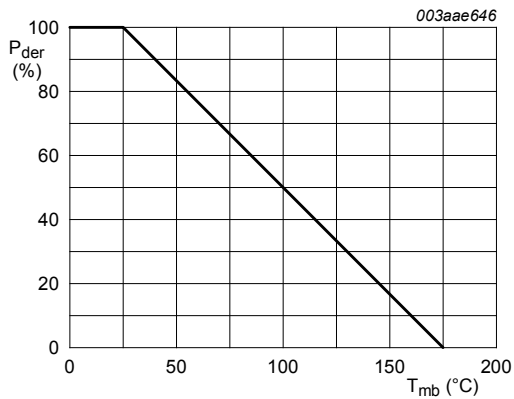


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

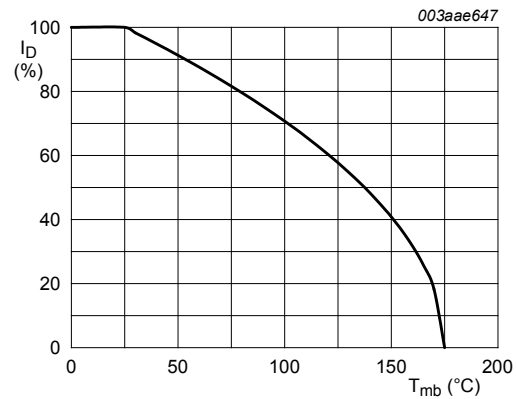
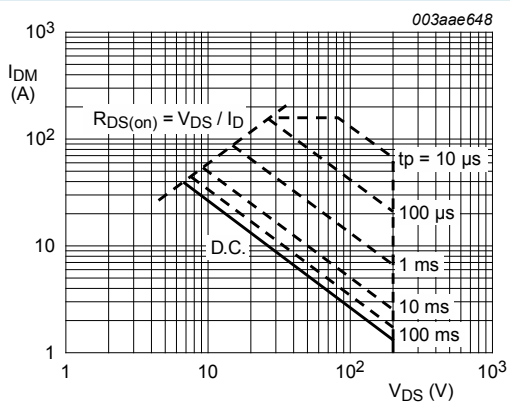


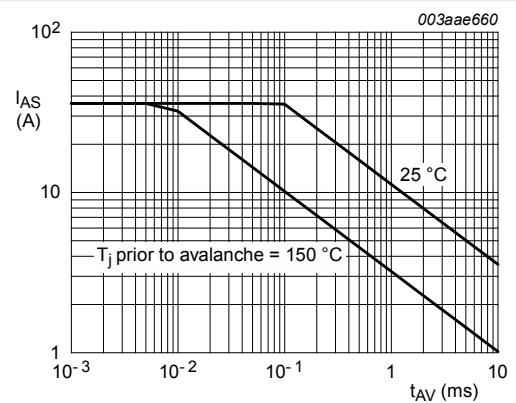
Fig. 2. Normalized continuous drain current as a function of mounting base temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$



$T_{mb} = 25\text{ °C}$; I_{DM} is single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



unclamped inductive load

Fig. 4. Single-shot avalanche rating; avalanche current as a function of avalanche period

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; FR4 board	-	50	-	K/W

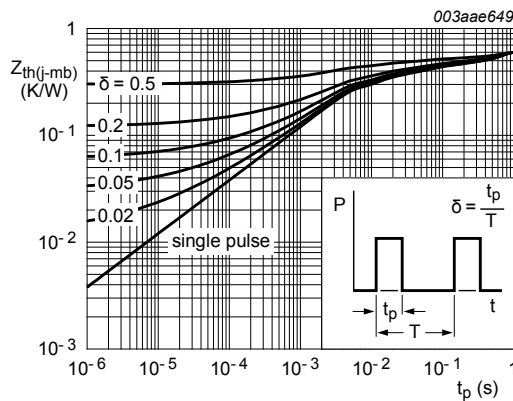


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	200	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	178	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	4.4	V
I_{DSS}	drain leakage current	$V_{DS} = 200 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
		$V_{DS} = 200 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.03	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 17 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	-	165	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 17 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	41	57	m Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	2	4.1	Ω
Dynamic characteristics						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 39 \text{ A}; V_{DS} = 160 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	96	135	nC
Q_{GS}	gate-source charge		-	13	-	nC
Q_{GD}	gate-drain charge		-	37	50	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	3750	5036	pF
C_{oss}	output capacitance		-	385	520	pF
C_{rss}	reverse transfer capacitance		-	180	252	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 100 \text{ V}; R_L = 2.7 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(\text{ext})} = 5.6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	18	-	ns
t_r	rise time		-	58	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	105	-	ns
t_f	fall time		-	78	-	ns
L_D	internal drain inductance	measured from tab to centre of die ; $T_j = 25 \text{ }^\circ\text{C}$	-	3.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad ; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	133	173	ns
Q_r	recovered charge		-	895	-	nC

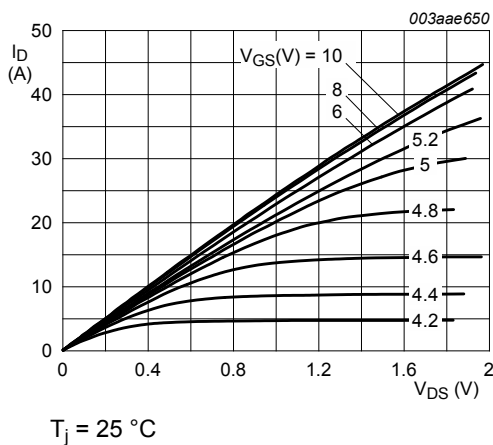


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

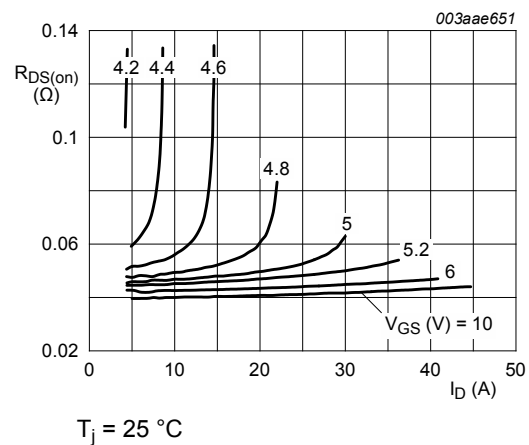
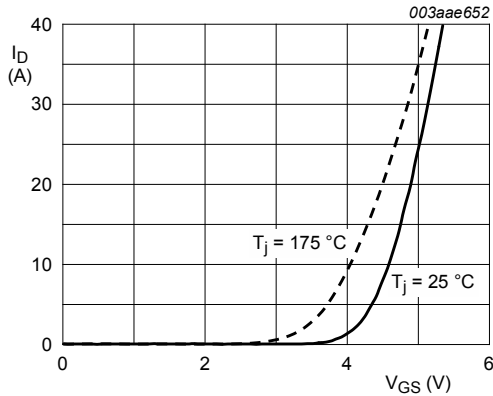
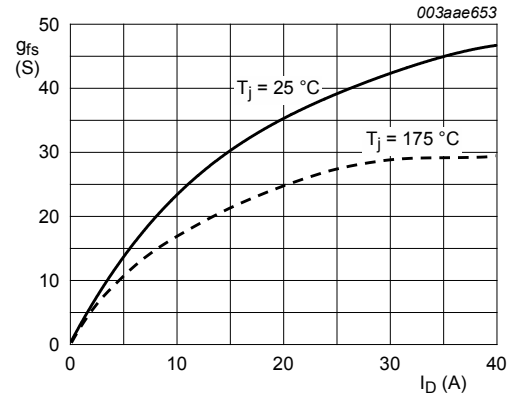


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 9. Forward transconductance as a function of drain current; typical values

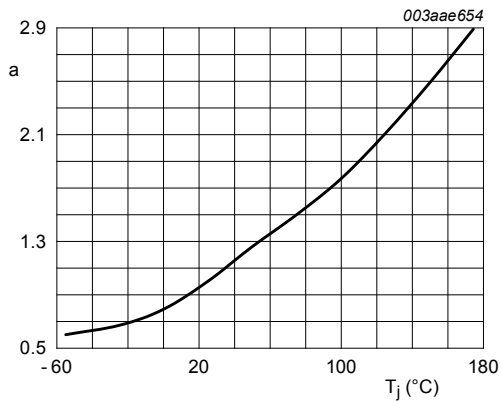
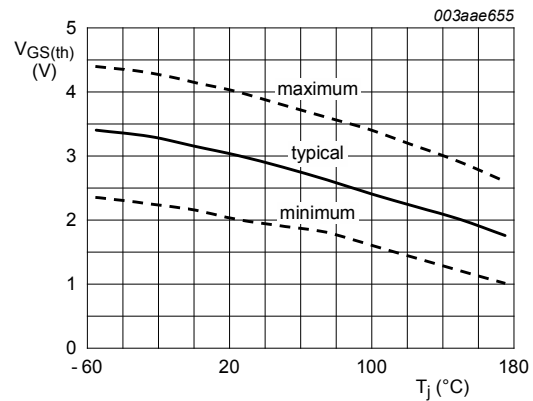


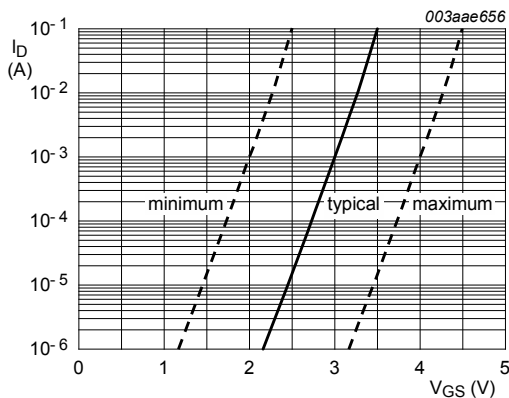
Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



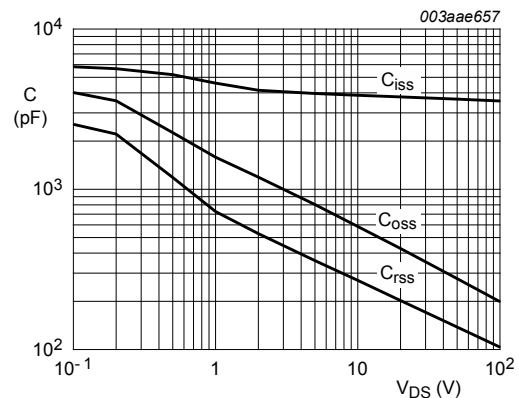
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig. 11. Gate-source threshold voltage as a function of junction temperature



$$T_j = 25^\circ C; V_{DS} = V_{GS}$$

Fig. 12. Sub-threshold drain current as a function of gate-source voltage



$$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

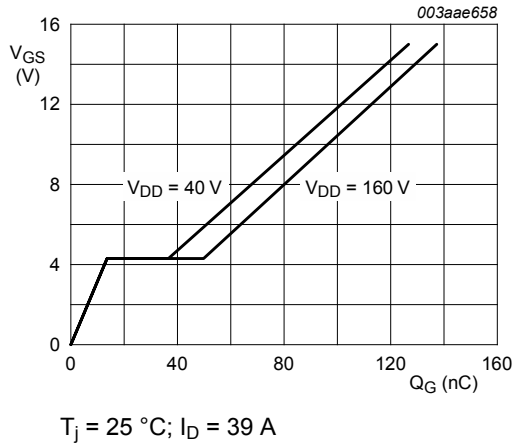


Fig. 14. Gate-source voltage as a function of gate charge; typical values

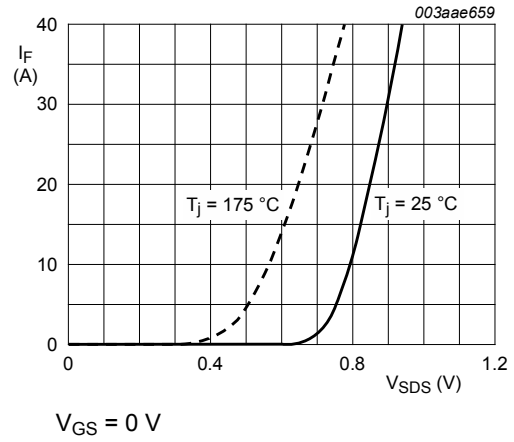
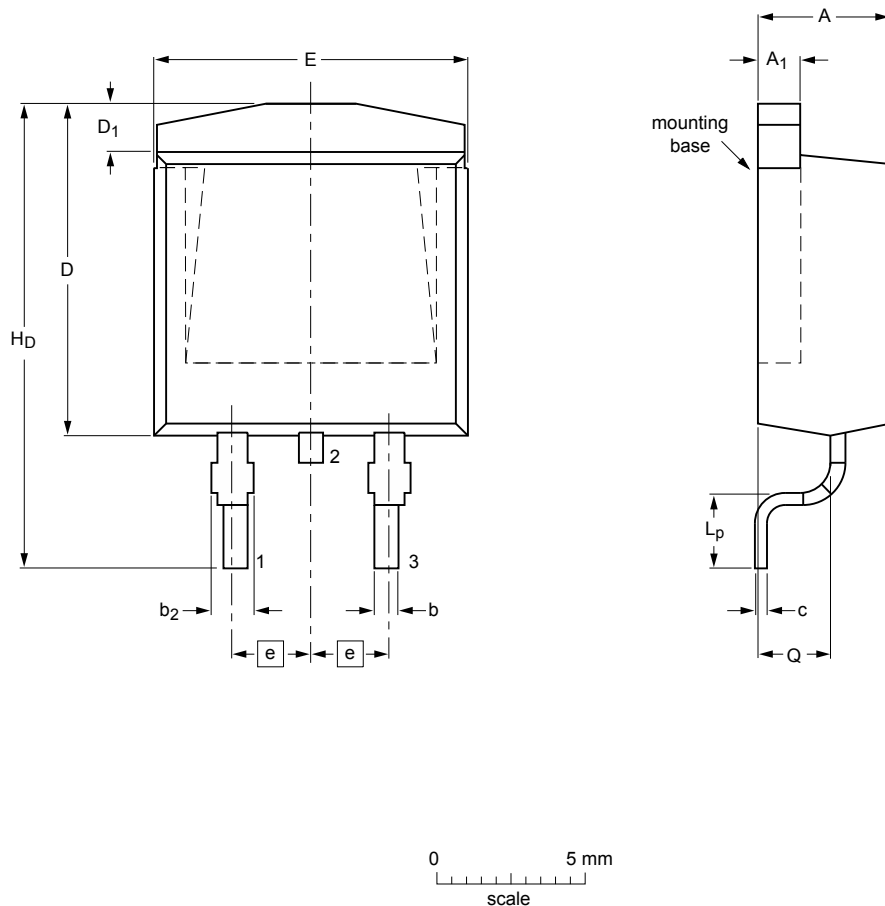


Fig. 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	b ₂	c	D	D ₁	E	e	H _D	L _p	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 16. Package outline D2PAK (SOT404)

12. Legal information

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