Never stop thinking

n-Channel Power MOSFET

OptiMOS™
BSB056N10NN3 G

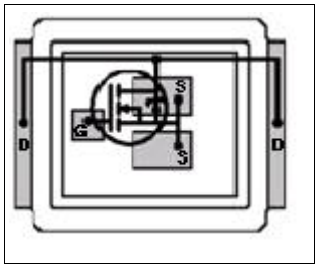
Data Sheet

2.5, 2011-05-27
Final

Industrial & Multimarket

1 Description

OptiMOS™100V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate- and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 100V the best choice forthe demanding requirements of voltage regulator solutions in Solar, Drives, Datacom and Telecom applications. Super fast switching Control FETs together with low EMI Sync FETs provide solutions that are easy to design in. OptiMOS™ products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space- efficiency and cost.



Features

- Optimized for high switching frequency DC/DC converter
- Excellent Q_g x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Double sided cooling
- Compatible with DirectFET® package MN footprint and outline
- Low parasitic inductance
- Low profile (<0.7 mm)

Applications

- Synchronous rectification
- Primary side switches
- Power management for high performance computing
- High power density point of load converters

RoHS

HAL PB

Table 1 Key Performance Parameters

Parameter	Value	Unit		Related Links
V_{DS}	100	V		IFX OptiMOS webpage
$R_{DS(on),max}$	5.6	mΩ		IFX OptiMOS product brief
I_D	83	A		IFX OptiMOS spice models
Q_{OSS}	73	nC		IFX Design tools
$Q_{g,typ}$	56			

Type	Package	Marking
BSB056N10NN3 G	MG-WDSON-2	0110

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	83	A	V_{GS}=10 V, T_C=25 °C
				52		V_{GS}=10 V, T_C=100 °C
				9		V_{GS}=10 V, T_A=25 °C, R_{thJA}=45 K/W)[1]
Pulsed drain current[2]	$I_{D,pulse}$	-	-	332		T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	450	mJ	I_D=30 A,R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	
Power dissipation	P_{tot}	-	-	78	W	T_C=25 °C
				2.8		T_A=25 °C, R_{thJA}=45[1] K/W
Operating and storage temperature	T_j,T_{stg}	-40	-	150	°C	
IEC climatic category; DIN IEC 68-1		55/150/56				

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

2) See figure 3 for more detailed information

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.6	K/W	top
		-	1	-		bottom
Device on PCB	R_{thJA}	-	-	45		6 cm^2 cooling area[1]

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70µ, thick) copper area for drain conneciton. PCB is vertical in still air.

4 Electrical characteristics

Electrical characteristics, at Tj=25 °C, unless otherwise specified.

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2	2.7	3.5		V_{DS}=V_{GS}, I_D=100 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	10	µA	V_{DS}=100V, V_{GS}=0 V, T_j=25 °C
		-	10	100		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	5	5.6	mΩ	V_{GS}=10 V, I_D=30A
			6.2	8.1		V_{GS}=6 V, I_D=15A
Gate resistance	R_G	-	0.5	-	Ω	
Transconductance	g_{fs}	34	69		S	|V_{DS}|>2|$I_{D\|RDS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4100	5500	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance	C_{oss}	-	750	1000		
Reverse transfer capacitance	C_{rss}	-	27	-		
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	V_{DD}=50V, V_{GS}=10 V, I_D=30 A, R_G= 1.6 Ω
Rise time	t_r	-	9	-		
Turn-off delay time	$t_{d(off)}$	-	25	-		
Fall time	t_f	-	8	-		

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	17	-	nC	V_{DD}=50 V, I_D=30 A, V_{GS}=0 to 10 V
	Q_{gd}		9.7			
Gate to drain charge	Q_{sw}	-	20	-		
Switching charge	Q_g	-	56	74		
Gate charge total	$V_{plateau}$	-	4.2	-	V	
Output charge	Q_{oss}		73	97	nC	V_{DD}=50 V, V_{GS}=0 V

1) See figure 16 for gate charge parameter definition

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_s			65	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			316		
Diode forward voltage	V_{SD}	-	0.9	1.2	V	V_{GS}=0 V, I_F=I_S, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	174	-	nC	V_R=50V, I_F=*30A*, di_F/dt=100 A/µs
Reverse recovery time	t_{rr}	-	64	-	ns	

5 Electrical characteristics diagrams

Table 8

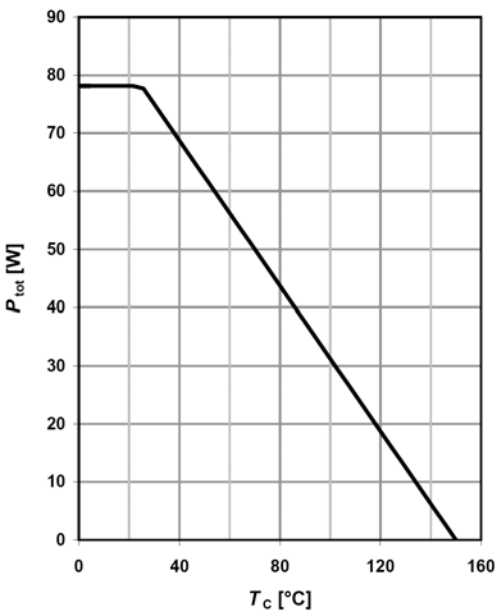
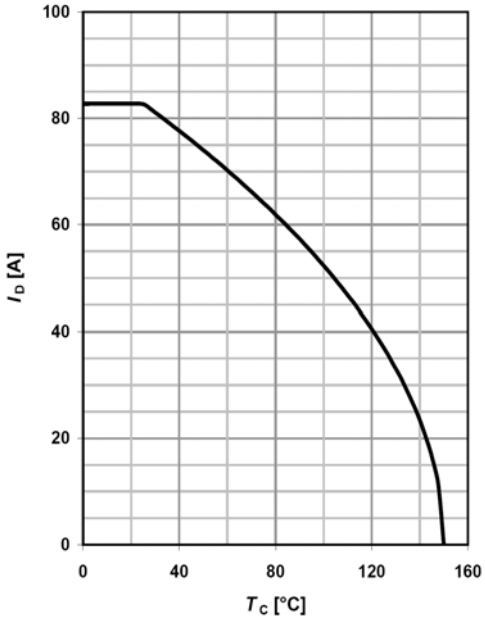
1 Power dissipation	2 Drain current
	
P_{tot} = f(T_C)	I_D=$f(T_C)$; parameter:V_{GS}

Table 9

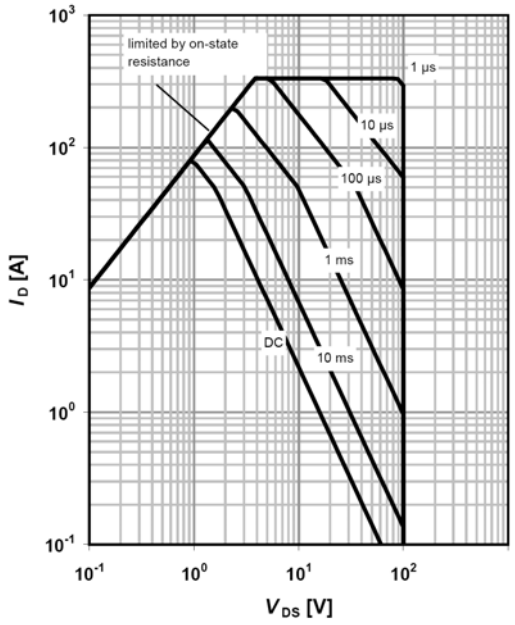
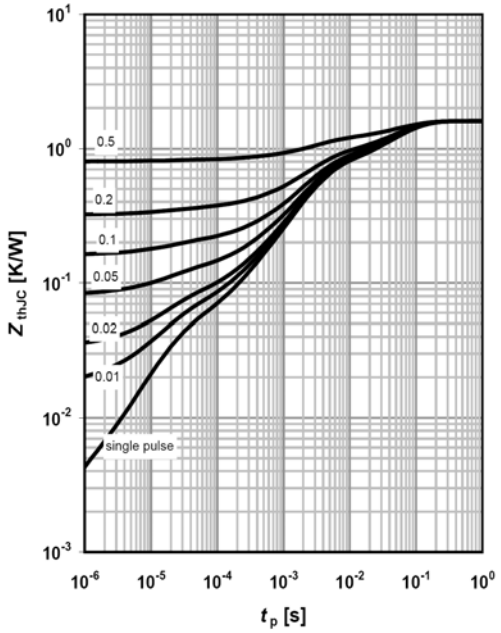
3 Safe operating area T_C=25 °C	4 Max. transient thermal impedance
	
I_D=f(V_{DS}); T_j=25 °C; D=0; parameter: T_p	$Z_{(thJC)}$=f(t_p); parameter: D=t_p/T

Table 10

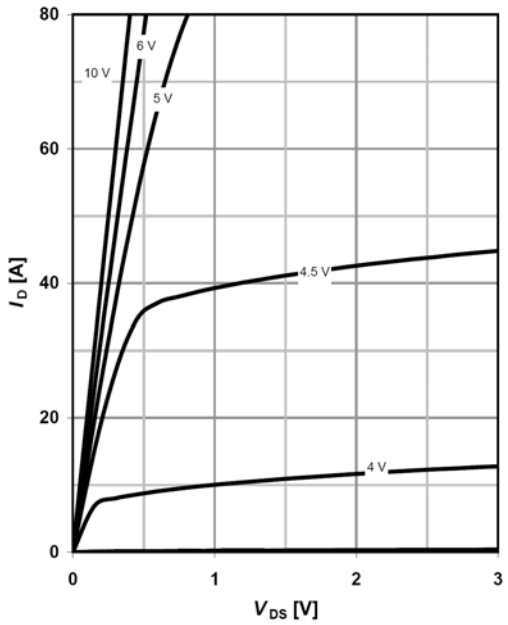
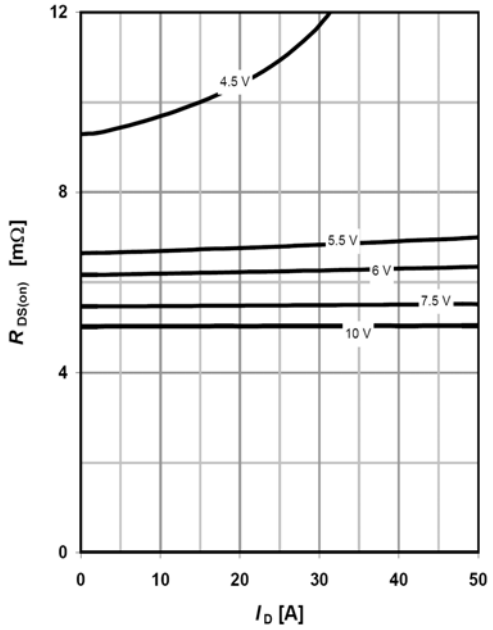
5 Typ. output characteristics T_C=25 °C	6 Typ. drain-source on-state resistance
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Table 11

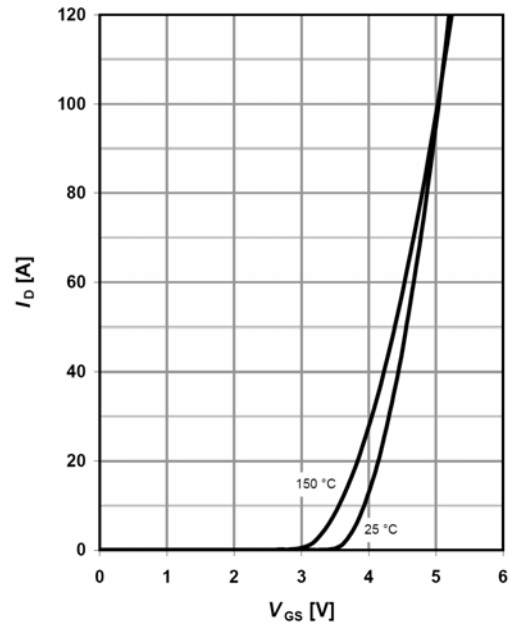
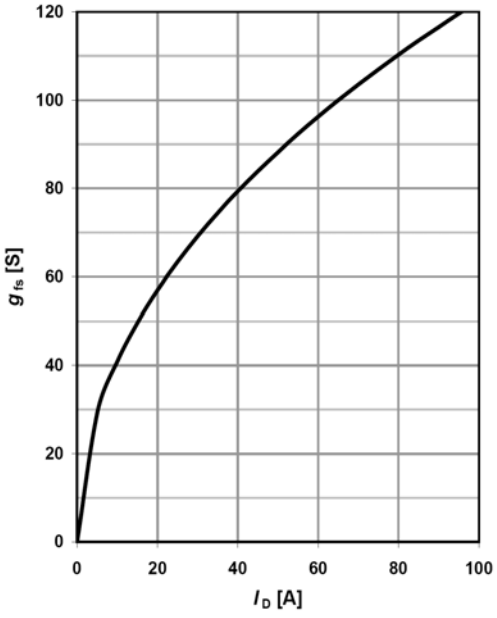
7 Typ. transfer characteristics	8 Typ. forward transconductance
	
I_D=f(VGS); |V_{DS}|>2|I_D|$R_{DS(on)max}$	g_{fs}=f(I_D); T_j=25 °C

Table 12

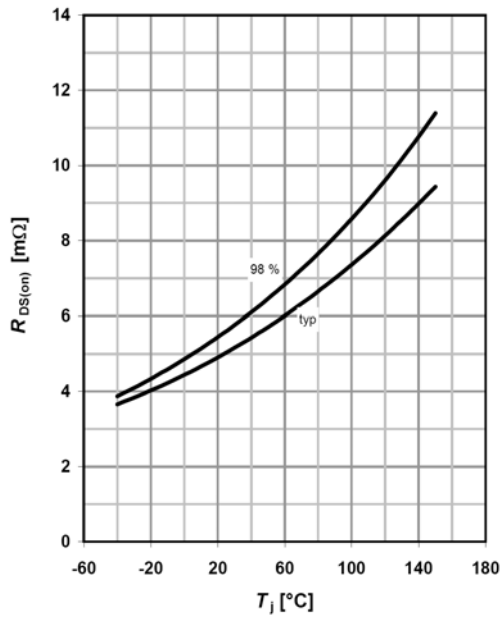
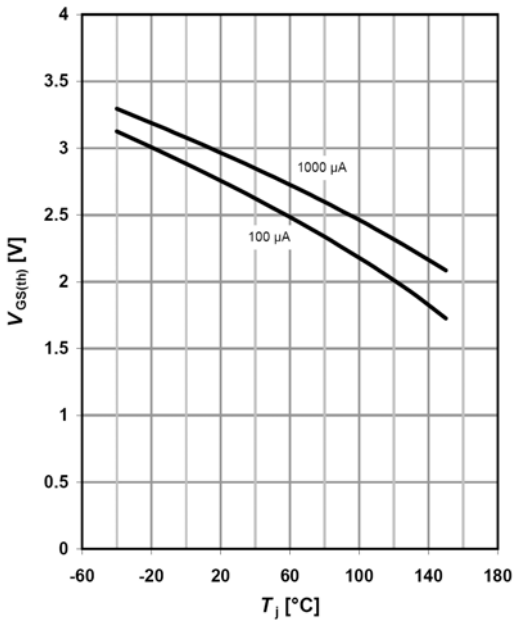
9 Drain-source on-state resistance	10 Typ. gate threshold voltage
	
$R_{DS(on)}=f(T_j)$; I_D=30 A; V_{GS}=10 V	$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$;

Table 13

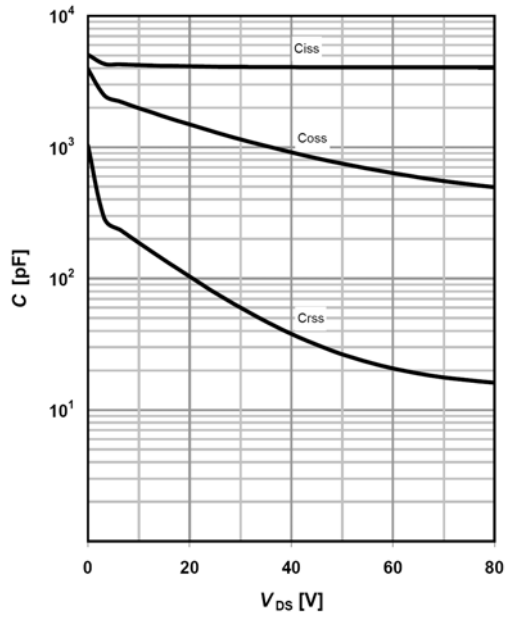
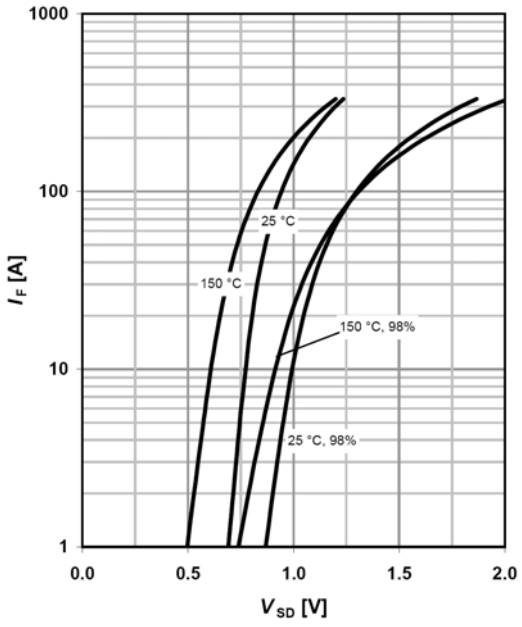
11 Typ. capacitances	12 Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	$I_F=f(V_{SD})$; parameter: T_j

Table 14

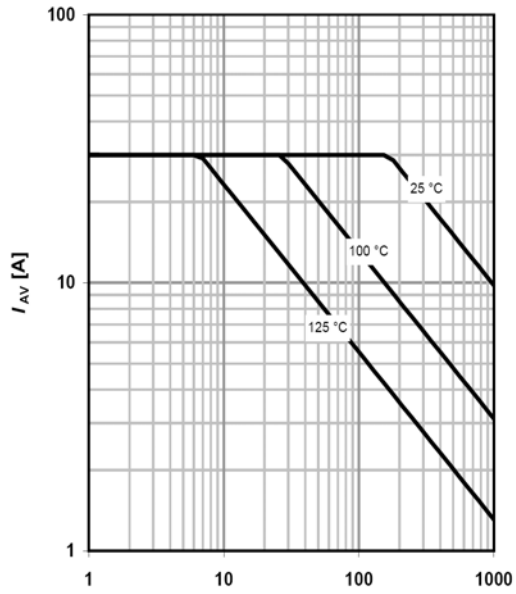
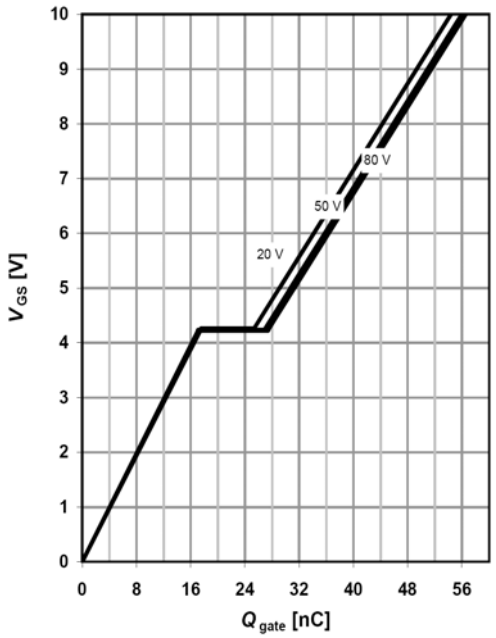
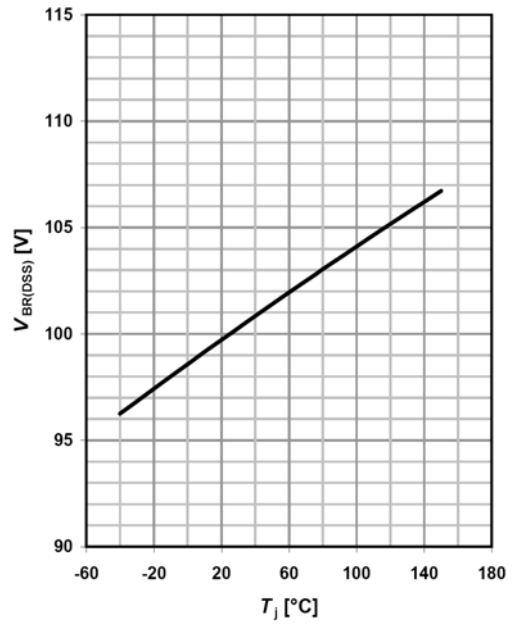
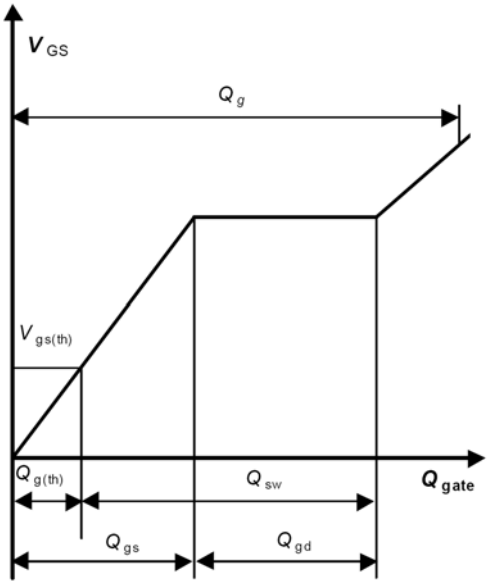
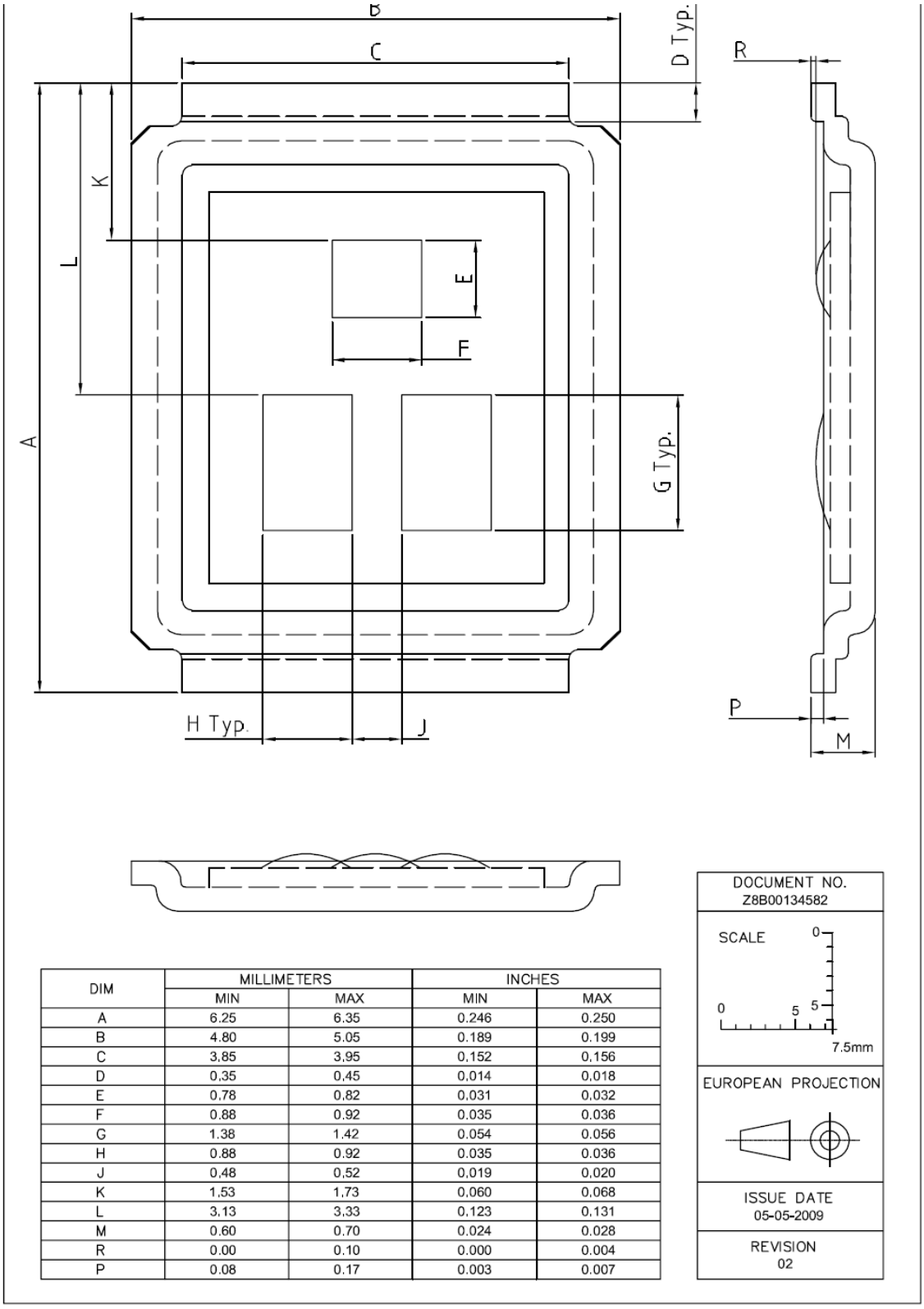
13 Avalanche characteristics	14 Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$	V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Table 15

15 Drain-source breakdown voltage	16 Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	

6 Package outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3,85	3,95	0,152	0,156
D	0,35	0,45	0,014	0,018
E	0,78	0,82	0,031	0,032
F	0.88	0.92	0.035	0.036
G	1.38	1.42	0.054	0.056
H	0.88	0.92	0.035	0.036
J	0,48	0,52	0,019	0,020
K	1,53	1,73	0,060	0,068
L	3,13	3,33	0,123	0,131
M	0.60	0.70	0.024	0.028
R	0.00	0.10	0.000	0.004
P	0.08	0.17	0.003	0.007

Figure 1 Outlines MG-WDSON-2, dimensions in mm/inches

7 Package outlines

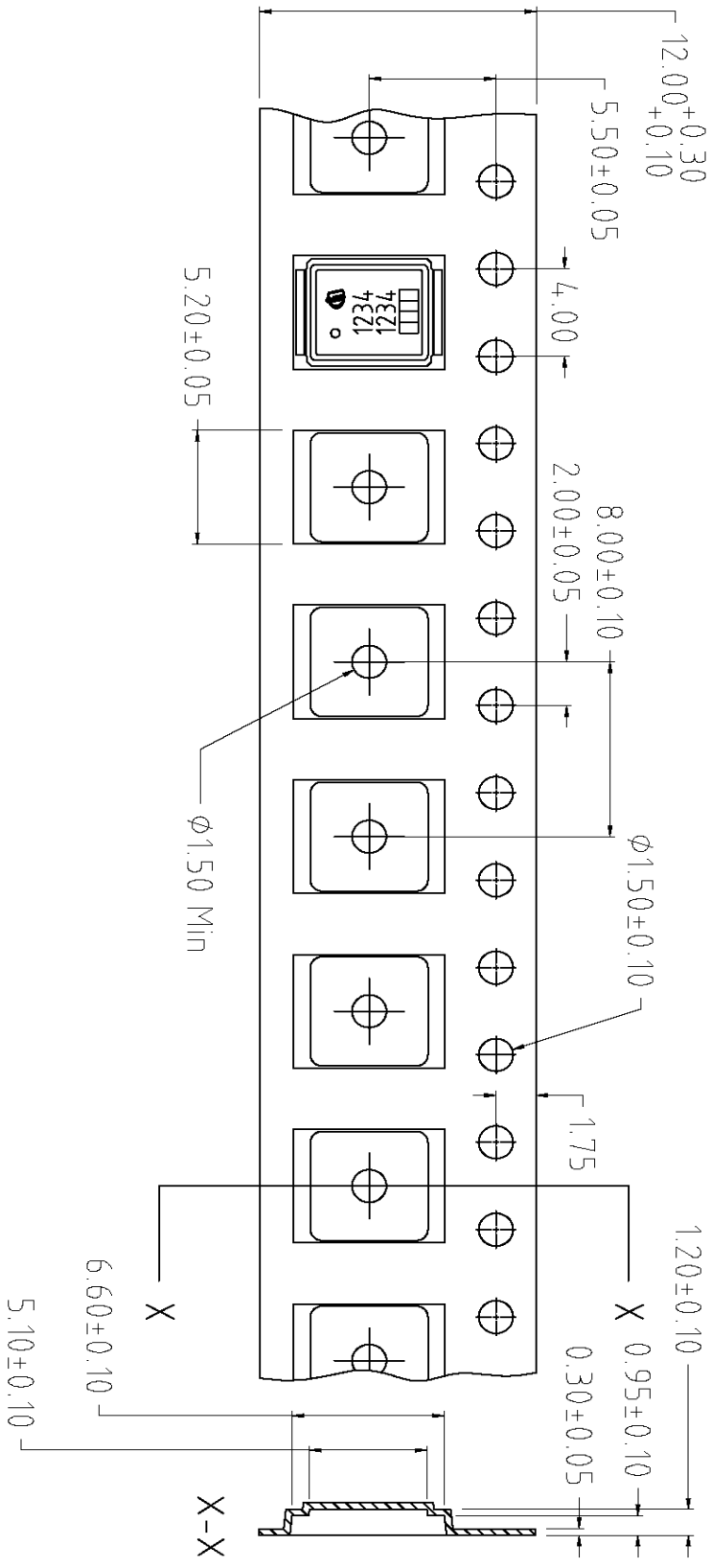
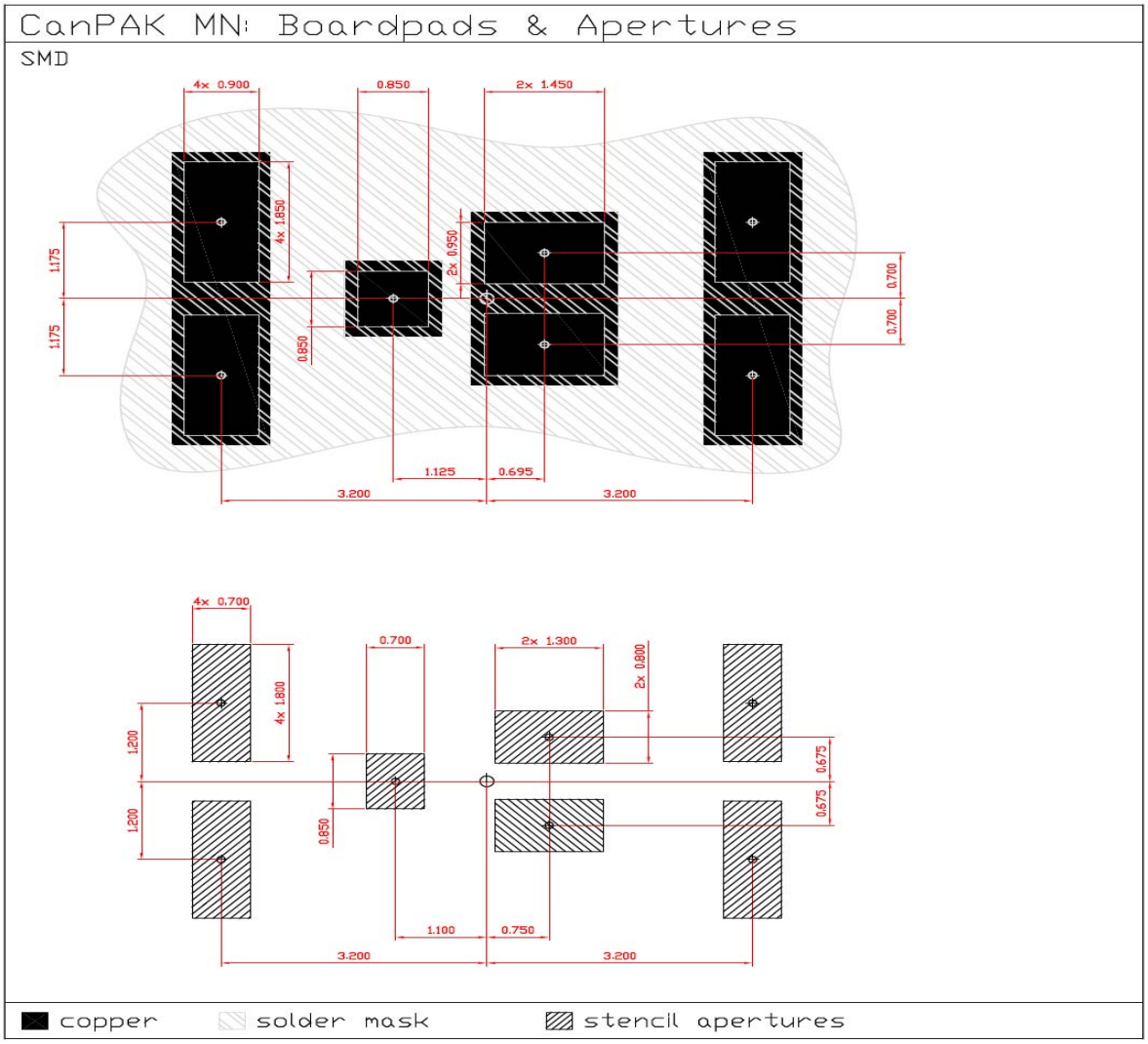


Figure 2 Outlines MG-WDSON-2, dimensions in mm/inches

8 Package outlines



9 Package outlines

9 Revision History

Revision History: 2011-05-27, 2.5

Previous Revision:

Revision	Subjects (major changes since last revision)
0.1	Release of target data sheet
2.0	Release of Final data sheet
2.3	Package outlines errata corrections
2.4	DirectFET Disclaimer expired

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