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Kind regards,

Team Nexperia

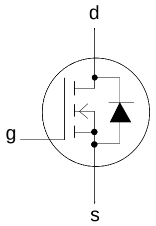
N-channel enhancement mode TrenchMOS™ transistor

BSP100

FEATURES

- **'Trench'** technology
- Low on-state resistance
- Fast switching
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 30 V

I_D = 6 A

$R_{DS(ON)} \leq 100\ m\Omega$ (V_{GS} = 10 V)

$R_{DS(ON)} \leq 200\ m\Omega$ (V_{GS} = 4.5 V)

GENERAL DESCRIPTION

N-channel enhancement mode field-effect transistor in a plastic envelope using '**trench**' technology.

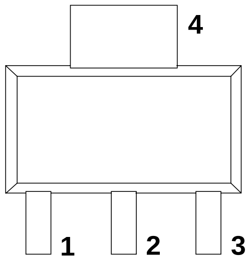
Applications:-
- Motor and relay drivers
- d.c. to d.c. converters
- Logic level translator

The BSP100 is supplied in the SOT223 surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

SOT223



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 150˚C	-	30	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 150˚C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	T_{sp} = 25 ˚C	-	6[1]	A
		T_{sp} = 100 ˚C	-	4.4	A
		T_{amb} = 25 ˚C	-	3.2	A
I_{DM}	Pulsed drain current	T_{sp} = 25 ˚C	-	24	A
P_D	Total power dissipation	T_{sp} = 25 ˚C	-	8.3	W
T_j, T_{stg}	Operating junction and storage temperature		- 65	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point	surface mounted, FR4 board	12	15	K/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	surface mounted, FR4 board	70	-	K/W

1 Continuous current rating limited by package

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_{AS} = 6 A; t_p = 0.2 ms; T_j prior to avalanche = 25˚C; V_{DD} ≤ 15 V; R_{GS} = 50 Ω; V_{GS} = 10 V	-	23	mJ
I_{AS}	Non-repetitive avalanche current		-	6	A

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 10 µA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	2	2.8	V
		T_j = 150˚C	0.4	-	-	V
		T_j = -55˚C	-		3.2	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.2 A	-	80	100	mΩ
		V_{GS} = 4.5 V; I_D = 1 A	-	120	200	mΩ
		V_{GS} = 10 V; I_D = 2.2 A; T_j = 150˚C	-	-	170	mΩ
g_{fs}	Forward transconductance	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	-	S
$I_{D(ON)}$	On-state drain current	V_{GS} = 10 V; V_{DS} = 1 V;	3.5	-	-	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	-	-	A
I_{DSS}	Zero gate voltage drain current	V_{DS} = 24 V; V_{GS} = 0 V;	-	10	100	nA
		V_{DS} = 24 V; V_{GS} = 0 V; T_j = 150˚C	-	0.6	10	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2.3 A; V_{DD} = 15 V; V_{GS} = 10 V	-	6	-	nC
Q_{gs}	Gate-source charge		-	0.7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	0.7	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 20 V; R_D = 18 Ω;	-	6	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 6 Ω	-	8	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	21	-	ns
t_f	Turn-off fall time		-	15	-	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz	-	250	-	pF
C_{oss}	Output capacitance		-	88	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{sp} = 25 ˚C	-	-	6	A
I_{SM}	Pulsed source current (body diode)		-	-	24	A
V_{SD}	Diode forward voltage	I_F = 1.25 A; V_{GS} = 0 V	-	0.82	1.2	V
t_{rr}	Reverse recovery time	I_F = 1.25 A; $-dI_F/dt$ = 100 A/µs;	-	69	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 25 V	-	55	-	nC

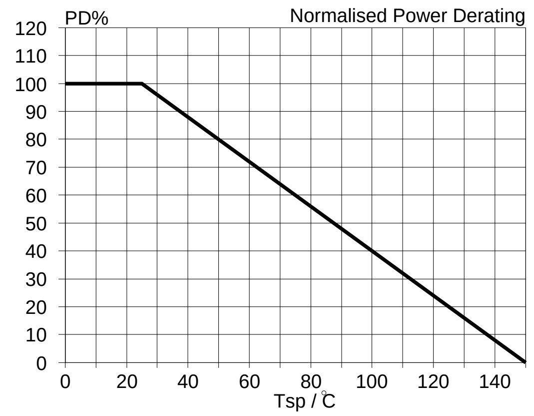


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ˚C} = f(T_{sp})$

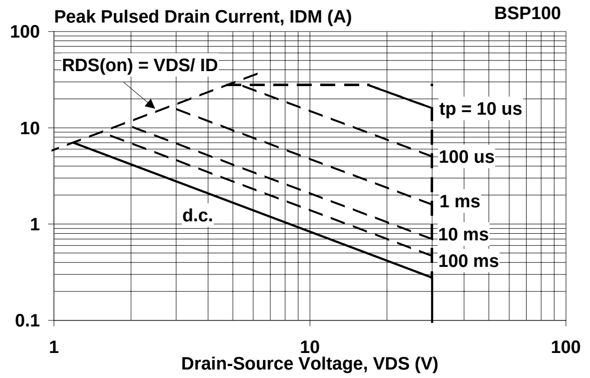


Fig.3. Safe operating area. T_{sp} = 25 ˚C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

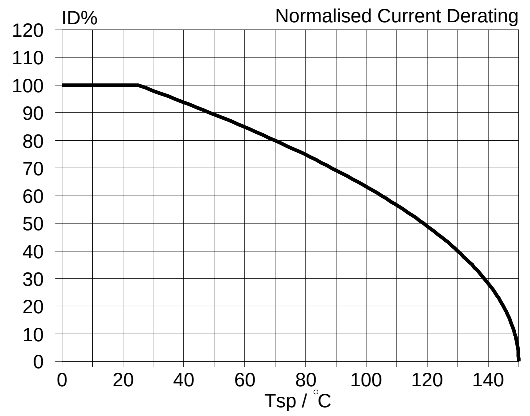


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ˚C} = f(T_{sp})$; conditions: $V_{GS} \geq 10$ V

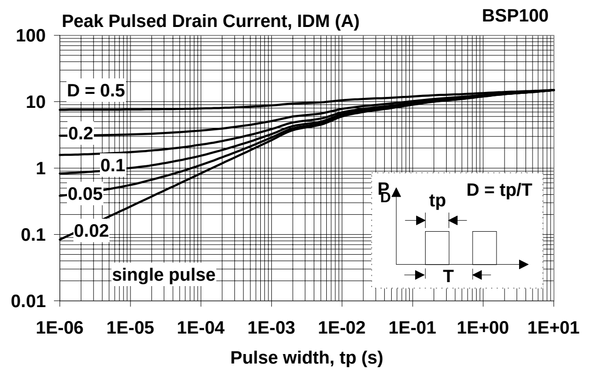


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp} = f(t)$; parameter $D = t_p/T$

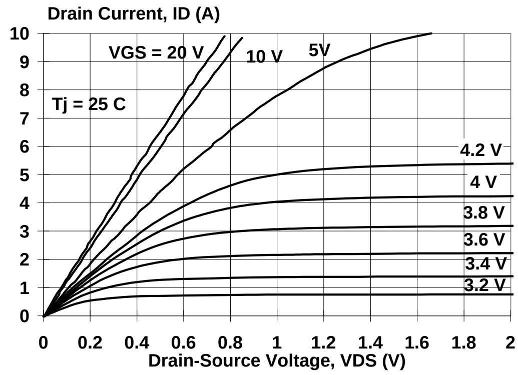


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

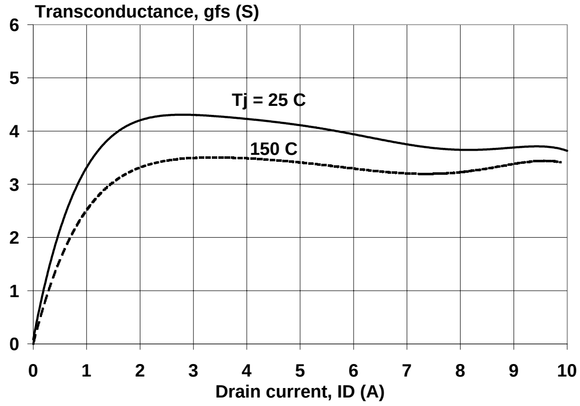


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; parameter T_j

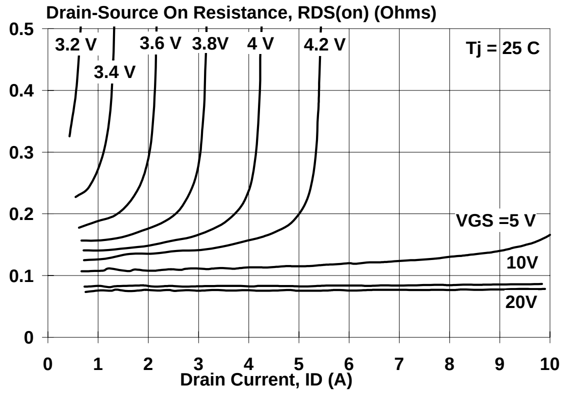


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

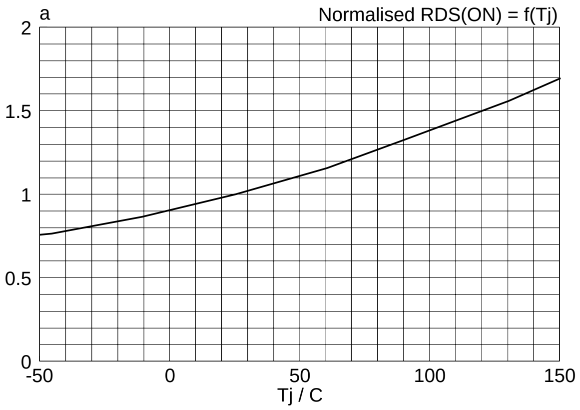


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$

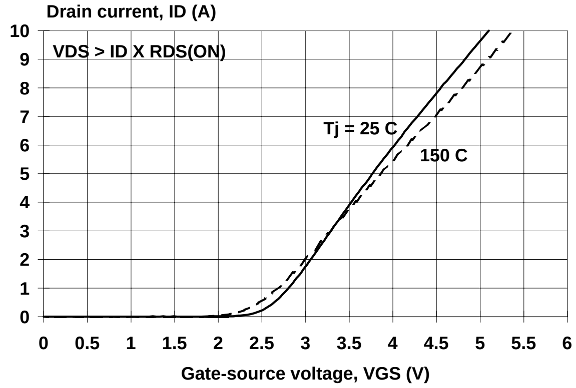


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

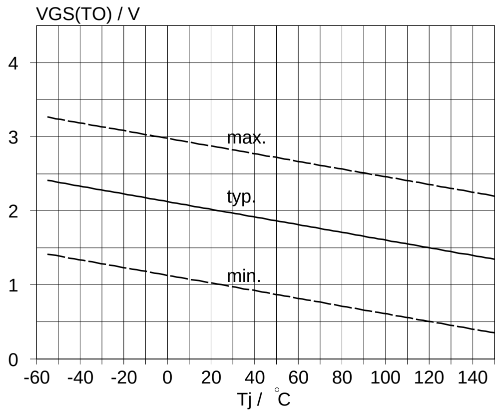


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

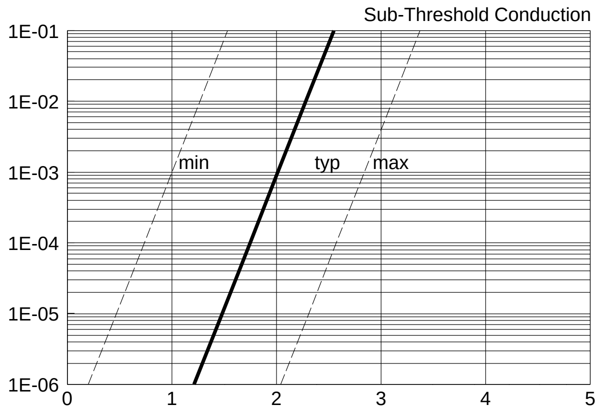


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

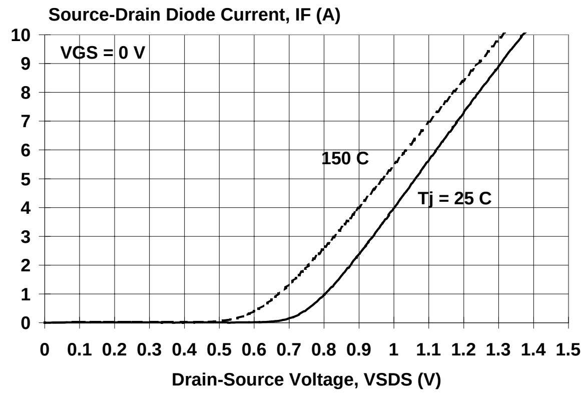


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

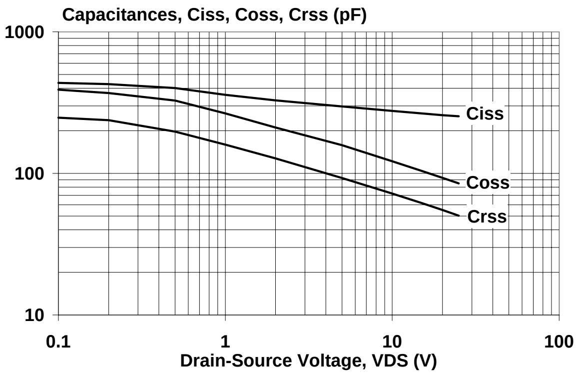


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; f = 1 MHz

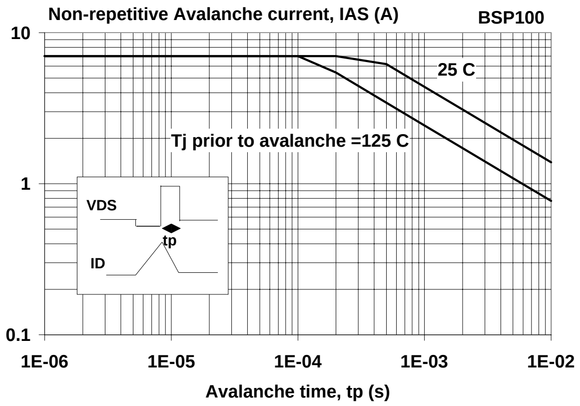


Fig.15. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_p); unclamped inductive load

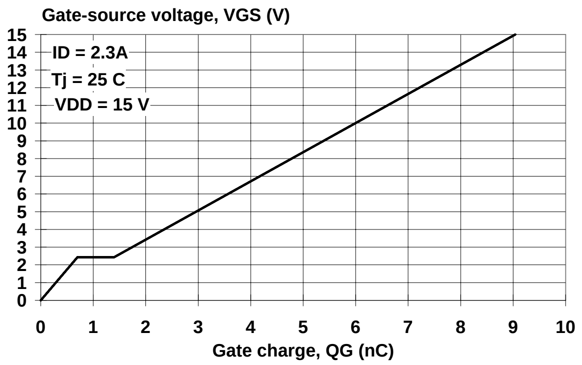


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

PRINTED CIRCUIT BOARD

Dimensions in mm.

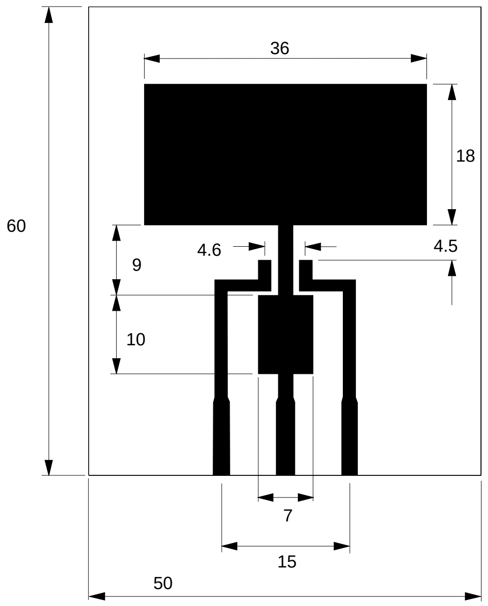
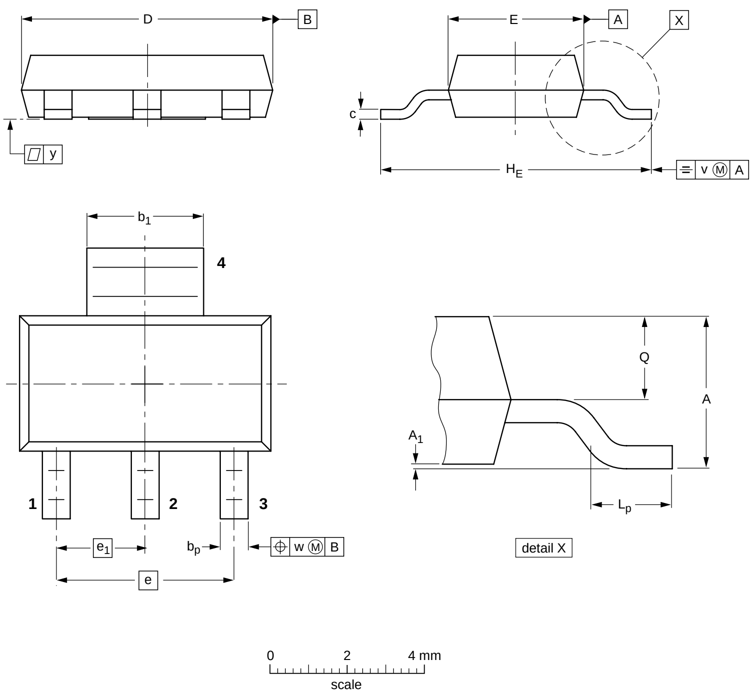


Fig.16. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).

MECHANICAL DATA

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28

Fig.17. SOT223 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Discrete Semiconductor Packages, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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