**Product data sheet** 

## 1. General description

Planar passivated SCR with sensitive gate in a SOT223 surface mountable plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

#### 2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

## 3. Applications

- Circuit breakers
- RCD/GFI/LCCB applications

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DRM}$	repetitive peak off- state voltage		[1]	-	-	600	V
V <sub>RRM</sub>	repetitive peak reverse voltage			-	-	600	V
I <sub>TSM</sub>	non-repetitive peak on- state current	half sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 10 \text{ ms}$ ; Fig. 4; Fig. 5		-	-	8	A
I <sub>T(AV)</sub>	average on-state current	half sine wave; T <sub>sp</sub> ≤ 112 °C; <u>Fig. 1</u>		-	-	0.63	Α
I <sub>T(RMS)</sub>	RMS on-state current	half sine wave; $T_{sp} \le 112 ^{\circ}\text{C}$ ; Fig. 2; Fig. 3		-	-	1	A
Static characte	eristics						
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 10 \text{ mA}; T_j = 25 ^{\circ}\text{C};$ Fig. 9		20	50	200	μΑ

<sup>[1]</sup> Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state.





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# 5. Pinning information

### Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	4	A <del>-                                   </del>
2	Α	anode		G sym037
3	G	gate		3
4	mb	mb; connected to anode	□1 □2 □3 SC-73 (SOT223)	

# 6. Ordering information

#### Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
BT168GW	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223			

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# 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		[1]	-	600	V
$V_{RRM}$	repetitive peak reverse voltage			-	600	V
I <sub>T(AV)</sub>	average on-state current	half sine wave; T <sub>sp</sub> ≤ 112 °C; <u>Fig. 1</u>		-	0.63	Α
I <sub>T(RMS)</sub>	RMS on-state current	half sine wave; $T_{sp} \le 112 ^{\circ}\text{C}$ ; Fig. 2; Fig. 3		-	1	А
I <sub>TSM</sub>	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 10 \text{ ms}$ ; Fig. 4; Fig. 5		-	8	А
		half sine wave; $T_{j(init)} = 25 ^{\circ}C$ ; $t_p = 8.3  ms$		-	9	А
I <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN		-	0.32	A <sup>2</sup> s
dl <sub>T</sub> /dt	rate of rise of on-state current	$I_T = 2 \text{ A}$ ; $I_G = 10 \text{ mA}$ ; $dI_G/dt = 100 \text{ mA}/\mu s$		-	50	A/µs
I <sub>GM</sub>	peak gate current			-	1	Α
$V_{RGM}$	peak reverse gate voltage			-	5	V
P <sub>GM</sub>	peak gate power			-	2	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period		-	0.1	W
T <sub>stg</sub>	storage temperature			-40	150	°C
Tj	junction temperature			-	125	°C

<sup>[1]</sup> Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state.

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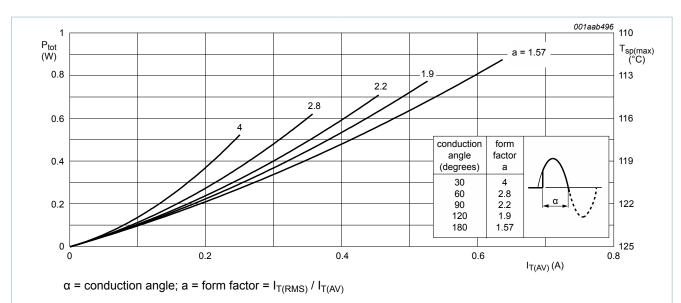


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

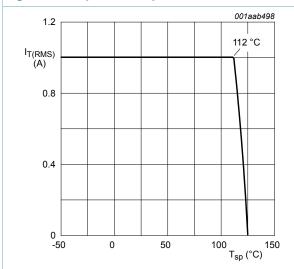
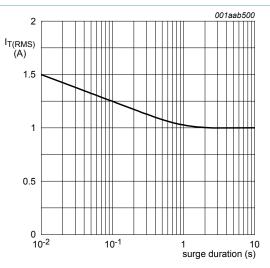


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values



 $f = 50 \text{ Hz}; T_{sp} = 112 \,^{\circ}\text{C}$ 

Fig. 3. RMS on-state current as a function of surge duration; maximum values

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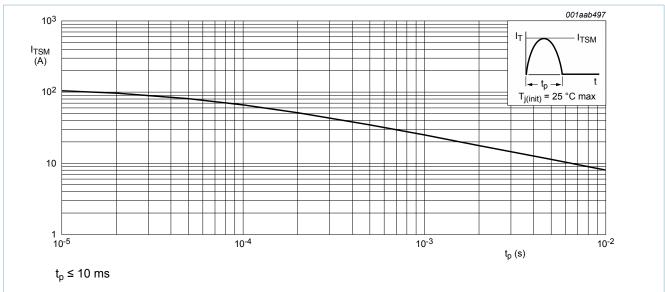


Fig. 4. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

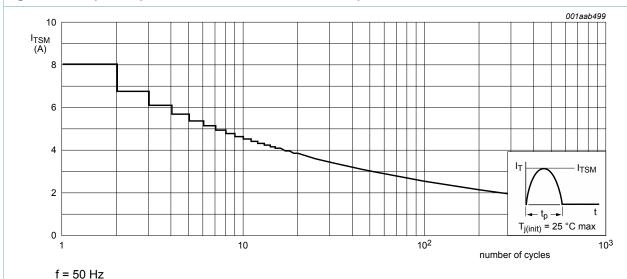


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point	Fig. 6	-	-	15	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to	printed circuit board mounted; minimum footprint; Fig. 7	-	156	-	K/W
	ambient	printed circuit board mounted; pad area; Fig. 8	-	70	-	K/W

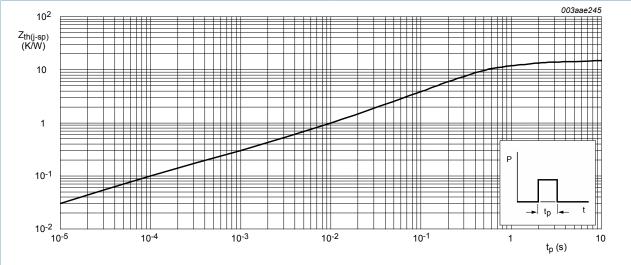
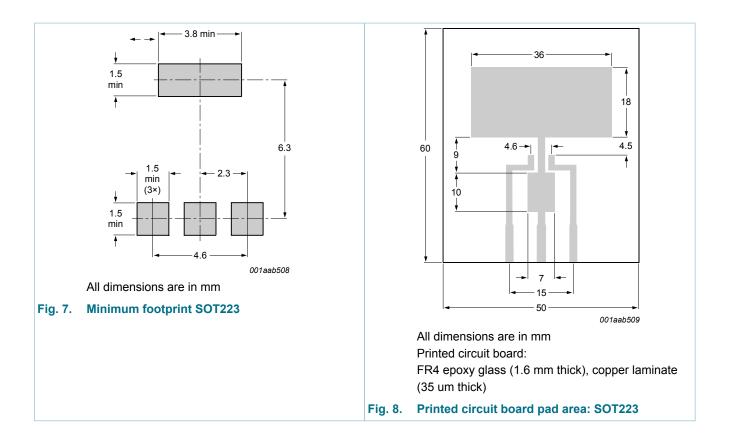


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width

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## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 10 \text{ mA}; T_j = 25 \text{ °C};$ Fig. 9	20	50	200	μA
l <sub>L</sub>	latching current	$V_D$ = 12 V; $I_G$ = 0.5 mA; $R_{GK}$ = 1 k $\Omega$ ; $T_j$ = 25 °C; Fig. 10	-	2	6	mA
I <sub>H</sub>	holding current	$V_D = 12 \text{ V}; R_{GK} = 1 \text{ k}\Omega; T_j = 25 \text{ °C};$ Fig. 11	-	2	5	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 1.2 A; T <sub>j</sub> = 25 °C; <u>Fig. 12</u>	-	1.25	1.7	V
$V_{GT}$	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 10 \text{ mA}; T_j = 25 \text{ °C};$ Fig. 13	-	0.5	0.8	V
		$V_D = 600 \text{ V}; I_T = 10 \text{ mA}; T_j = 125 ^{\circ}\text{C}$	0.2	0.3	-	V
I <sub>D</sub>	off-state current	$V_D = 600 \text{ V}; T_j = 125 \text{ °C}; R_{GK} = 1 \text{ k}\Omega$	-	0.05	0.1	mA
I <sub>R</sub>	reverse current	$V_R = 600 \text{ V}; T_j = 125 \text{ °C}; R_{GK} = 1 \text{ k}\Omega$	-	0.05	0.1	mA
Dynamic c	haracteristics	1				
	rate of rise of off-state voltage	$V_{DM}$ = 402 V; $T_j$ = 125 °C; $R_{GK}$ = 1 k $\Omega$ ; $(V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; Fig. 14	500	800	-	V/µs
		$V_{DM}$ = 402 V; $T_j$ = 125 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; gate open circuit; Fig. 14	-	25	-	V/µs
t <sub>gt</sub>	gate-controlled turn-on time	$I_{TM}$ = 2 A; $V_D$ = 600 V; $I_G$ = 10 mA; $dI_G/$ dt = 0.1 A/µs; $T_j$ = 25 °C	-	2	-	μs
t <sub>q</sub>	commutated turn-off time	$\begin{split} &V_{DM} = 402 \text{ V}; \text{ T}_j = 125 \text{ °C}; \text{ I}_{TM} = 1.6 \text{ A}; \\ &V_R = 35 \text{ V}; (\text{dI}_T/\text{dt})_M = 30 \text{ A/µs}; \text{dV}_D/\\ &\text{dt} = 2 \text{ V/µs}; \text{ R}_{GK} = 1 \text{ k}\Omega; (\text{V}_{DM} = 67\% \text{ of } \\ &V_{DRM}) \end{split}$	-	100	-	μs

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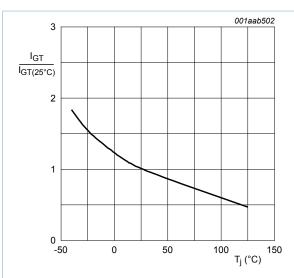


Fig. 9. Normalized gate trigger current as a function of junction temperature

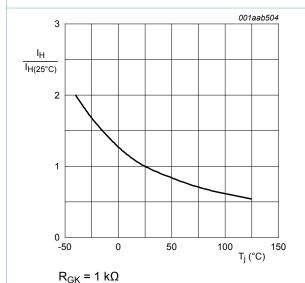
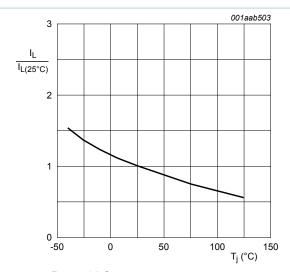
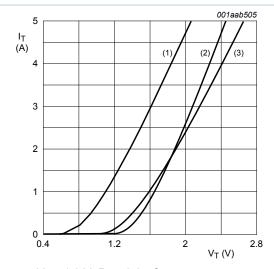


Fig. 11. Normalized holding current as a function of junction temperature



 $R_{GK} = 1 k\Omega$ 

Fig. 10. Normalized latching current as a function of junction temperature



 $V_0 = 1.0 \text{ V}; R_s = 0.27 \Omega$ 

(1) T<sub>i</sub> = 125 °C; typical values

(2) T<sub>i</sub> = 125 °C; maximum values

(3) T<sub>i</sub> = 25 °C; maximum values

Fig. 12. On-state current as a function of on-state voltage

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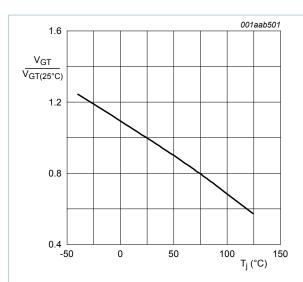


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

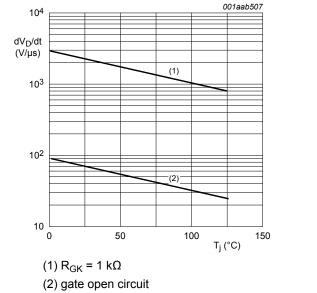
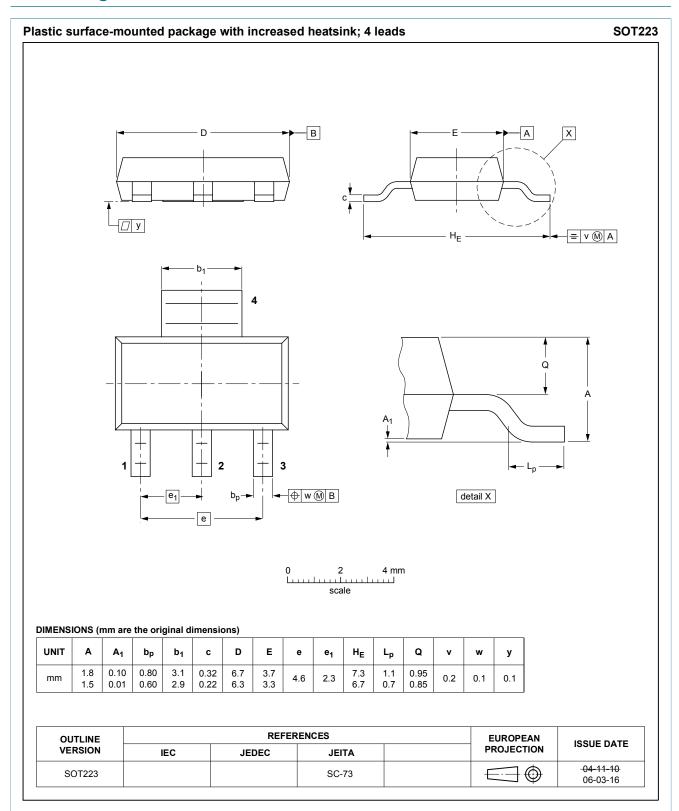


Fig. 14. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

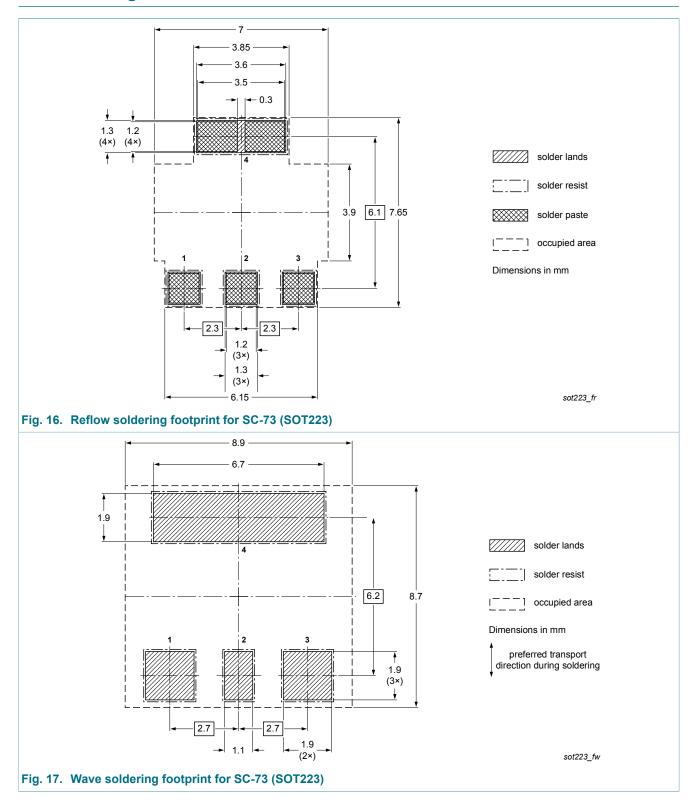
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# 10. Package outline



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## 11. Soldering



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### 12. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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