BATRON

Specification for
BTHQ 21605V-FSTF-I2C-COG

Version October 2003

DOCUMENT REVISION HISTORY 1:

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A	2003.10.16	First release.	SUNNY LEE	MICHAEL TSE

CONTENTS

Specification
of
LCD Module Type
Model No.: COG-BTHQ21605-01

1. General Description

- 16 characters (5x 8 dots) x 2 lines FSTN Positive Black & White Translective LCD Character module.
- Driving scheme: 1:18 multiplexed drive, 1/4 bias.
- Optimal view direction: 6 O'clock.
- Driving IC: 'PHILIPS' PCF 2119RU/2/F2 COG form LCD controller/driver.
- Data interface: I^2C-bus.
- RTV coating.
- White LED05 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	74.5(W) x 29.8(H) x 4.5(D) (Excluded pins, backlight terminals and epoxy)	mm
Viewing area	61.0(W) x 15.8(H)	mm
Active area	56.20(W) x 11.50(H)	mm
Display format	16 characters (5 x 8 dots) x 2 lines	-
Character size	2.95(W) x 5.553(H)	mm
Character spacing	0.60(W) x 0.394(H)	mm
Character pitch	3.55(W) x 5.947(H)	mm
Dot size	0.578(W) x 0.681(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.593(W) x 0.696(H)	mm
Weight	Approx. 13.0	grams

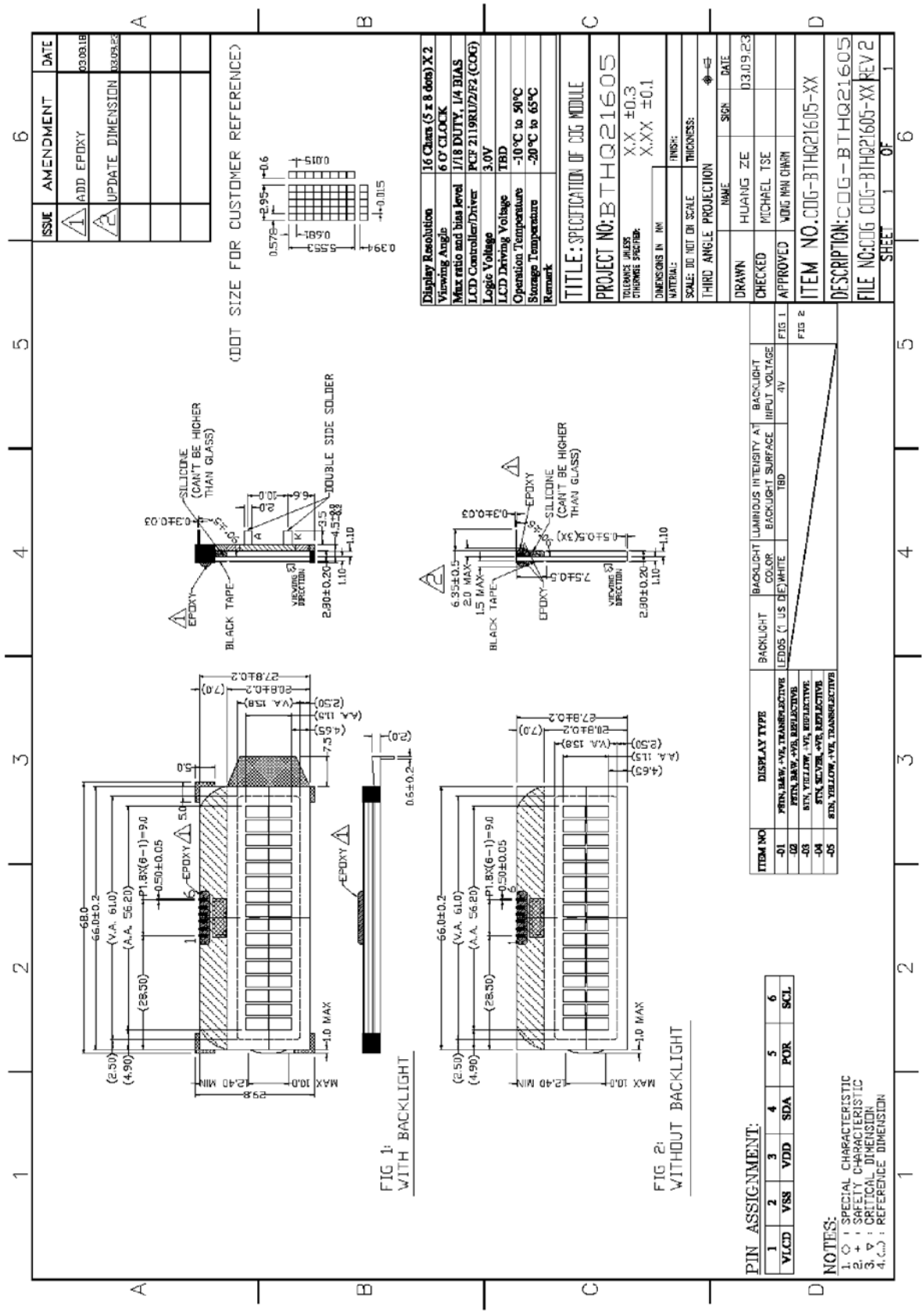


Figure 1 and Figure 2: Specification Drawing

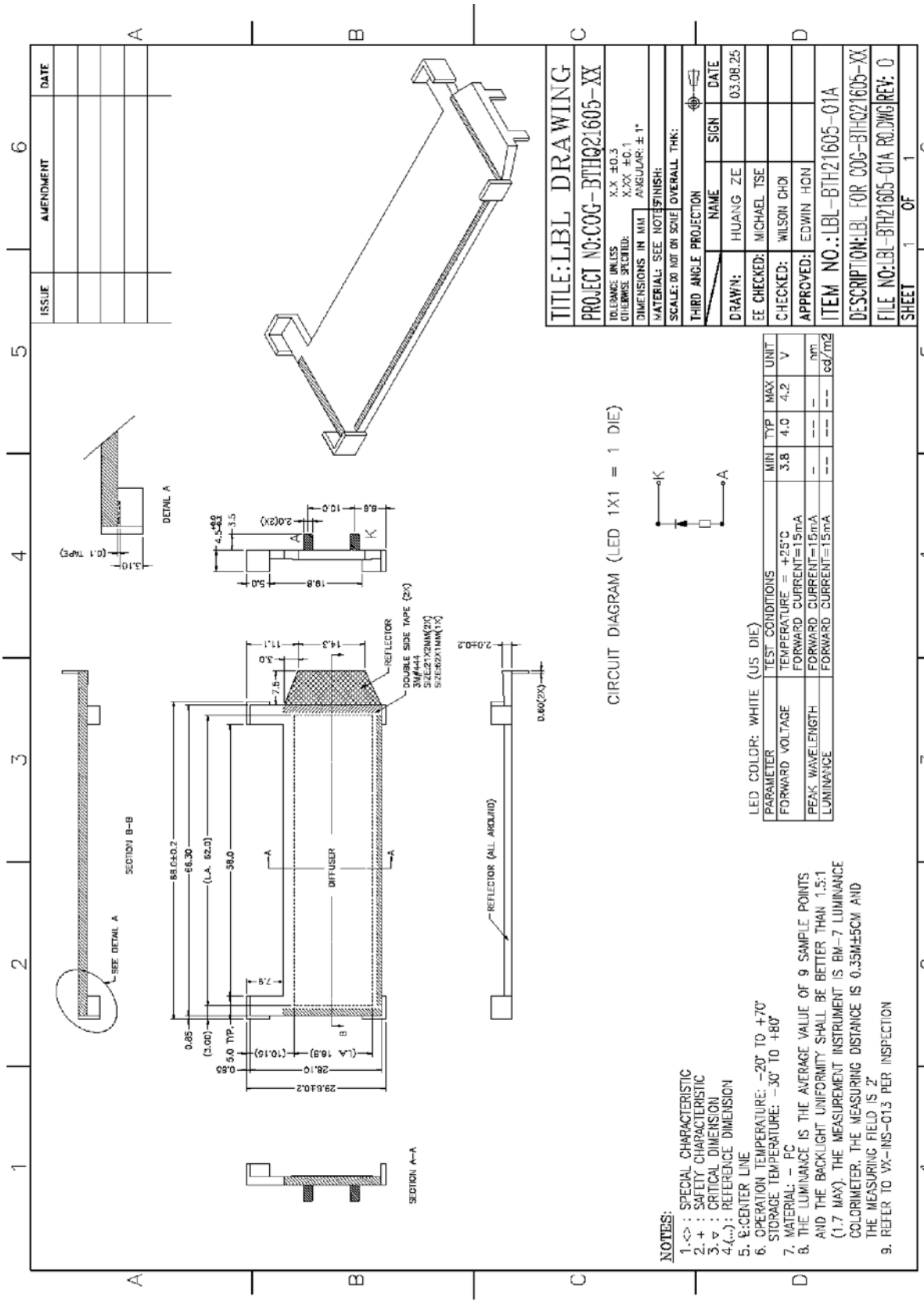


Figure 3: Backlight Drawing

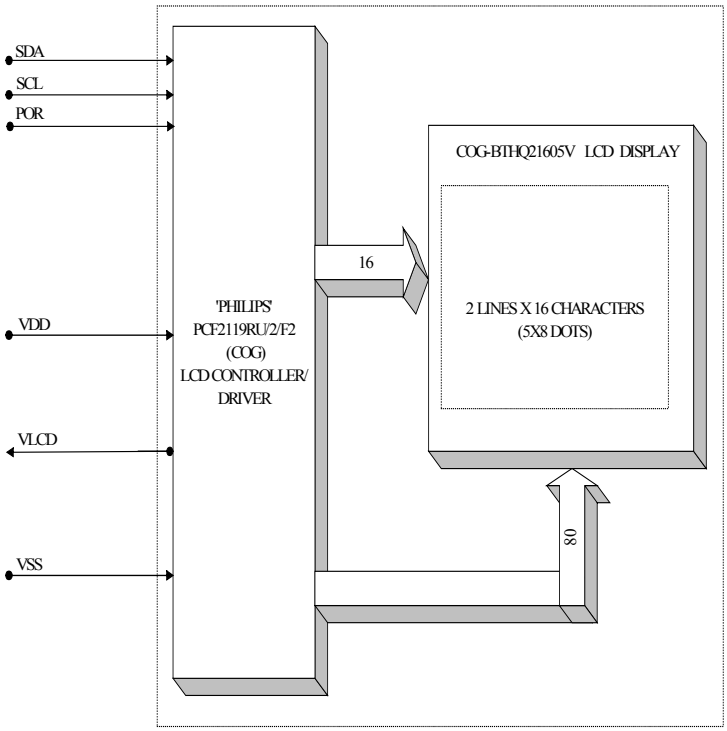
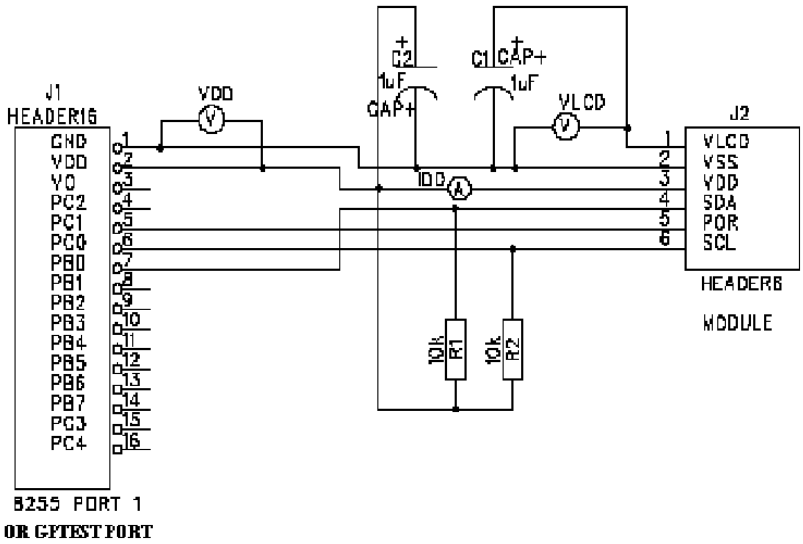


Figure 4: Block Diagram



NOTES

1. VLCD is measured between pin 1 (VLCD) & pin 2 (VSS) of module

2. IDD is measured in series between pin 2 (VDD) of 8255 or gptest
   and pin 3 (VDD) of module

3. VDD=3V is measured between pin 2 (VDD) & pin 1 (GND) of 8255 or gptest

Figure 5: Reference Circuit

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VLCD	LCD driver voltage
2	VSS	Ground (0V)
3	VDD	Power supply for logic.
4	SDA	I^2C serial data input/output
5	POR	External power –on reset input. Active High.
6	SCL	I^2C serial clock input

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings (Ta = 25 ºC)

Table 3

Parameter	Condition	Symbol	Min.	Max.	Unit
Supply voltage range (Logic)	-	VDD - VSS	-0.5	+4.0	V
Input voltage range	OSC,SCL,SDA	Vi	-0.5	VDD +0.5	V
Input voltage range (LCD)		V_{LCD}	-0.5	+6.5	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-10°C	+50°C	-20°C	+65°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating voltage (Logic)	VDD-VSS		2.85	3.0	3.15	V
Operating voltage for LCD (built-in)	VLCD-VSS	Note 1	5.0	5.3	5.6	V
Input signal voltage low (SDA, SCL)	Vil		0	-	0.3 VDD	V
Input signal voltage high (SDA, SCL)	Vih		0.7 VDD	-	5.5	V
Operating supply current	I_{DD}	Character mode, VDD =3.0V	-	0.17	0.26	mA
		Checker board mode, VDD =3.0V	-	0.18	0.27	mA
Supply voltage of White LED05 backlight	VLED05	Forward current =15 mA Number of LED dies =1x1 =1.	3.8	4.0	4.2	V

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

Ta = -10 °C to +50 °C, VDD =1.8 ~ 5.5V, VSS=0V; V_{LCD}= 2.2V to 6.5V.

Refer to Fig. 6, I^2C Bus Timing Diagram of 'PHILIPS' PCF2119.

Table 6

Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
LCD frame frequency (internal clock) (note 1)	f_{FR}	45	81	147	Hz
Oscillator frequency(not available at any pin)	f_{OSC}	140	250	450	kHz
External clock frequency	$f_{OSC(ext)}$	tbf	-	450	kHz
Oscillator start-up time after power-down	t_{OSCST}	-	200	300	µs
Timing characteristics: I^2C-bus interface; (note 2)					
SCL clock frequency	f_{SCL}	-	-	400	kHz
SCL clock LOW period	t_{LOW}	1.3	-	-	µs
SCL clock HIGH period	t_{HIGH}	0.6	-	-	µs
Data set-up time	$t_{SU;DAT}$	100	-	-	ns
Data hold time	$t_{HD;DAT}$	0	-	-	ns
SCL and SDA rise time	t_r	-	-	300	ns
SCL and SDA fall time	t_f	-	-	300	ns
Capacitive bus line load	C_B			400	pF
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	-	µs
START condition hold time	$t_{HD;STA}$	0.6	-	-	µs
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	-	µs
Tolerable spike width on bus	t_{SW}	-	-	50	ns

Notes :

1 VDD=5.0V.

2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing to VSS to VDD.

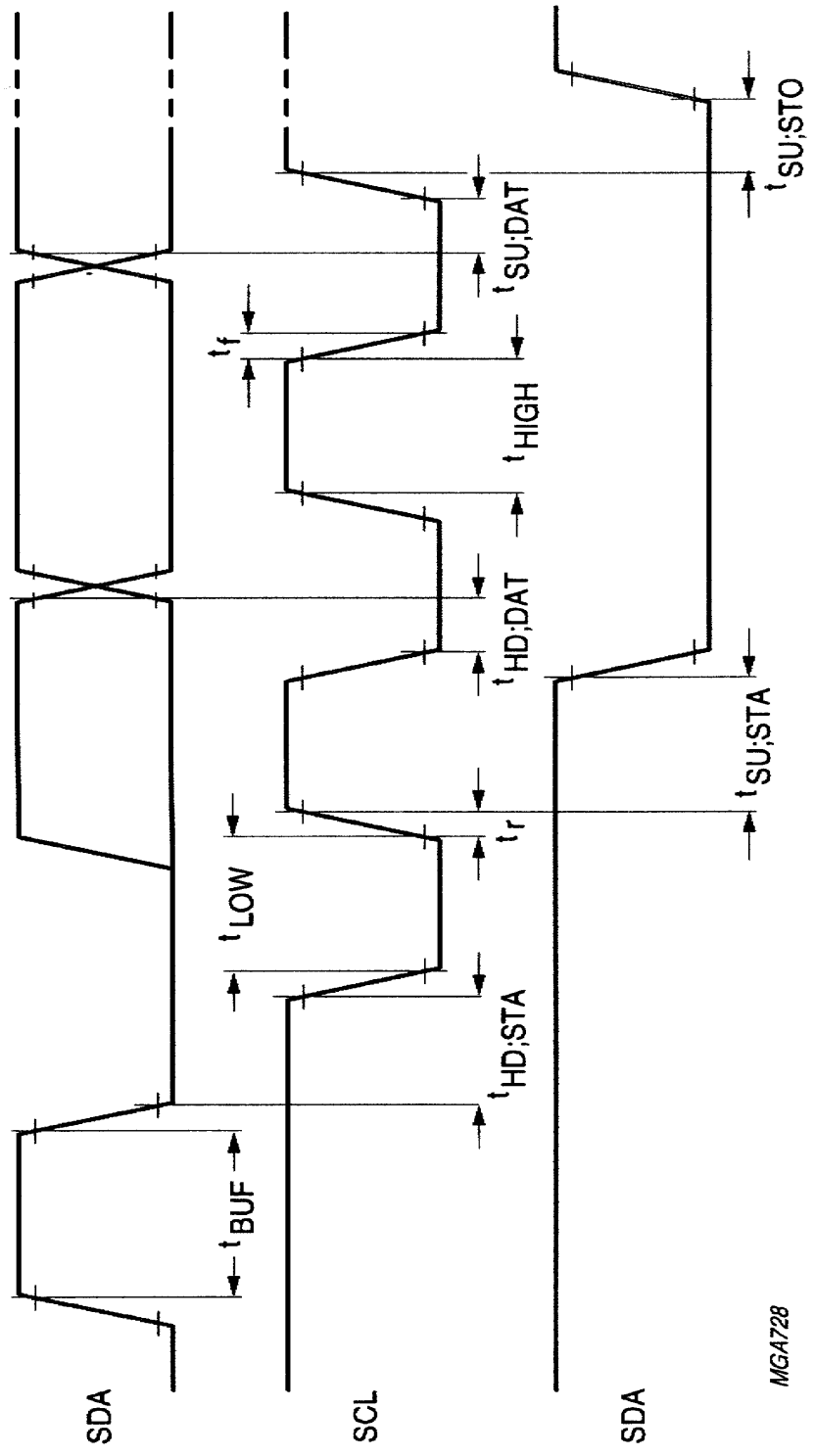


Figure 6: I^{2}C Bus Timing Diagram of 'PHILIPS' PCF2119.

6. Character Set 'R' in CGROM

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

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